FEATURES

- **Qualcomm Application Processor**
  - QCS5430:
    - **FP1**: Hex-core Kryo 670 CPU up to 2.1 GHz
    - **FP2**: Octa-core Kryo 670 CPU up to 2.2 GHz
    - **FP2.5**: Octa-core Kryo 670 CPU up to 2.4 GHz
    - **FP3**: Octa-core Kryo 670 CPU up to 2.4 GHz
  - QCS6490:
    - Octa-core Kryo 670 CPU up to 2.7 GHz
- **Memory**
  - Up to 8 GB LPDDR5
    - 32 bits wide
    - Up to 204.8Gbps read/write rate.
  - Up to 256 GB UFS
    - 8 bits wide
    - Up to 14/9.2Gbps read/write rate.
- **Integrated Power Management**
  - Power, Reset and Clock Management
  - Integrated USB-C power delivery with battery charging and operation.
  - Single input DC supply
  - Integrated supplies for external circuitry or for mobile applications
- **Mechanical**
  - 45mm (1.77”) x 45mm (1.77”) size
  - 2x 200 pin board to board connector
- **Processor IO**
  - 1 USB 2.0 On-The-Go (OTG) Port
  - 1 USB 3.1 Gen 1 Superspeed Port with DsiplayPort
  - 1 DisplayPort 1.4
  - 2 PCIe Gen 3*
  - 1 MIPI DSI D-PHY 1.2 or C-PHY 1.0
  - 5 MIPI CSI D-PHY 1.2 or C-PHY 1.2
  - 2 SDC
  - 3 UARTs
  - 3 SPI masters
  - 7 I2C controllers
  - 2 I3C controllers
  - 2 I2S controllers
  - 1 SoundWire controller
  - 2 UIM interfaces

APPLICATIONS

- Robotics
- Image Processing
- Test and Measurement
- Embedded AI processing
- Embedded Instrumentation
- Industrial Instrumentation
- Medical Instrumentation
- Mobile Applications

BENEFITS

- Rapid Development / Deployment
- Multiple Connectivity and I/O Options
- Rich User Interfaces
- High System Integration
- High Level OS Support
  - Android
  - Embedded Linux
  - Win 11 IoT Enterprise

* Feature pack 1 only supports 1 PCIe Gen 3

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Table 1: Processor Comparison Table

SOC	QCS5430				QCS6490
Configuration	FP1	FP2	FP2.5	FP3	-
CPU	2 x Kryo Prime up to 2.1 GHz	1 x Kryo Prime up to 2.2 GHz	1 x Kryo Prime up to 2.38 GHz		1 x Kryo Prime up to 2.7 GHz
	-	3 x Kryo Gold up to 2.13 GHz	3 x Kryo Gold up to 2.4 GHz		3 x Kryo Gold up to 2.4 GHz
	4 x Kryo Silver up to 1.8 GHz	4 x Kryo Silver up to 1.8 GHz	4 x Kryo Silver up to 1.8 GHz		4 x Kryo Silver up to 1.9 GHz
GPU	A642L @ 315 MHz FHD+ @ 120 Hz Encode / Decode: 4K30 / 4K60		A642L @ 520 MHz FHD+ @ 120 Hz Encode / Decode: 4K30 / 4K60		A643 @ 812 MHz FHD+ @ 144 Hz Encode / Decode: 4K30 / 4K60
AI-cDSP	2 x HVX 2K-HMX @ 912 MHz (~3.5 INT8 TOPS)		2 x HVX 2K-HMX @ 1.45 GHz (~6 INT8 TOPS)	2 x HVX 3K-HMX @ 1.45 GHz (~9 INT8 TOPS)	2 x GVK 4K-HMX @ 1.45 GHz (~12.15 INT8 TOPS)
Camera	2 x 22 MP @ 30 fps		36 MP + 22 MP @ 30 fps / 3 x 22 MP @ 30 fps		
PCIe	1 x Gen 3 1-lane	1 x Gen 3 1-lane			
	-	1 x Gen 3 2-lane			

1. Kryo Prime cores are custom ARM® Cortex®-A78 cores best for high-performance
2. Kryo Gold cores are custom ARM® Cortex®-A78 cores meant for balanced performance / power
3. Kryo Silver Cores are custom ARM® Cortex®-A55 cores ideal for light weight applications

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DESCRIPTION

The MitySOM-QC is a highly configurable, small form-factor System-on-Module (SOM) featuring a Qualcomm SoC processor. In addition to the processor, the module includes on-board power supplies, an LPDDR5 RAM memory subsystem, and a UFS configuration memory. The MitySOM-QC provides a complete and flexible CPU infrastructure for highly integrated embedded systems.

The MitySOM-QC is available with a Low Power Island (LPI) enabling limited operation at a low power draw while the rest of the processor is asleep.

Figure 1
~~Figure 1~~ illustrates a block diagram of the MitySOM-QC. As shown in the figure, the primary interface to the MitySOM-QC is through two 200 Pin vertical board-to-board mezzanine connectors. The MitySOM-QC is intended to interface to a carrier card base module for applications development. Details of the board-to-board interfaces are included in the Interface Description section.

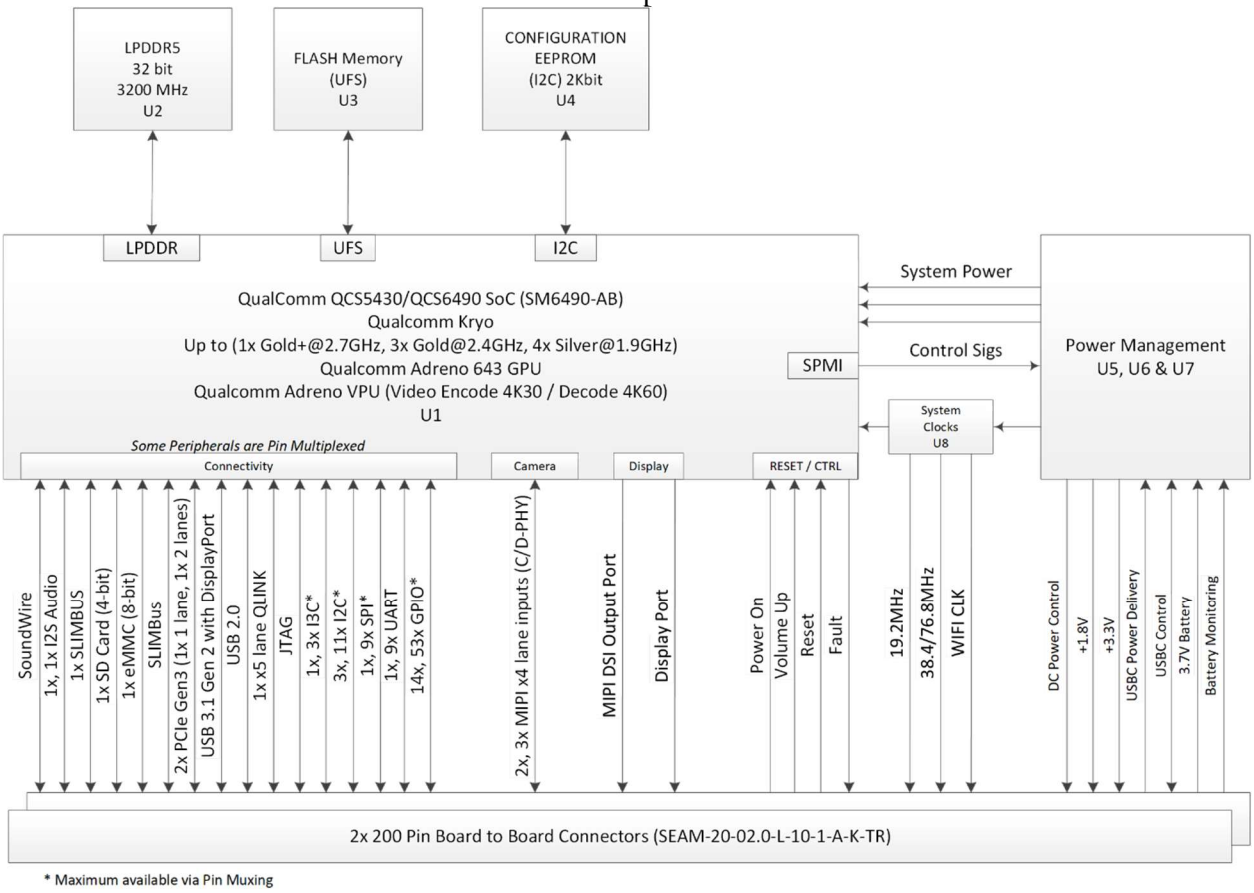

Figure 1 MitySOM-QC Block Diagram

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LPDDR5 Memory

The MitySOM-QC includes a dedicated 32-bit LPDDR5 memory interface that can address a maximum of 8GB of RAM.

The MitySOM-QC family adheres to Qualcomm's maximum memory speeds. The LPDDR memory is clocked at 3200Mhz by default.

Configuration EEPROM

MitySOM-QC modules contain a 2048 x 8-bit EEPROM that is used to hold factory configuration data for the module. The EEPROM is connected to the QCS5430/QCS6490 using the I2C0 interface. This EEPROM contains information such as the module type and Serial Number. This EEPROM is not available for customer use.

Console Serial port

The console serial port (DEBUG-RX/TX) is supported on pins B18 (RX) and A18 (TX) of the 200 pin Samtec connector (J2) with 1.8V compatible asynchronous UART I/O. By default, the flow control signals are not enabled but can be added to the console serial interface if desired.

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I2C0 Interface

The I2C0 peripheral is consumed local to the module. It is used for the Configuration EEPROM.

Table 2: I2C0 Peripherals

Address	Device	Feature
1010000	CAT24AA16TDI-GT3	256Kbit EEPROM for factory configuration parameters

Debug JTAG

The JTAG interface signals for the Qualcomm processor are available through the 200-pin Samtec connector (J1).

Table 3: JTAG Signals

JTAG Signal	Samtec Connector Pin	Processor Pin
SRSTn	D16	BR27
TCK	D15	BR29
TDI	D14	BN27
TDO	D13	BN29
TMS	D12	BM28
TRSTn	D11	BP28

SOM Clocking

The MitySOM-QC has a single clock generation IC to drive the processor as well as generate clocks for peripheral use. The two on-board clocks are the main processor clock which runs at 19.2MHz and a sleep clock at 32.7645kHz. On top of that, three output clocks are run to the external board to board connectors. There is one 19.2 MHz clock, and two software selectable clocks that can run at 38.4MHz or 76.8MHz. There is a dedicated 76.8Mhz oscillator to drive the clock generator.

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External Interfaces

The QCS5430/QCS6490 makes extensive use of functional pin multiplexing to provide a highly configurable device that can be tailored to a multitude of applications.

Processor Interfaces

A list of the interfaces/functions that are available to the user from the Processor is provided below.

- 1 Universal Serial Bus (USB) 3.1 Gen 1 Super-Speed Controller with DisplayPort 1.4
- 1 Universal Serial Bus (USB) 2.0 High-Speed On-The-Go Controller
- 1 DisplayPort 1.4
- 2 Peripheral Component Interconnect Express (PCIe) Gen 3
- 1 MIPI DSI D-PHY 1.2 or C-PHY 1.0
- 5 MIPI CSI D-PHY 1.2 or C-PHY 1.2
- 2 Secure Digital Interfaces (SDC) SD 3.0
- Up to 4 Improved Inter-Integrated Circuit (I3C) Ports
- Up to 14 Inter-Integrated Circuit (I2C) Ports
- Up to 10 Serial Peripheral (SPI) Ports
- Up to 10 Universal Asynchronous Receive/Transmit (UART) Ports
- 2 Inter-IC Sound (I2S) Ports
- 1 SoundWire (SWR) Port
- 2 Universal Interface Modules (UIM)
- Up to 67 1.8V GPIO

Configuration and Boot Modes

The QCS5430/QCS6490 BOOT-x pins (GPIO_118, GPIO_120, GPIO_122, GPIO 124) are used to configure the boot source. On the MitySOM-QC, the BOOT-x pins are strapped to fixed settings on the board as described below.

Boot Media Configuration

The QCS5430/QCS6490 can be configured to boot from various interfaces and configure the watchdog timer by pulling BOOT[3:0] either high or low. All The BOOT pins are pulled down to ground using 10k resistors on the SOM. This results in the SOM being configured to boot from its UFS interface and enable the watchdog timer by default. These bootstrapping pins are accessible to the user through pins A14, B14, C14 and D14 on the Samtec connector (J2).

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Debug LEDs

Power Status LEDs

D2 illuminates, green, when the MitySOM-QC on-module power supplies have been enabled in sequence and are operating correctly. This can also be disabled via GPIO pin 151 for low power applications.

Configurable RGB LED

D1 is a programable RGB that can be used for various uses. D1 is driven via the internal current driver of the PM7350C.

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Power Interfaces

The below sections provide details descriptions on the different use cases for powering the SOM. Additionally, a block diagram is provided in Figure 2 below.

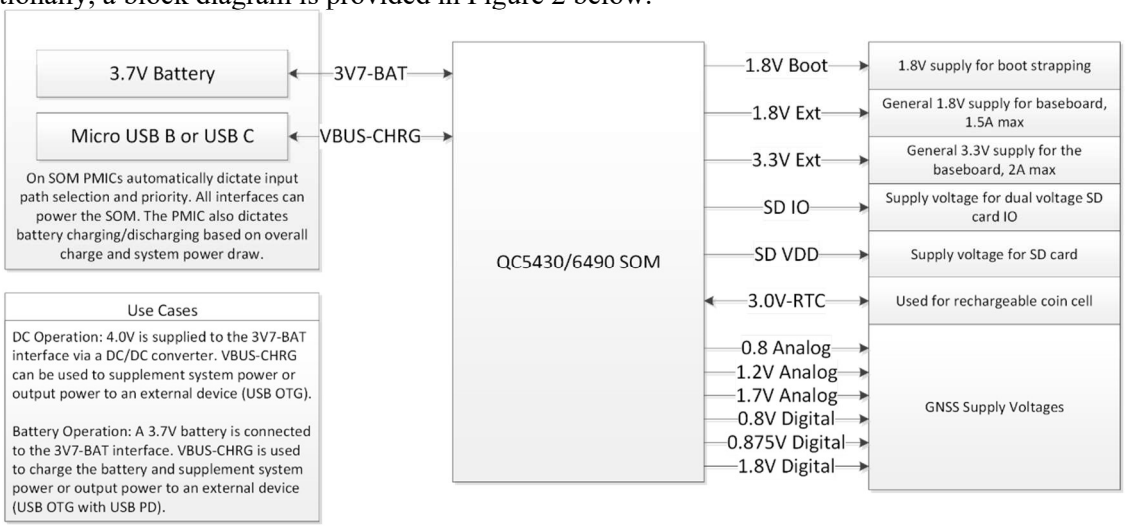

Figure 2 Primary power interfaces to the SOM (on the left) and secondary supplies to the SOM (on the right)

DC Input Voltage

For DC operation, a 4V source should be supplied to the 3V7-BAT pins on J2. If a DC voltage is applied to these pins, BATT-THERM should have a 100kΩ pulldown and BATT-ID should have a 10kΩ pulldown. The system reads this as a good battery charge and will draw power from this source as needed.

USB Input Voltage

A secondary method for powering the MitySOM-QC is via the VBUS-CHRG pins on J2. The MitySOM-QC accepts an input voltage of +5V DC and automatically negotiates power delivery with the power adapter.

3V7-BAT Input Voltage

Instead of a 4V DC voltage, a 3V7 lithium ion battery can be connected to the 3V7-BAT pins on J2. If a battery is connected to these pins, a 100kΩ NTC thermistor should be used to monitor the battery temperature. The thermistor should be connected between BATT-THERM and GND. An ID resistance of TBDΩ should be used to determine the battery profile. The ID resistor should be connected between BATT-ID and GND.

Battery Charging

If a battery is connected to the 3V7-BAT pins, power will be drawn from the VBUS-CHRG connector (when applicable) and used to charge the battery. If the system power draw ever exceeds the supply from VBUS-CHRG, power will be supplemented from the battery.

Power utilization of the MitySOM-QC is heavily dependent on end-user application. Major factors include: CPU configuration, CPU Utilization, and LPDDR5 RAM utilization.

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Power Sequencing

The state of the local power supplies is provided on J1 via the external 1.8V and 3.3V supplies. Until either of these supplies come up, the local SOM power supplies should not be assumed to be on and stable. Either of these supplies should be used to sequence or enable any user IO to the module.

Software Development Support

Users of the MitySOM-QC are encouraged to develop applications using the GCC based MitySOM-QC software development kit (SDK) provided by Critical Link LLC. The SDK is an expansion of the Qualcomm platform support package for the QCS5430/QCS6490 and includes an implementation of a Yocto Project-compatible board support package providing a Linux root filesystem/distribution and compatible gcc compiler tool-chain with debugger.

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Growth Options

The MitySOM-QC has been designed to support several upgrade options. These options include a range of speed grades, DDR memory configurations and UFS memory configurations. The available options are listed in the section below containing ordering information. For additional ordering information and details regarding these options, or to inquire about a configuration not listed below, please contact Critical Link at info@criticallink.com.

Absolute Maximum Ratings

If Military/Aerospace specified cards are required, please contact Critical Link at info@criticallink.com for availability and specifications.

Table 4: Absolute Maximum Ratings

Maximum Supply Voltage (VBUS-CHRG)	28 V
Maximum Battery Voltage (3V7-BAT)	6V
Storage Temperature Range	-55ºC to 150ºC

Operating Conditions

The following are the minimum temperature ratings for the components that are installed on a MitySOM-QC. For specifications not contained in this table please contact Critical Link at info@criticallink.com.

Table 5: Module Component Temperature Ratings

Temperature Range	Component Ratings*
Wireless (-RL)	-25ºC to 80ºC

**** Please see the Thermal Management section below for ambient/operating temperature recommendations.***

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Thermal Management

The MitySOM-QC module requires careful consideration of thermal management. Depending on load, different thermal management will be required for operation at room temperatures and above. The primary thermal concern is with the QCS5430/QCS6490 SoC device. Additional processing activity will require more power consumption and more heat dissipation.

Thermal management is a system level issue that must be addressed in conjunction with the overall system design. Some systems may have available airflow with limited space for a heat sink; others may have room for a heat sink with or without the possibility for additional airflow. As a result, the approach taken for thermal management is a design consideration that must be addressed by the overall system designers when integrating the MitySOM-QC.

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J1/J2 Connector Interface

The next sections outline the connector pin interface. The pin interfaces are grouped into the signal classes defined in the table below.

Table 6: Connector Interface Signal Class Groups

Class	Applicable IO Standard	Description
POWER	N/A	These are module power input pins and corresponding return pins.
IO	1.8V CMOS	These pins provide single-ended input/output buffers that support 1.8V CMOS logic.
I	1.8V CMOS	These pins provide single-ended input buffers that support 1.8V CMOS logic.
O	1.8V CMOS	These pins provide single-ended output buffers that support 1.8V CMOS logic.

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J1 Interface Description

The connector used for J1 is a 200 Pin Samtec SEAF series connector, SEAF-20-05.0-L-10-1-A-K-TR, which mates with Samtec SEAM-20-02.0-L-10-1-A-K-TR (the mating height, indicated by the 02.0 in the part number may be taller if desired). The connector is logically broken up into 10 groups (rows) of 20 pins as documented below.

Table 7 contains a summary of the MitySOM-QC J1 Interface pin-mapping.

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Table 7: MitySOM-QC J1 Connector Pin-Out

J1 Pin	Class	Schematic Net Name	Processor Pin	Signal Options
A1	O	DSI0-CLK_N	AC45	MIPI DSI 0 (D-PHY), differential clock – negative MIPI DSI 0 (C-PHY), trio lane 1 – C
A2	O	DSI0-CLK_P	AC43	MIPI DSI 0 (D-PHY), differential clock – positive MIPI DSI 0 (C-PHY), trio lane 1 – B
A3	P	GND	-	-
A4	O	DSI0-LN1_N	AD44	MIPI DSI 0 (D-PHY), differential lane 1 – negative MIPI DSI 0 (C-PHY), trio lane 1 – A
A5	O	DSI0-LN1_P	AE43	MIPI DSI 0 (D-PHY), differential lane 1 – positive MIPI DSI 0 (C-PHY), trio lane 0– C
A6	O	DSI0-LN3_N	AD46	MIPI DSI 0 (D-PHY), differential lane 3 – negative MIPI DSI 0 (C-PHY), no connect
A7	O	DSI0-LN3_P	AE45	MIPI DSI 0 (D-PHY), differential lane 3 – positive MIPI DSI 0 (C-PHY), trio lane 2 – C
A8	O	DSI0-LN2_N	AF46	MIPI DSI 0 (D-PHY), differential lane 2 – negative MIPI DSI 0 (C-PHY), trio lane 2 – B
A9	O	DSI0-LN2_P	AF44	MIPI DSI 0 (D-PHY), differential lane 2 – positive MIPI DSI 0 (C-PHY), trio lane 2 – A
A10	O	DSI0-LN0_N	AG45	MIPI DSI 0 (D-PHY), differential lane 0 – negative MIPI DSI 0 (C-PHY), trio lane 0 – B
A11	O	DSI0-LN0_P	AG43	MIPI DSI 0 (D-PHY), differential lane 0 – positive MIPI DSI 0 (C-PHY), trio lane 0 – A
A12	P	uSD-VDD	-	Voltage supply for uSD card
A13	IO	SDC2-DATA3	AT42	Secure digital controller 2 data bit 3
A14	IO	SDC2-DATA2	AT46	Secure digital controller 2 data bit 2
A15	IO	SDC2-DATA1	AR45	Secure digital controller 2 data bit 1
A16	IO	SDC2-DATA0	AR43	Secure digital controller 2 data bit 0
A17	O	SDC2-CMD	AR41	Secure digital controller 2 command
A18	P	GND	-	-
A19	O	SDC2-CLK	AT44	Secure digital controller 2 clock
A20	P	uSD-IO	-	IO voltage for the SDC2 signals

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J1 Pin	Class	Schematic Net Name	Processor Pin	Signal Options
B1	IO	LQ-1-L0-2-L4	G45	Configurable I/O LPI GPIO 17 LPI_QUP0 SE1, lane 0: I2C_SDA LPI_QUP0 SE1, lane 0: I3C_SDA LPI_QUP0 SE2, lane 4: SPI_CS_1 Sync out GPIO_2
B2	IO	LQ-1-L1	H46	Configurable I/O LPI GPIO 18 LPI_QUP0 SE1, lane 1: I2C_SCL LPI_QUP0 SE1, lane 1: I3C_SCL Sync out GPIO_3
B3	IO	LQ-2-L2	K46	Configurable I/O QDSS trigger output 0 B LPI GPIO 21 LPI_QUP0 SE2, lane 2: UART_TX LPI_QUP0 SE2, lane 2: SPI_SCLK Sync out GPIO_6
B4	I	HOMEn	-	Active low home signal
B5	IO	I2S1-WS	U47	Configurable I/O LPI GPIO 11 LPI I2S 2 Word select SoundWire data for WSA
B6	IO	I2S1-D1	V46	Configurable I/O QDSS trigger input 1 B LPI GPIO 13 LPI DMIC 3 data LPI I2S 2 data 1 External master clock 1 A
B7	IO	SLIMBUS_CLK	W45	Configurable I/O Low-power audio SLIMbus clock
B8	IO	SLIMBUS_DAT	Y46	Configurable I/O Low-power audio SLIMbus data 0
B9	IO	Q1-0-L2	AY42	Configurable I/O QUP1 SE0, lane 2: UART_TX QUP1 SE0, lane 2: SPI_SCLK
B10	IO	PWM1	AU43	Configurable I/O MI^{2}S 1 clock General purpose clock 2 A QDSS trace data bit 5 B
B11	P	GND	-	-
B12	IO	SMB-SPMI-CLK	AW41	Configurable I/O QUP1 SE0, lane 1: UART_RFR QUP1 SE0, lane 1: I2C_SCL QUP1 SE0, lane 1: SPI_MOSI
B13	IO	SMB-SPMI-DAT	AW43	Configurable I/O QUP1 SE0, lane 0: UART_CTS QUP1 SE0, lane 0: I2C_SDA QUP1 SE0, lane 0: SPI_MISO
B14	I	USB-OPT	-	USB0 options. Tie to GND for µSD or leave floating for USBC
B15	I	SMB-THERM	-	Thermistor for parallel charger
B16	I	USB0-THERM	-	100kΩ NTC thermistor for USB connector
B17	I	BATT-THERM	-	100kΩ NTC thermistor for battery
B18	I	SMB-ISNS	-	Current sense for parallel charger
B19	I	BATT-ID	-	Battery ID signal
B20	I	SMB-EN	-	Enable for parallel charger

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J1 Pin	Class	Schematic Net Name	Processor Pin	Signal Options
C1	IO	LQ-0-L1	G47	Configurable I/O LPI GPIO 16 LPI_QUP0 SE0, lane 1: I2C_SCL LPI_QUP0 SE0, lane 1: I3C_SCL Sync out GPIO_1
C2	IO	LQ-2-L0	J47	Configurable I/O LPI GPIO 19 LPI_QUP0 SE2, lane 0: UART_CTS LPI_QUP0 SE2, lane 0: I2C_SDA LPI_QUP0 SE2, lane 0: SPI_MISO Sync out GPIO_4
C3	IO	LQ-2-L1	J45	Configurable I/O LPI GPIO 20 LPI_QUP0 SE2, lane 1: UART_RFR LPI_QUP0 SE2, lane 1: I2C_SCL LPI_QUP0 SE2, lane 1: SPI_MOSI Sync out GPIO_5
C4	IO	LQ-2-L3	L47	Configurable I/O QDSS trigger output 1 B LPI GPIO 22 LPI_QUP0 SE2, lane 3: UART_RX LPI_QUP0 SE2, lane 3: SPI_CS_0 Sync out GPIO_7
C5	IO	I2S1-CLK	T46	Configurable I/O LPI GPIO 10 LPI MI^{2}S 2 clock SoundWire clock for WSA
C6	IO	I2S1-D0	U45	Configurable I/O QDSS trigger input 0 B LPI GPIO 12 LPI DMIC 3 clock LPI I2S 2 Data 0
C7	IO	Q1-3-L2	BC41	Configurable I/O QUP1 SE3, lane 2: UART_TX QUP1 SE3, lane 2: SPI_SCLK
C8	IO	PWM0	AW45	Configurable I/O Secondary MI^{2}S master clock MI^{2}S 1 serial data channel 1 Audio reference clock General purpose clock 1 A QDSS trace data bit 4 B
C9	IO	Q1-0-L3	BA43	Configurable I/O QUP1 SE0, lane 3: UART_RX QUP1 SE0, lane 3: SPI_CS_0
C10	IO	Q1-4-L2	BC45	Configurable I/O QUP1 SE4, lane 2: UART_TX QUP1 SE4, lane 2: SPI_SCLK QUP1 SE6, lane 6: SPI_CS_3
C11	IO	Q1-2-L3	BB46	Configurable I/O QUP1 SE2, lane 3: UART_RX QUP1 SE2, lane 3: SPI_CS_0
C12	IO	Q1-4-L0	BB44	Configurable I/O QUP1 SE4, lane 0: UART_CTS QUP1 SE4, lane 0: I2C_SDA QUP1 SE4, lane 0: SPI_MISO
C13	IO	Q1-2-L2	BA45	Configurable I/O QUP1 SE2, lane 2: UART_TX QUP1 SE2, lane 2: SPI_SCLK
C14	P	GND	-	-
C15	I	SMB-STAT	-	Status of parallel charger
C16	I	VBAT-SNS_P	-	Battery voltage sense
C17	I	VBAT-SNS_N	-	Battery voltage sense
C18	I	VBAT-ISNS_N	-	Battery current sense
C19	I	VBAT-ISNS_P	-	Battery current sense
C20	I	VBAT-PACK-SNSn	-	Negative battery terminal

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J1 Pin	Class	Schematic Net Name	Processor Pin	Signal Options
D1	IO	I2S0-D1	AB46	Configurable I/O MI^{2}S 0 serial data channel 1
D2	IO	I2S0-D0	AB44	Configurable I/O MI^{2}S 0 serial data channel 0
D3	IO	I2S0-WS	AH46	Configurable I/O MI^{2}S 0 serial data word select
D4	IO	I2S0-CLK	AA47	Configurable I/O MI^{2}S 0 clock
D5	IO	SW0-RX-D1	M46	Configurable I/O LPI GPIO 5 SoundWire receive data 1 External master clock 1 C LPI quaternary MI^{2}S data 3
D6	IO	SW0-RX-D0	L45	Configurable I/O LPI GPIO 4 SoundWire receive data 0 LPI quaternary MI^{2}S data 2
D7	IO	SW0-RX-CLK	N47	Configurable I/O LPI GPIO 3 SoundWire receive clock LPI quaternary MI^{2}S data 1
D8	IO	SW0-TX-D1	P44	Configurable I/O LPI GPIO 2 SoundWire transmit data 1 LPI quaternary MI^{2}S data 0
D9	IO	SW0-TX-D0	P46	Configurable I/O LPI GPIO 1 SoundWire transmit data 0 LPI quaternary MI^{2}S word select
D10	IO	SW0-TX-CLK	N45	Configurable I/O LPI GPIO 0 SoundWire transmit clock LPI quaternary MI^{2}S clock
D11	I	JTAG-TRSTn	BP28	JTAG reset
D12	I	JTAG-TMS	BM28	JTAG mode select input
D13	O	JTAG-TDO	BN29	JTAG data output
D14	I	JTAG-TDI	BN27	JTAG data input
D15	I	JTAG-TCK	BR29	JTAG clock input
D16	I	JTAG-SRSTn	BR27	JTAG reset for debug
D17	IO	Q1-3-L1	BB42	Configurable I/O QUP1 SE3, lane 1: UART_RFR QUP1 SE3, lane 1: I2C_SCL QUP1 SE3, lane 1: SPI_MOSI
D18	IO	Q1-3-L0	BA41	Configurable I/O QUP1 SE3, lane 0: UART_CTS QUP1 SE3, lane 0: I2C_SDA QUP1 SE3, lane 0: SPI_MISO
D19	IO	GPIO115	BM42	Configurable I/O UIM0_RESET
D20	IO	GPIO116	BM44	Configurable I/O UIM0 presence detection

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J1 Pin	Class	Schematic Net Name	Processor Pin	Signal Options
E1	IO	Q1-5-L0	BD44	Configurable I/O QUP1 SE5, lane 0: UART_CTS QUP1 SE5, lane 0: I2C_SDA QUP1 SE5, lane 0: SPI_MISO
E2	IO	Q1-5-L1	BE45	Configurable I/O QUP1 SE5, lane 1: UART_RFR QUP1 SE5, lane 1: I2C_SCL QUP1 SE5, lane 1: SPI_MOSI
E3	I	POW-BTNn	-	Active low power signal
E4	IO	Q1-5-L3-4-L4	BE43	Configurable I/O QUP1 SE5, lane 3: UART_RX QUP1 SE5, lane 3: SPI_CS_0 QUP1 SE4, lane 4: SPI_CS_1
E5	IO	Q1-6-L1	BF44	Configurable I/O QUP1 SE6, lane 1: UART_RFR QUP1 SE6, lane 1: I2C_SCL QUP1 SE6, lane 1: SPI_MOSI
E6	IO	Q1-6-L3	BG45	Configurable I/O QUP1 SE6, lane 3: UART_RX QUP1 SE6, lane 3: SPI_CS_0 QDSS trace clock B
E7	IO	Q1-1-L3	BH44	Configurable I/O QUP1 SE1, lane 3: UART_RX QUP1 SE1, lane 3: SPI_CS_0
E8	IO	Q1-1-L1	BG43	Configurable I/O QUP1 SE1, lane 1: UART_RFR QUP1 SE1, lane 1: I2C_SCL QUP1 SE1, lane 1: SPI_MOSI QUP 1SE1, lane 1: I3C_SCL
E9	IO	Q1-1-L0	BF42	Configurable I/O QUP1 SE1, lane 0: UART_CTS QUP1 SE1, lane 0: I2C_SDA QUP1 SE1, lane 0: SPI_MISO QUP 1SE1, lane 0: I3C_SDA
E10	IO	FORCE-USB-BOOT	BK44	Configurable I/O Forced USB boot
E11	O	FAULTn	-	Active low fault signal
E12	IO	EDP-DETECT	BH42	Configurable I/O QUP1 SE7, lane 0: UART_CTS QUP1 SE7, lane 0: I2C_SDA QUP1 SE7, lane 0: SPI_MISO eDP hot plug detect
E13	IO	I2S0-MCLK	AA45	Configurable I/O Primary MI^{2}S master clock
E14	IO	GPIO109	BL47	Configurable I/O UIM1 data (dual voltage)
E15	IO	GPIO110	BM46	Configurable I/O UIM1 clock (dual voltage)
E16	I	MODE-0	BR31	Mode control bit 0 – unconnected for native mode
E17	IO	Q1-2-L0	AY46	Configurable I/O QUP1 SE2, lane 0: UART_CTS QUP1 SE2, lane 0: I2C_SDA QUP1 SE2, lane 0: SPI_MISO
E18	IO	Q1-2-L1	AY44	Configurable I/O QUP1 SE2, lane 1: UART_RFR QUP1 SE2, lane 1: I2C_SCL QUP1 SE2, lane 1: SPI_MOSI
E19	IO	GPIO113	BR45	Configurable I/O UIM0 data (dual voltage)
E20	IO	GPIO114	BN43	Configurable I/O UIM0 clock (dual voltage)

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J1 Pin	Class	Schematic Net Name	Processor Pin	Signal Options
F1	P	3V3-SOM	-	External 3.3V Supply
F2	P	3V3-SOM	-	External 3.3V Supply
F3	IO	Q1-4-L3	BD46	Configurable I/O QUP1 SE4, lane 3: UART_RX QUP1 SE4, lane 3: SPI_CS_0
F4	IO	Q1-6-L0	BF46	Configurable I/O QUP1 SE6, lane 0: UART_CTS QUP1 SE6, lane 0: I2C_SDA QUP1 SE6, lane 0: SPI_MISO
F5	IO	Q1-6-L2	BG47	Configurable I/O QUP1 SE6, lane 2: UART_TX QUP1 SE6, lane 2: SPI_SCLK QDSS trace control B
F6	IO	Q1-1-L2-4-L6	BH46	Configurable I/O QUP1 SE1, lane 2: UART_TX QUP1 SE1, lane 2: SPI_SCLK QUP1 SE4, lane 6: SPI_CS_3
F7	IO	Q1-5-L2-4-L5	BD42	Configurable I/O QUP1 SE5, lane 2: UART_TX QUP1 SE5, lane 2: SPI_SCLK QUP1 SE4, lane 5: SPI_CS_2
F8	P	GND	-	-
F9	P	GND	-	-
F10	O	USB0-SBU2	-	SBU2 signal for USB 3.0 connector
F11	I	USB0-SBU1	-	SBU1 signal for USB 3.0 connector
F12	P	GND	-	-
F13	P	GND	-	-
F14	I	USB0-CC2	-	CC2 signal for USB 3.0 connector
F15	I	USB0-CC1	-	CC2 signal for USB 3.0 connector
F16	P	GND	-	-
F17	P	GND	-	-
F18	P	1V8-SOM	-	External 1.8V Supply
F19	IO	Q1-3-L3-DP-HPD	BC43	Configurable I/O QUP1 SE3, lane 3: UART_RX QUP1 SE3, lane 3: SPI_CS_0 DisplayPort hot plug detect
F20	I	PS-HOLD	C47	Power-supply hold signal to PMIC
-	-	-	-	-
G1	IO	Q1-4-L1	BC47	Configurable I/O QUP1 SE4, lane 1: UART_RFR QUP1 SE4, lane 1: I2C_SCL QUP1 SE4, lane 1: SPI_MOSI
G2	P	GND	-	-
G3	P	GND	-	-
G4	I	VOL-UPn	-	Active low volume increase
G5	I	RESINn	-	Active low reset
G6	P	GND	-	-
G7	P	GND	-	-
G8	O	DP-TX2_P	AK44	eDP 1.4 transmit channel 2 – positive
G9	O	DP-TX2_N	AK46	eDP 1.4 transmit channel 2 – negative
G10	P	GND	-	-
G11	P	GND	-	-
G12	I	PCIE1-RX1_N	BN37	PCIe 1 Gen 3 receive lane 1 – negative
G13	I	PCIE1-RX1_P	BL37	PCIe 1 Gen 3 receive lane 1 – positive
G14	P	GND	-	-
G15	P	GND	-	-
G16	I	USB0-RX1_P	BJ31	USB 3.0 Type-C PHY receiver 1 – positive
G17	I	USB0-RX1_N	BL31	USB 3.0 Type-C PHY receiver 1 – negative
G18	P	GND	-	-
G19	P	GND	-	-
G20	O	19M2-CLK	-	19.2MHz output clock

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J1 Pin	Class	Schematic Net Name	Processor Pin	Signal Options
H1	P	GND	-	-
H2	I	PCIE1-RX0_N	BM40	PCIe 1 Gen 3 receive lane 0 – negative
H3	I	PCIE1-RX0_P	BP40	PCIe 1 Gen 3 receive lane 0 – positive
H4	P	GND	-	-
H5	P	GND	-	-
H6	O	PCIE1-TX1_P	BP38	PCIe 1 Gen 3 Transmit lane 1 – posiive
H7	O	PCIE1-TX1_N	BM38	PCIe 1 Gen 3 Transmit lane 1 – negative
H8	P	GND	-	-
H9	P	GND	-	-
H10	O	DP-TX1_P	AL45	eDP 1.4 transmit channel 1 – positive
H11	O	DP-TX1_N	AL47	eDP 1.4 transmit channel 1 – negative
H12	P	GND	-	-
H13	P	GND	-	-
H14	O	DP-TX0_N	AM46	eDP 1.4 transmit channel 0 – negative
H15	O	DP-TX0_P	AM44	eDP 1.4 transmit channel 0 – positive
H16	P	GND	-	-
H17	P	GND	-	-
H18	IO	DP-AUX_N	AN45	eDP 1.4 auxiliary channel – negative
H19	IO	DP-AUX_P	AN43	eDP 1.4 auxiliary channel – positive
H20	P	GND	-	-
-	-	-	-	-
I1	O	GNSS-CLK	-	38.4MHz or 76.8MHz output clock for GNSS
I2	P	GND	W45	Configurable I/O Low-power audio SLIMbus clock
I3	P	GND	Y46	Configurable I/O Low-power audio SLIMbus data 0
I4	O	PCIE1-REFCLK_N	BP36	PCIe 1 Gen 3 reference clock – negative
I5	O	PCIE1-REFCLK_P	BM36	PCIe 1 Gen 3 reference clock – positive
I6	P	GND	-	-
I7	P	GND	-	-
I8	O	PCIE1-TX0_N	BN39	PCIe 1 Gen 3 Transmit lane 0 – negative
I9	O	PCIE1-TX0_P	BR39	PCIe 1 Gen 3 Transmit lane 0 – positive
I10	P	GND	-	-
I11	P	GND	-	-
I12	IO	USB0-DP-AUX_P	BK30	DisplayPort auxiliary channel – positive
I13	IO	USB0-DP-AUX_N	BM30	DisplayPort auxiliary channel – negative
I14	P	GND	-	-
I15	P	GND	-	-
I16	O	USB0-TX1_N	BK32	USB 3.0 Type-C PHY transmit 1 – negative
I17	O	USB0-TX1_P	BM32	USB 3.0 Type-C PHY transmit 1 – positive
I18	P	GND	-	-
I19	P	GND	-	-
I20	O	38M4-76M8-CLK	-	38.4MHz or 76.8MHz output clock
-	-	-	-	-
J1	P	GND	-	-
J2	O	DP-TX3_P	AJ43	eDP 1.4 transmit channel 3 – positive
J3	O	DP-TX3_N	AJ45	eDP 1.4 transmit channel 3 – negative
J4	P	GND	-	-
J5	P	GND	-	-
J6	IO	USB1-HS_P	BH26	USB1_HS – positive
J7	IO	USB1-HS_N	BJ25	USB1_HS – negative
J8	P	GND	-	-
J9	P	GND	-	-
J10	I	USB0-RX0_N	BK34	USB 3.0 Type-C PHY receiver 0 – negative
J11	I	USB0-RX0_P	BM34	USB 3.0 Type-C PHY receiver 0 – positive
J12	P	GND	-	-
J13	P	GND	-	-
J14	O	USB0-TX0_N	BL33	USB 3.0 Type-C PHY transmit 0 – negative
J15	O	USB0-TX0_P	BN33	USB 3.0 Type-C PHY transmit 0 – positive
J16	P	GND	-	-
J17	P	GND	-	-
J18	IO	USB0-HS_N	BJ27	USB 2.0 high-speed data – negative
J19	IO	USB0-HS_P	BH28	USB 2.0 high-speed data – positive
J20	P	GND	-	-

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J2 Interface Description

The connector used for J2 is a 200 Pin Samtec SEAF series connector, SEAF-20-05.0-L-10-1-A-K-TR, which mates with Samtec SEAM-20-02.0-L-10-1-A-K-TR (the mating height, indicated by the 02.0 in the part number may be taller if desired). The connector is logically broken up into 10 groups (rows) of 20 pins as documented below.

Table 8
~~Table 8~~ contains a summary of the MitySOM-QC J2 Interface pin-mapping.

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Table 8: MitySOM-QC J2 Connector Pin-Out

J2 Pin	Class	Schematic Net Name	Processor Pin	Signal Options
A1	O	SDC1-CLK	G3	Secure digital controller 1 clock
A2	IO	Q0-3-L0	M2	Configurable I/O QUP0 SE3, lane 0: UART_CTS QUP0 SE3, lane 0: I2C_SDA QUP0 SE3, lane 0: SPI_MISO QDSS trace control A
A3	I	CSI4-LN1_P	AA7	MIPI CSI 4 (D-PHY), differential lane 1 – positive MIPI CSI 4 (C-PHY), trio lane 1 – A
A4	I	CSI4-LN0_P	AB8	MIPI CSI 4 (D-PHY), differential lane 0 – positive MIPI CSI 4 (C-PHY), trio lane 0 – B
A5	IO	Q0-4-L3	N3	Configurable I/O QUP0 SE4, lane 3: UART_RX QUP0 SE4, lane 3: SPI_CS_0
A6	I	CSI3-LN2_N	AF4	MIPI CSI 3 (D-PHY), differential lane 2 – negative MIPI CSI 3 (C-PHY), trio lane 2 – A
A7	I	CSI3-LN3_N	AG5	MIPI CSI 3 (D-PHY), differential lane 3 – negative MIPI CSI 3 (C-PHY), trio lane 2 – C
A8	IO	LQ-5-L0-L2	C45	Configurable I/O QDSS trace data bit 12 B LPI GPIO 23 LPI_QUP0 SE5, lane 0: I2C_SDA LPI_QUP0 SE5, lane 2: UART_TX Sync out GPIO_12
A9	I	CSI2-LN1_N	AJ3	MIPI CSI 2 (D-PHY), differential lane 1 – negative MIPI CSI 2 (C-PHY), trio lane 1 – B
A10	I	CSI2-LN3_N	AL7	MIPI CSI 2 (D-PHY), differential lane 3 – negative MIPI CSI 2 (C-PHY), trio lane 2 – C
A11	IO	LQ-6-L2	E47	Configurable I/O QDSS trace data bit 14 B LPI GPIO 25 LPI_QUP0 SE6, lane 2: UART_TX Sync out GPIO_14
A12	I	CSI1-LN0_P	AP6	MIPI CSI 1 (D-PHY), differential lane 0 –positive MIPI CSI 1 (C-PHY), trio lane 0 – B
A13	I	CSI1-LN3_N	AR7	MIPI CSI 1 (D-PHY), differential lane 3 – negative MIPI CSI 1 (C-PHY), trio lane 2 – C
A14	IO	GPIO118-B0	BM6	Configurable I/O RF front end 0 interface data Boot configuration control bit 0
A15	IO	CSI-I2C3-SCL	BA7	Configurable I/O Dedicated camera control interface I^2C 3 clock Global general purpose clock 1 B
A16	IO	CSI-I2C2-SCL	BA3	Configurable I/O Dedicated camera control interface I^2C 2 clock
A17	IO	PCIE0-CLKREQn	BL9	Configurable I/O PCIe clock request
A18	IO	DEBUG-TX	BF6	Configurable I/O QUP0 SE5, lane 2: UART_TX QUP0 SE5, lane 2: SPI_SCLK QDSS trace data 8
A19	IO	Q0-6-L3	BD2	Configurable I/O QUP0 SE6, lane 3: UART_RX QUP0 SE6, lane 3: SPI_CS_0 QDSS trace data 13
A20	IO	PCIE1-CLKREQn	BH6	Configurable I/O Camera control interface timer 4 Camera control interface async 2 PCIe1 clock request signal MDP vertical sync – external

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J2 Pin	Class	Schematic Net Name	Processor Pin	Signal Options
B1	O	SDC1-CMD	H4	Secure digital controller 1 command
B2	IO	Q0-1-L1	BN3	Configurable I/O QUP0 SE1, lane 1:UART_RFR QUP0 SE1, lane 1: I2C_SCL QUP0 SE1, lane 1: SPI_MOSI QUP 0 SE1, lane 1: I3C_SCL
B3	I	CSI4-LN1_N	AA5	MIPI CSI 4 (D-PHY), differential lane 1 – negative MIPI CSI 4 (C-PHY), trio lane 1 – B
B4	I	CSI4-LN0_N	AB6	MIPI CSI 4 (D-PHY), differential lane 0 – negative MIPI CSI 4 (C-PHY), trio lane 0 – C
B5	IO	Q0-1-L0	BP2	Configurable I/O QUP0 SE1, lane 0 UART_CTS QUP0 SE1, lane 0 I2C_SDA QUP0 SE1, lane 0 SPI_MISO QUP 0 SE1, lane 0: I3C_SDA
B6	I	CSI3-LN2_P	AF2	MIPI CSI 3 (D-PHY), differential lane 2 – positive MIPI CSI 3 (C-PHY), trio lane 1 – C
B7	I	CSI3-LN3_P	AG3	MIPI CSI 3 (D-PHY), differential lane 3 – positive MIPI CSI 3 (C-PHY), trio lane 2 – B
B8	IO	Q0-1-L2	BN1	Configurable I/O QUP0 SE1, lane 2: UART_TX QUP0 SE1, lane 2: SPI_SCLK QUP0 SE7, lane 6: SPI_CS_3
B9	I	CSI2-LN1_P	AJ1	MIPI CSI 2 (D-PHY), differential lane 1 – positive MIPI CSI 2 (C-PHY), trio lane 1 – A
B10	I	CSI2-LN3_P	AL5	MIPI CSI 2 (D-PHY), differential lane 3 – positive MIPI CSI 2 (C-PHY), trio lane 2 – B
B11	IO	Q0-1-L3	BM2	Configurable I/O QUP0 SE1, lane 3: UART_RX QUP0 SE1, lane 3: SPI_CS_0
B12	I	CSI1-LN0_N	AP4	MIPI CSI 1 (D-PHY), differential lane 0 – negative MIPI CSI 1 (C-PHY), trio lane 0 – C
B13	I	CSI1-LN3_P	AR5	MIPI CSI 1 (D-PHY), differential lane 3 – positive MIPI CSI 1 (C-PHY), trio lane 2 – B
B14	IO	GPIO124-B3	BL3	Configurable I/O Boot configuration control bit 3
B15	IO	CSI-I2C3-SDA	BA5	Configurable I/O Dedicated camera control interface I^2C 3 serial data
B16	IO	CSI-I2C2-SDA	BA1	Configurable I/O Dedicated camera control interface I^2C 2 serial data
B17	IO	Q0-6-L2	BE3	Configurable I/O QUP0 SE6, lane 2: UART_TX QUP0 SE6, lane 2: SPI_SCLK QDSS trace data bit 12 A
B18	IO	DEBUG-RX	BF4	Configurable I/O QUP0 SE5, lane 3: UART_RX QUP0 SE5, lane 3: SPI_CS_0 QDSS trace data 9
B19	IO	GPIO-128-B10	BK8	Configurable I/O Interface between WCN and QCS6490 Boot configuration control bit 10
B20	I	MODE-1	BP30	Mode control bit 1 – unconnected for native mode

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J2 Pin	Class	Schematic Net Name	Processor Pin	Signal Options
C1	IO	SDC1-DATA7	J3	Secure digital controller 1 data bit 7
C2	P	3V-RTC	-	3V rechargeable lithium ion coin
C3	I	CSI4-LN3_P	W5	MIPI CSI 4 (D-PHY), differential lane 3 – positive MIPI CSI 4 (C-PHY), trio lane 2 – B
C4	I	CSI4-LN2_P	Y6	MIPI CSI 4 (D-PHY), differential lane 2 – positive MIPI CSI 4 (C-PHY), trio lane 1 – C
C5	IO	Q0-4-L0	P4	Configurable I/O QUP0 SE4, lane 0: UART_CTS QUP0 SE4, lane 0: I2C_SDA QUP0 SE4, lane 0: SPI_MISO QDSS trigger output 1 A
C6	I	CSI3-LN0_N	AD2	MIPI CSI 3 (D-PHY), differential lane 0 – negative MIPI CSI 3 (C-PHY), trio lane 0 – C
C7	I	CSI3-LN1_N	AE3	MIPI CSI 3 (D-PHY), differential lane 1 – negative MIPI CSI 3 (C-PHY), trio lane 1 – B
C8	IO	LQ-6-L3	E45	Configurable I/O QDSS trace data bit 15 B LPI GPIO 26 LPI_QUP0 SE6, lane 3: UART_RX Sync out GPIO_15
C9	I	CSI2-LN0_N	AK4	MIPI CSI 2 (D-PHY), differential lane 0 – negative MIPI CSI 2 (C-PHY), trio lane 0 – C
C10	I	CSI2-LN2_P	AL1	MIPI CSI 2 (D-PHY), differential lane 2 – positive MIPI CSI 2 (C-PHY), trio lane 1 – C
C11	IO	LQ-5-L1-L3	D46	Configurable I/O QDSS trace data bit 13 B LPI GPIO 24 LPI_QUP0 SE5, lane 1: I2C_SCL LPI_QUP0 SE5, lane 3: UART_RX Sync out GPIO_13
C12	I	CSI1-LN1_N	AN3	MIPI CSI 1 (D-PHY), differential lane 1 – negative MIPI CSI 1 (C-PHY), trio lane 1 – B
C13	I	CSI1-LN2_N	AR3	MIPI CSI 1 (D-PHY), differential lane 2 – negative MIPI CSI 1 (C-PHY), trio lane 2 – A
C14	IO	GPIO122-B2	BP4	Configurable I/O Boot configuration control bit 2
C15	I	CSI0-LN1_N	AU3	MIPI CSI 0 (D-PHY), differential lane 1 – negative MIPI CSI 0 (C-PHY), trio lane 1 – B
C16	I	CSI0-LN1_P	AU1	MIPI CSI 0 (D-PHY), differential lane 1 – positive MIPI CSI 0 (C-PHY), trio lane 1 – A
C17	I	CSI0-LN0_P	AV6	MIPI CSI 0 (D-PHY), differential lane 0 – positive MIPI CSI 0 (C-PHY), trio lane 0 – B
C18	I	CSI0-LN0_N	AV4	MIPI CSI 0 (D-PHY), differential lane 0 – negative MIPI CSI 0 (C-PHY), trio lane 0 – C
C19	P	VBUS-CHRG	-	USB0 VBUS
C20	P	VBUS-CHRG	-	USB0 VBUS

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J2 Pin	Class	Schematic Net Name	Processor Pin	Signal Options
D1	IO	SDC1-DATA6	J1	Secure digital controller 1 data bit 6
D2	P	GND	-	-
D3	I	CSI4-LN3_N	W7	MIPI CSI 4 (D-PHY), differential lane 3 – negative MIPI CSI 4 (C-PHY), trio lane 2 – C
D4	I	CSI4-LN2_N	Y4	MIPI CSI 4 (D-PHY), differential lane 2 – negative MIPI CSI 4 (C-PHY), trio lane 2 – A
D5	P	GND	-	-
D6	I	CSI3-LN0_P	AC1	MIPI CSI 3 (D-PHY), differential lane 0 – positive MIPI CSI 3 (C-PHY), trio lane 0 – B
D7	I	CSI3-LN1_P	AE1	MIPI CSI 3 (D-PHY), differential lane 1 – positive MIPI CSI 3 (C-PHY), trio lane 1 – A
D8	P	GND	-	-
D9	I	CSI2-LN0_P	AK6	MIPI CSI 2 (D-PHY), differential lane 0 – positive MIPI CSI 2 (C-PHY), trio lane 0 – B
D10	I	CSI2-LN2_N	AL3	MIPI CSI 2 (D-PHY), differential lane 2 – negative MIPI CSI 2 (C-PHY), trio lane 2 – A
D11	P	GND	-	-
D12	I	CSI1-LN1_P	AN1	MIPI CSI 1 (D-PHY), differential lane 1 – positive MIPI CSI 1 (C-PHY), trio lane 1 – A
D13	I	CSI1-LN2_P	AR1	MIPI CSI 1 (D-PHY), differential lane 2 – positive MIPI CSI 1 (C-PHY), trio lane 1 – C
D14	IO	GPIO120-B1	BL5	Configurable I/O Boot configuration control bit 1
D15	I	CSI0-LN2_P	AW1	MIPI CSI 0 (D-PHY), differential lane 2 – positive MIPI CSI 0 (C-PHY), trio lane 1 – C
D16	I	CSI0-LN2_N	AW3	MIPI CSI 0 (D-PHY), differential lane 2 – negative MIPI CSI 0 (C-PHY), trio lane 2 – A
D17	I	CSI0-LN3_P	AW5	MIPI CSI 0 (D-PHY), differential lane 3 – positive MIPI CSI 0 (C-PHY), trio lane 2 – B
D18	I	CSI0-LN3_N	AW7	MIPI CSI 0 (D-PHY), differential lane 3 – negative MIPI CSI 0 (C-PHY), trio lane 2 – C
D19	P	VBUS-CHRG	-	USB0 VBUS
D20	P	VBUS-CHRG	-	USB0 VBUS

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J2 Pin	Class	Schematic Net Name	Processor Pin	Signal Options
E1	IO	SDC1-DATA1	H2	Secure digital controller 1 data bit 1
E2	IO	Q0-3-L2-B12	L3	Configurable I/O QUP0 SE3, lane 2: UART_TX QUP0 SE3, lane 2: SPI_SCLK Boot configuration control bit 12
E3	P	1V8-L19B	-	1.8V output for digital GNSS expansion
E4	P	0V88-L15B	-	0.875V output for digital GNSS expansion
E5	IO	Q0-4-L2	N1	Configurable I/O QUP0 SE4, lane 2: UART_TX QUP0 SE4, lane 2: SPI_SCLK QDSS trigger input 1 A
E6	P	1V2-L14B	-	1.2V output for analog GNSS expansion
E7	P	0V8-L13B	-	0.8V output for digital GNSS expansion
E8	IO	LQ-0-L0	F46	Configurable I/O LPI GPIO 15 LPI_QUP0 SE0, lane 0: I2C_SDA LPI_QUP0 SE0, lane 0: I3C_SDA Sync out GPIO_0
E9	P	0V8-L12B	-	0.8V output for analog GNSS expansion
E10	P	1V776-L11B	-	1.776V output for analog GNSS expansion
E11	IO	CSI-I2C0-SDA	BC3	Configurable I/O Dedicated camera control interface I^2C serial data
E12	P	GND	-	-
E13	P	GND	-	-
E14	IO	QL0-RST-B14	BR15	Configurable I/O QLINK0 SDR subsystem reset output Boot configuration control bit 14
E15	P	GND	-	-
E16	P	GND	-	-
E17	IO	QL0-REQ	BP12	Configurable I/O QLink0 request
E18	IO	QL0-EN	BN15	Configurable I/O QLink0 enable
E19	P	GND	-	-
E20	P	VBUS-CHRG	-	USB0 VBUS

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J2 Pin	Class	Schematic Net Name	Processor Pin	Signal Options
F1	IO	SDC1-DATA4	F2	Secure digital controller 1 data bit 4
F2	P	GND	-	-
F3	O	CSI4-CLK_P	AC7	MIPI CSI 4 (D-PHY), differential clock – positive MIPI CSI 4 (C-PHY), no connect
F4	O	CSI4-CLK_N	AC5	MIPI CSI 4 (D-PHY), differential clock – negative MIPI CSI 4 (C-PHY), trio lane 0 – A
F5	P	GND	-	-
F6	O	CSI3-CLK_N	AC3	MIPI CSI 3 (D-PHY), differential clock – negative MIPI CSI 3 (C-PHY), trio lane 0 – A
F7	O	CSI3-CLK_P	AB2	MIPI CSI 3 (D-PHY), differential clock – positive MIPI CSI 3 (C-PHY), no connect
F8	P	GND	-	-
F9	O	CSI2-CLK_P	AJ7	MIPI CSI 2 (C-PHY), no connect MIPI CSI 2 (D-PHY), differential clock – positive
F10	O	CSI2-CLK_N	AJ5	MIPI CSI 2 (D-PHY), differential clock – negative MIPI CSI 2 (C-PHY), trio lane 0 – A
F11	P	GND	-	-
F12	O	CSI0-CLK_P	AU7	MIPI CSI 0 (D-PHY), differential clock – positive MIPI CSI 0 (C-PHY), no connect
F13	O	CSI0-CLK_N	AU5	MIPI CSI 0 (D-PHY), differential clock – negative MIPI CSI 0 (C-PHY), trio lane 0 – A
F14	IO	PCIE0-RESn	BN9	Configurable I/O
F15	I	QLINK-L0_N	BJ13	QLink0 lane 0 – negative
F16	I	QLINK-L0_P	BL13	QLink0 lane 0 – positive
F17	P	GND	-	-
F18	P	GND	-	-
F19	I	QLINK-L1_P	BK16	QLink0 lane 1 – positive
F20	I	QLINK-L1_N	BH16	QLink0 lane 1 – negative

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J2 Pin	Class	Schematic Net Name	Processor Pin	Signal Options
G1	IO	SDC1-DATA5	E1	Secure digital controller 1 data bit 5
G2	IO	Q0-3-L1	M4	Configurable I/O QUP0 SE3, lane 1: UART_RFR QUP0 SE3, lane 1: I2C_SCL QUP0 SE3, lane 1: SPI_MOSI QDSS trace clock A
G3	P	GND	-	-
G4	P	GND	-	-
G5	IO	Q0-3-L3-B9	L1	Configurable I/O QUP0 SE3, lane 3: UART_RX QUP0 SE3, lane 3: SPI_CS_0 QDSS trigger output 0 A Boot configuration control bit 9
G6	IO	SD-DETECT	K4	Configurable I/O
G7	IO	Q0-0-L1	AF6	Configurable I/O QUP 0 SE0, lane 1: UART_RFR QUP 0 SE0, lane 1: I2C_SCL QUP 0 SE0, lane 1: SPI_MOSI QUP 0 SE0, lane 1: I3C_SCL
G8	IO	CSI-I2C1-SDA	BB4	Configurable I/O Dedicated camera control interface I^2C 1 serial data
G9	IO	PCIE1-RESn	AE5	Configurable I/O QUP 0 SE0, lane 2: UART_TX QUP 0 SE0, lane 2: SPI_SCLK QUP 0 SE7, lane 4: SPI_CS_1 QDSS trace data bit 0 A
G10	IO	PCIE1-WAKEn	AE7	Configurable I/O QUP0 SE0, lane 3: UART_RX QUP0 SE0, lane 3: SPI_CS_0 QUP0 SE7, lane 5: SPI_CS_2 QDSS trace data bit 1 A
G11	IO	CSI-I2C0-SCL	BB2	Configurable I/O Dedicated camera control interface I^2C clock
G12	P	GND	-	-
G13	P	GND	-	-
G14	IO	PCIE0-WAKEn	BJ9	Configurable I/O
G15	P	GND	-	-
G16	P	GND	-	-
G17	I	QLINK-L3_N	BL15	QLink0 lane 3 – negative
G18	I	QLINK-L3_P	BJ15	QLink0 lane 3 – positive
G19	P	GND	-	-
G20	P	GND	-	-

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J2 Pin	Class	Schematic Net Name	Processor Pin	Signal Options
H1	IO	SDC1-DATA0	D2	Secure digital controller 1 data bit 0
H2	P	GND	-	-
H3	I	PCIE0-RX_N	U3	PCIe 0 Gen 3 receive – negative
H4	I	PCIE0-RX_P	U1	PCIe 0 Gen 3 receive – positive
H5	P	GND	-	-
H6	P	GND	-	-
H7	IO	Q0-0-L0	AG7	Configurable I/O QUP 0 SE0, lane 0: UART_CTS QUP 0 SE0, lane 0: I2C_SDA QUP 0 SE0, lane 0: SPI_MISO QUP 0 SE0, lane 0: I3C_SDA
H8	P	GND	-	-
H9	IO	CSI-I2C1-SCL	BB6	Configurable I/O Dedicated camera control interface I^2C 1 clock
H10	P	GND	-	-
H11	P	GND	-	-
H12	O	CSI1-CLK_N	AN5	MIPI CSI 1 (D-PHY), differential clock – negative MIPI CSI 1 (C-PHY), trio lane 0 – A
H13	O	CSI1-CLK_P	AN7	MIPI CSI 1 (D-PHY), differential clock – positive MIPI CSI 1 (C-PHY), no connect
H14	P	GND	-	-
H15	O	QLINK-CLK_N	BK12	QLink0 clock – negative
H16	O	QLINK-CLK_P	BM12	QLink0 clock – positive
H17	P	GND	-	-
H18	P	GND	-	-
H19	P	3V7-BAT	-	3.7V lithium-ion battery input
H20	P	3V7-BAT	-	3.7V lithium-ion battery input

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J2 Pin	Class	Schematic Net Name	Processor Pin	Signal Options
I1	IO	SDC1-DATA3	C3	Secure digital controller 1 data bit 3
I2	IO	Q0-4-L1	W45	Configurable I/O Low-power audio SLIMbus clock
I3	P	GND	-	-
I4	P	GND	-	-
I5	O	PCIE0-TX_P	V4	PCIe 0 Gen 3 transmit – positive
I6	O	PCIE0-TX_N	V2	PCIe 0 Gen 3 transmit – negative
I7	P	GND	-	-
I8	IO	CSI-MCLK3	W1	Configurable I/O Camera master clock 3
I9	P	GND	-	-
I10	IO	CSI-MCLK1	Y2	Configurable I/O Camera master clock 1
I11	P	GND	-	-
I12	IO	GNSS-L1-EN	BJ3	Configurable I/O eLNA enable for L1 QUP0 SE2, lane 2: UART_TX QUP0 SE2, lane 2: SPI_SCLK QDSS trace data bit 4 A
I13	IO	GNSS-L25-EN	BJ1	Configurable I/O eLNA enable for L2_L5 QUP0 SE2, lane 3: UART_RX QUP0 SE2, lane 3: SPI_CS_0 QDSS trace data bit 5 A
I14	IO	RFFE4-CLK	BL7	Configurable I/O
I15	P	GND	-	-
I16	P	GND	-	-
I17	I	QLINK-L2_N	BH14	QLink0 lane 2 – negative
I18	I	QLINK-L2_P	BK14	QLink0 lane 2 – positive
I19	P	GND	-	-
I20	P	3V7-BAT	-	3.7V lithium-ion battery input

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J2 Pin	Class	Schematic Net Name	Processor Pin	Signal Options
J1	IO	SDC1-DATA2	E3	Secure digital controller 1 data bit 2
J2	P	GND	-	-
J3	O	PCIE0-REFCLK_P	R3	PCIe 0 Gen 3 reference clock – positive
J4	O	PCIE0-REFCLK_N	T2	PCIe 0 Gen 3 reference clock – negative
J5	P	GND	-	-
J6	P	GND	-	-
J7	IO	CSI-MCLK4	P2	Configurable I/O Camera master clock 4
J8	P	GND	-	-
J9	IO	CSI-MCLK2	AA3	Configurable I/O Camera master clock 2
J10	P	GND	-	-
J11	IO	CSI-MCLK0	AA1	Configurable I/O Camera master clock 0
J12	P	GND	-	-
J13	IO	RFFE4-DAT-B4	BJ7	Configurable I/O Boot configuration control bit 4
J14	P	GND	-	-
J15	I	QLINK-L4_P	BJ11	QLink0 lane 4 – positive
J16	I	QLINK-L4_N	BL11	QLink0 lane 4 – negative
J17	P	GND	-	-
J18	P	1V8-L18B	-	1.8V output for bootstrapping
J19	P	3V7-BAT	-	3.7V lithium-ion battery input
J20	P	3V7-BAT	-	3.7V lithium-ion battery input

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ELECTRICAL CHARACTERISTICS

Table 7: Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VBUS-CHRG	USB PD supply		3.7	-	12.6	V
VBATT-PWR	+3.8V Battery supply		2.7	3.8	4.8	V
$I_{5.0}$	Quiescent Current draw	5.0 volt input, 3200 MHz LPDDR5, Linux prompt	TBD	TBS	TBS	mA
$I_{5.0\text{-}max}$	Max current draw	5.0 volt input		TBS	9	A
	1. Power utilization of the MitySOM-QC is heavily dependent on end-user application. Major factors include: CPU Utilization, and external LPDDR5 RAM utilization. See section Power Interfaces for more info.					

ORDERING INFORMATION

The following table lists the standard module configurations. For availability, price, and minimum order quantity of these configurations, or to inquire about a development kit for these products, contact Critical Link via email at info@criticallink.com.

Table 8: Standard Model Numbers

Model / Part Number	CPU Speed Grade	HPS RAM (32-bit)	On-board Flash	Component Temperature Ratings
6490-EX-4X8-RL	2.7GHz	8GB	256GB	-25ºC to 80º C
6490-EX-3X8-RC	2.7GHz	8GB	128GB	0ºC to 70º C
5430-AX-2X4-RC	2.1GHz	4GB	64GB	0ºC to 70º C

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MitySOM-QC Module Family Model Number Guide

If a module suitable for your specific application is not found in Figure 3 please reference the following MitySOM-QC model number decoder for configuring a custom module. Please contact your Critical Link representative to determine pricing, lead-time and availability of a custom module.

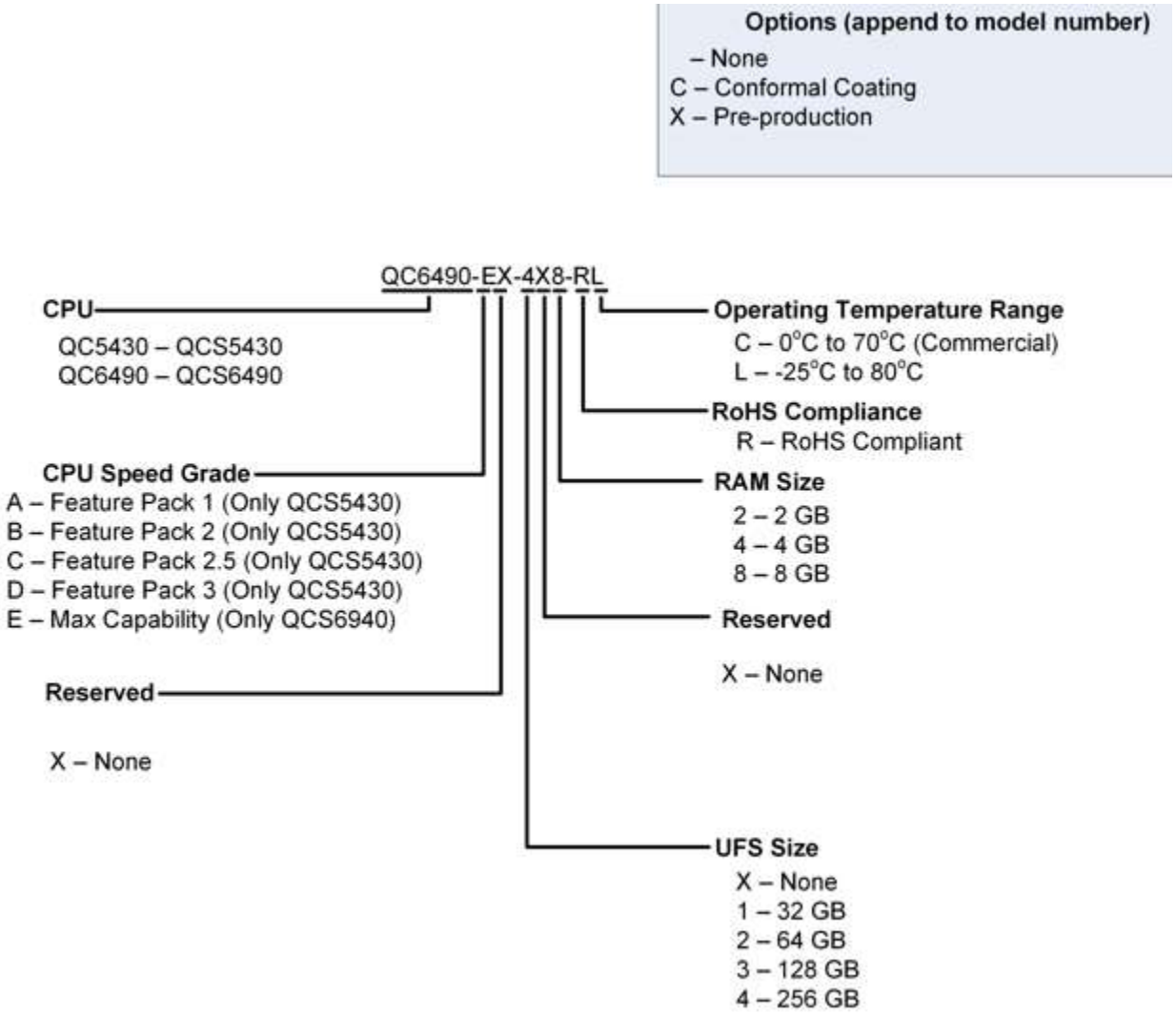

Figure 3: MitySOM-QC6490/5430 Model Number Decoder

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MECHANICAL INTERFACE

A bottom view mechanical outline of the MitySOM-QC is illustrated in Figure 4, below. All dimensions are in mm. The alignment holes for the board to board interfaces are shown.

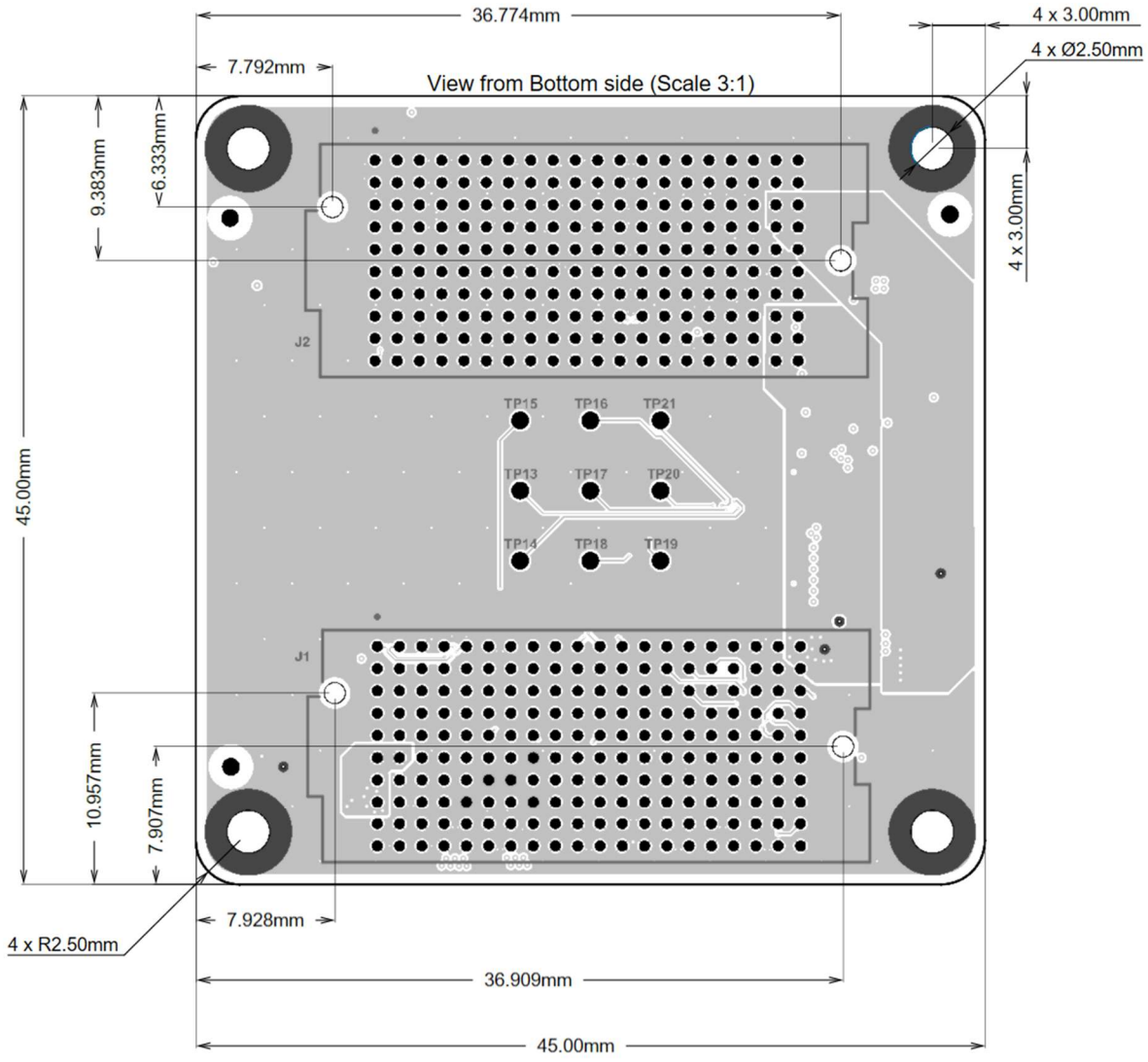

Figure 4: MitySOM-QC Mechanical Outline, View From Bottom

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REVISION HISTORY

Revision	Date	Change Description
1A	November 12, 2024	Preliminary Release for early adopters
1B	December 20, 2024	Update Standard Model Numbers and Model Number Decorder

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