FEATURES

MitySOM-QC6490/5430 Development Board

MitySOM-QC6490/5430 System on Module

Additional Hardware Included

- USB Cable
- AC to DC 12V 3A Adapter

Integrated +1.8V/+3.3V/+5V Power Supplies

Digital Interfaces

- Display Port Video Only Interface supporting FHD+ @ 144Hz
- Audio Output and Microphone Input
- Micro-USB port UART Console
- Dual USB 2.0 Host Ports
- USB Type-C with DP Dual Role Interface
- Up to 64GB eMMC
- Micro-SD/MMC Card Socket
- 5x 22-pin 4-lane MIPI camera interface port

Expansion Connectors

- M.2 E-key interface for Silex SX-PCEAX-M2 Wi-Fi 6E and BT Module
- MIPI DSI LCD Output Adapter
- 2-channel PCI Express Gen 3 slot
- Qualcomm GPS header
- 2x 34-Pin Expansion Headers

Software and Documentation

- Linux Kernel
- Embedded Linux Root Filesystem
- UEFI based boot loader
- Development Board Schematics
- Development Board Gerber Files
- Development Board BOM

Applications

- MitySOM-QC5430 Evaluation
- MitySOM-QC6490 Evaluation
- Process Automation
- Factory Automation
- Industrial Automation
- Mobile Applications
- Embedded Instrumentation
- Human Machine Interfaces
- Rich Displays
- Rapid Prototyping

DESCRIPTION

The MitySOM-QC6490/5430 Development Kit provides all the hardware and software support for system designers and developers to evaluate the Critical Link MitySOM-QC6490/5430 System on Module. The MitySOM-QC6490/5430 Development Kit comes complete with the MitySOM-QC6490/5430 module that meets your project's needs.

The MitySOM-QC6490/5430 Development Kit includes an on-board UART to Micro-USB Port, dual USB 2.0 Host Ports, one 3.1 USB Type-C with Display Port, one 1.4 Display Port connector, five MIPI camera interface ports, one 8-bit eMMC up to 64GB and one 3.5mm 4-conductor audio interface. The kit also includes an E-key M.2 connector that was designed to interface with a Silex SC-PCEAX-M2 WIFI/Bluetooth Module, a 2 channel PCI Express port as well as two 34-pin 0.1" header that provides several direct connections to the QCS6490/5430 processor supporting GPIO, SPI, I2C, SoundWire, I2S and Slimbus peripherals.

The kit supports Full High Definition Plus (FHD+) displays with resolutions up to 2220 × 1080 through a standard DisplayPort connector for video output. In addition, display functionality can be configured either through a single LCD interface utilizing MIPI DSI, accessible via an external connector, or through USB Type-C DisplayPort alternate mode. For audio, a standard stereo line-in, left channel and right channel 3.5mm / 1/8th jacks are provided. A standard Micro-SD card interface is available for MitySOM-QC6490/5430 general non-volatile data storage. The card is powered by a single 12V DC input and provides onboard +1.8V/+3.3V/+5V power supplies. Power for almost all ICs and interfaces on the development board can be powered from either the DC supply or via the battery pack to allow for maximum design flexibility.

A block diagram of the MitySOM-QC6490/5430 Development Kit is illustrated in Figure 1 on the following page. All available processor interface pins are used directly by the MitySOM-QC6490/5430 Development Kit. Control of the onboard interface hardware and connected Expansion IO cards require proper configuration of the MitySOM-QC6490/5430 Module. While not required, it is strongly recommended that the MitySOM-QC6490/5430 software development kit and supplied API be used to manage these interfaces.

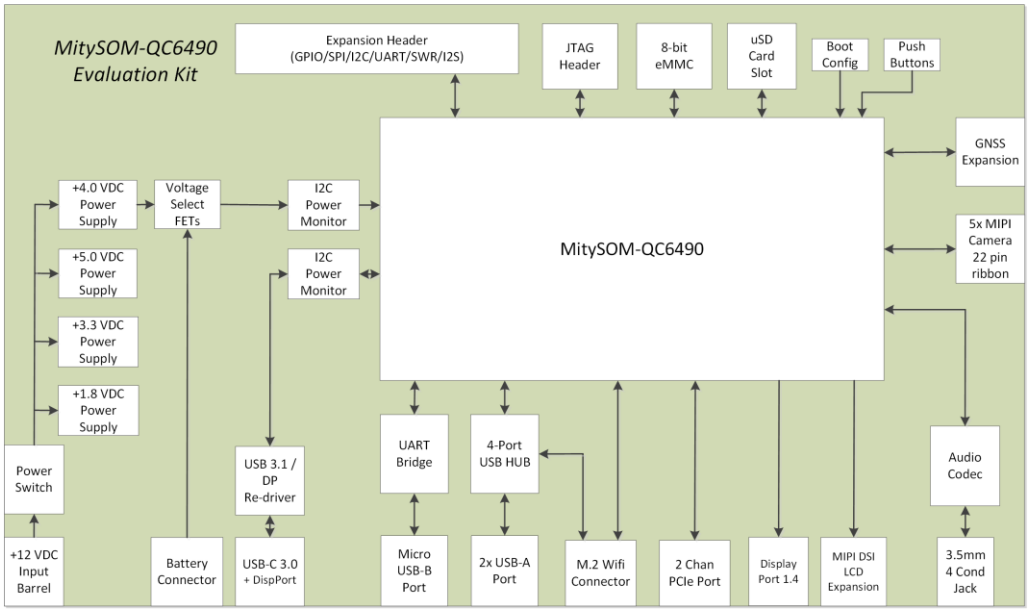


Figure 1: MitySOM-QC6490 Development Kit Block Diagram

Additional details about the QCS6490/5430, available peripherals, and their features are provided in the datasheet on the Qualcomm website:

https://docs.qualcomm.com/bundle/publicresource/topics/80-23889-1/device-description.html

Feature Descriptions

Electrical Interface Descriptions

USB Bridge Console Port

The MitySOM-QC6490/5430 development kit baseboard includes a FT230XS UART to USB bridge chip interfacing to DEBUG-UART.

Audio Input/Output Description

Standard 3.5mm / 1/8th inch audio jacks are provided for both stereo audio output and a microphone audio input from/to a SGTL5000XNLA3 low power stereo codec with headphone amp audio CODEC connected to the MitySOM-QC6490/5430 module.

The electrical interfaces are provided via 1/8th inch jack J8.

Linux Driver and API examples are available to support the audio functionality.

2-Port USB 2.0 Interface Description

A 2-port USB 2.0 Hub is connected to the USB1 interface of the QCS6490/5430 processor. The interface is through a dual USB-A stacked connector, J7, and the ports are configured to operate in host mode. Linux drivers are available.

3.1 USB Type-C Dual Role w/ Display Port Interface Description

The USB0 interface of the QCS6490/5430 processor is connected to a USB type-C port, J6. This port can operate in host or device mode, supports receiving USB power delivery (PD) for battery charging and supports USB 3.1 or Display Port over USB. Linux drivers are available.

µSD/MMC Card Interface Description

The onboard micro multimedia card (MMC) slot uses a micro secure digital (µSD) connector J4 and supports SD Standard v3.0 dual-voltage with 4-bits. It is compatible with standard (SD), SDHC (up to 32GB), and SDXC (Up to 2TB) cards. This interface is meant for extra storage and cannot be used as a boot media. Linux drivers are available.

eMMC Interface Description

The onboard embedded multimedia card (eMMC) U3 supports eMMC Standard v5.1 with 8-bits. Linux drivers are available.

MIPI Camera Interface Description

The MitySOM-QC6490/5430 Development Kit provides five 22-position flat flex cable interfaces to the QCS6490/5430 Camera Subsystem interface, a MIPI CSI v1.2 compliant device supporting up to 4 Data Lanes at up to 2.5 Gbps per lane.

GPS Interface Description

The MitySOM-QC6490-5430 Development Kit provides a 40-pin high-speed board-to-board expansion connector that connects the available QLINK interface, applicable voltage rails and necessary control signals from the QCS6490/5430 processor to support powering and reading from a Qualcomm SDR735 multiband GNSS receiver.

LCD with I2C Touch Interface Description

The MitySOM-QC6490/5430 Development Kit provides a 30-position high-speed board-to-board expansion connector that connects the available DSI v1.2 interface (4 pairs of data lanes, 1 clock lane) from the QCS6490/5430 processor to support controlling one LCD display. The interface also provides a connection to I2C1 to support communication with touch screens, a PWM signal to support backlight dimming and two IO signals.

Display Port (Video Only) Interface Description

The MitySOM-QC6490/5430 Development Kit provides a standard DP interface for external monitor connection. The maximum resolution supported by the display circuit is 7680 x 4320 at up to 60 Hz, 10-bit chroma.

Expansion Port Interface Description

The two 36-pin headers can be used for a multitude of expansion functions. GPIO, LPGPIO (Lower Power Island GPIO, LQUPS), SPI, I2C, SoundWire, I2S, Slimbus, PWM, clocks, and signals for parallel charging connections are available. Both 1.8V and 3.3V from either the MitySOM-QC6490/5430 module or the DC converters are available on the connector.

Boot Configuration Header Description

The MitySOM-QC6490/5430 Development Kit provides 1 6-position dip-switch (SW1) that is used to configure the BootMode (BM) settings of bits [0] to [3] of the QCS6490/5430 processor to determine the search order of peripherals/boot media to be used for a valid boot image.

By default, the MitySOM-QC6490/5430 Development Kit is configured to boot from the on board UFS.

Qualcomm JTAG Interface Description

A 10-pin 0.05” pitch header, J3, is available onboard for debugging the MitySOM QC6490/5430 module with a compatible JTAG Emulator.

WiFi/Bluetooth Expansion Interface Description

The WiFi/Bluetooth expansion interface, J16, is designed to be directly compatible with the Silex SX-PCEAX-M2 WiFi and Bluetooth expansion card. Linux drivers are available for the expansion card.

This interface can also be used for a user-designed interface card and features a 1-channel PCIe interface, a USB 2.0 interface and a +3.3V supply.

MitySOM-QC6490/5430 Current/Power Monitors

Two power/current monitors, U32 and U33, are installed in line with the VBUS-CHRG and 3V7-BAT power lines to the MitySOM-QC6490/5430 module. Additionally, these devices have a single-channel ADC that can monitor the +1.8V and the +3.3V power supply voltage on the Development Board. It is accessible over the I2C2 interface to the QCS6490/5430 processor.

Control Pushbuttons

Debounced normally open, contact to ground, momentary pushbuttons are included to signal the PMIC power button (S2), volume up (S3), and volume down (S4).

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Maximum Supply Voltage	13.2 V
Storage Temperature Range	0 to 80C

OPERATING CONDITIONS

Ambient Temperature Range	-20 to 85C
Humidity	0 to 95% Non-condensing

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Typical	Limit	Units (Limits)
Maximum Power Supply Output					
I_{Max}	12V Supply (AC Adapter)[1] all components			8.0	A
I_{Max}	12V Supply[2] for external components			2.0	A
I_{Max}	3.3V Supply[2] for external components			1.25	A
I_{Max}	1.8V Supply[2] for external components			0.9	A
Power Dissipation					
V_S	Supply Voltage		12±5%		V
I_S	Supply Current[3]		TBD		mA

Notes:

1. An alternative higher amperage AC/DC 12V adapter is available upon request. Contact Critical Link for details and ordering information.
2. The maximum current supplied to external components should be limited to the specified maximum for both the 12V, 3.3V and 1.8V supplies.
3. Expansion cards not attached, 100% QCS6490/5430 utilization, USB is enabled and active.

ELECTRICAL INTERFACE DESCRIPTIONS

Input Power – P1

The MitySOM-QC6490/5430 Development Kit power interface, P1, requires a single +12Volt power supply. P1 uses a Würth Elektronik 694106301002 2.1/5.5 mm inner/outer diameter jack. Slide switch S13 is included to support turning on and off the main power input such that the unit may be powered off without disconnecting P1. The MitySOM-QC6490/5430 Development Kit provides reverse polarity protection on P1.

Table 1: P1 Input Power Interface Pin Description

Signal	P1 Position
+12V	1
GND	2

MultiMedia Card (µSD) Interface – J2

The MitySOM-QC6490/5430 Development Kit provides a MMC interface that uses a standard Micro–Secure Digital (µSD) card slot for the physical interface. By default, the slot is supplied with 3.3V for use with standard SD cards and the IO voltages can be lowered to 1.8V by the QC6490/5430 SOM during runtime to support higher data rates provided by SDHC cards.

Table 2: J4 Micro SD Card Connector

J4 Pin	J4 Signal	SOM Interface Signal	SOM Pin
1	DAT2	SDC2-DATA2	J1-A14
2	CD/DAT3	SDC2-DATA3	J1-A13
3	CMD	SDC2-CMD	J1-A17
4	VDD	+3.3V	J1-A12
5	CLK	SDC2-CLK	J1-A19
6	VSS	GND	N/A
7	DAT0	SDC2-DATA0	J1-A16
8	DAT1	SDC2-DATA1	J1-A15
9	Switch (B)	GND	N/A
10	Switch(A)	DETECT	J2-G6

3.1 USB-C w/ DP Connector – J6

The MitySOM-QC6490/5430 Development Board features a USB-C DP re-driver, PI2DPX1217XUAEX – U7, which is connected to the USB0 interface from the QCS6490/5430 processor. The USB-C connector supports four operation modes: USB3.1 Gen1, USB3.1 Gen1/2-lane DP1.4 or 4-lane DP1.4 via I2C configuration.

The USB-C port supports OTG operation as well as USB Power Delivery (PD) 3.0 for battery charging. The pinout for J6 is included in Table 4.

Table 3: J6 USB-C Connector Pin Out

J6 Pin	J6 Signal	Type
A1	GND	Power
A2	CON-TX1_P	O
A3	CON-TX1_N	O
A4	USB0-VBUS	Power
A5	USB0-CC1	I/O
A6	USB0-HS_P	I/O
A7	USB0-HS_N	I/O
A8	USB0-SBU1	I/O
A9	USB0-VBUS	Power
A10	CON-RX2_N	I
A11	CON-RX2_P	I
A12	GND	Power
B1	GND	Power
B2	CON-TX2_P	O
B3	CON-TX2_N	O
B4	USB0-VBUS	Power
B5	USB0-CC2	I/O
B6	USB0-HS_P	I/O
B7	USB0-HS_N	I/O
B8	USB0-SBU2	I/O
B9	USB0-VBUS	Power
B10	CON-RX1_N	I
B11	CON-RX1_P	I
B12	GND	Power
S1	USB-SHIELD	Power
S2	USB-SHIELD	Power
S3	USB-SHIELD	Power
S4	USB-SHIELD	Power

2 Port USB 2.0 Type-A – J7

The MitySOM-QC6490/5430 Development Board features a 4-port USB hub, TUSB4041IPAPR – U12, which is connected to the USB1 interface from the QCS6490/5430 processor. Two of the USB ports are exposed from the Development Board on a dual USB Type-A Host-only connector, J7, and another is connected to the M.2 expansion connector.

This interface is a USB 2.0 interface and supports up to 480Mbps throughput speeds and is backward compatible with Full-speed and Low-speed devices. Each port can supply a maximum of 0.5A of current at +5V and an overcurrent detection circuit is connected to each port individually. The pinout for both J7 ports are included in Table 4.

Table 4: J7 Dual USB Host Connector Pin Out

J7 Pin	J7 Signal	J7 Upper or Lower Port
1	VBUS3	Lower
2	USB-D3_N	
3	USB-D3_P	
4	GND	
5	VBUS2	Upper
6	USB-D2_N	
7	USB-D2_P	
8	GND	

Auxiliary LCD Interface – J15

The Auxiliary LCD interface connector provides the necessary connections to connect a display as well as pins to support touchscreen controls. The interface uses a Samtec ST4-15-1.00-L-D-P-TR board-to-board interface connector. Table 5 defines the connector, J15, pinout which contains signals that are routed from the MitySOM-QC6490/5430 to this connector.

Table 5: J15 Aux / LCD Interface Pin Description

J15 Pin	Schematic Signal	SOM Pin	Type	Standard	Notes
1	GND	-	Power	-	
2	GND	-	Power	-	
3	3V3-MIPI	-	Power	-	
4	1V8-MIPI	-	Power	-	
5	3V3-MIPI	-	Power	-	
6	12V-DC	-	Power	-	
7	GND	-	Power	-	
8	GND	-	Power	-	
9	DSI-IO1	-	I/O	-	I/O expander from I2C1
10	PWM0-3V3	J1-C8	I/O	-	
11	DSI-IO0	-	I/O	-	I/O expander from I2C1
12	DSI-IO2	-	I/O	-	I/O expander from I2C1
13	GND	-	Power	-	
14	GND	-	Power	-	
15	DSI0-CLK_N	J1-A1	O	LVDS	
16	I2C1-SCL-3V3	J1-E18	O	-	
17	DSI0-CLK_P	J1-A2	O	LVDS	
18	I2C1-SDA-3V3	J1-E17	O	-	
19	GND	-	Power	-	
20	GND	-	Power	-	
21	DSI0-LN2_N	J1-A8	O	LVDS	
22	DSI0-LN3_N	J1-A6	O	LVDS	
23	DSI0-LN2_P	J1-A9	O	LVDS	
24	DSI0-LN3_P	J1-A7	O	LVDS	
25	GND	-	Power	-	
26	GND	-	Power	-	
27	DSI0-LN0_N	J1-A10	O	LVDS	
28	DSI0-LN1_N	J1-A4	O	LVDS	
29	DSI0-LN0_P	J1-A11	O	LVDS	
30	DSI0-LN1_P	J1-A5	O	LVDS	

Note: Some of these signals are pin-muxed in the QCS6490/5430 CPU.

DP Interface – J14

The MitySOM-QC6490/5430 Development Kit provides a 20-pin standard DP connector with video only, J14. Supporting DP 1.4, the MitySOM-QC6490/5430 can output up to a resolution of 7680 x 4320 pixels.

Table 6: J14 Connector Pin Assignments

J14 Pin	Signal	Type	Standard	Notes
1	DP-TX0_P	O	DSI	
2	GND	Power		
3	DP-TX0_N	O	DSI	
4	DP-TX1_P	O	DSI	
5	GND	Power		
6	DP-TX1_N	O	DSI	
7	DP-TX2_P	O	DSI	
8	GND	Power		
9	DP-TX2_N	O	DSI	
10	DP-TX3_P	O	DSI	
11	GND	Power		
12	DP-TX3_N	O	DSI	
13	Reserved	-		
14	Reserved	-		
15	DP-AUX_P	I/O		
16	GND	Power		
17	DP-AUX_N	I/O		
18	DP-HPD-3V3	I		
19	GND	Power		
20	3V3-DP	Power		

Camera MIPI Interfaces – J9-J13

The MitySOM-QC6490/5430 Development Kit provides five 22-pin 0.5 mm pitch flat flex connector, J9-J13, to interface with the camera subsystem of the QCS6490/5430 processor.

Table 7: J9 Connector Pin Assignments

J9 Pin	Signal	Type	Standard	Notes
1	GND	-	-	
2	CSI0-LN0_N	I	CSI	
3	CSI0-LN0_P	I	CSI	
4	GND	-	-	
5	CSI0-LN1_N	I	CSI	
6	CSI0-LN1_P	I	CSI	
7	GND	-	-	
8	CSI0-CLK_N	I	CSI	
9	CSI0-CLK_P	I	CSI	
10	GND	-	-	
11	CSI0-LN2_N	I	CSI	
12	CSI0-LN2_P	I	CSI	
13	GND	-	-	
14	CSI0-LN3_N	I	CSI	
15	CSI0-LN3_P	I	CSI	
16	GND	-	-	
17	CSI0-MCLK	I	-	
18	CSI0-IO	I/O	-	
19	GND	-	-	
20	CSI0-SCL	I	-	
21	CSI0-SDA	I/O	-	
22	3V3-MIPI	Power	-	Max 500 mA

Table 8: J10 Connector Pin Assignments

J10 Pin	Signal	Type	Standard	Notes
1	GND	-	-	
2	CSI1-LN0_N	I	CSI	
3	CSI1-LN0_P	I	CSI	
4	GND	-	-	
5	CSI1-LN1_N	I	CSI	
6	CSI1-LN1_P	I	CSI	
7	GND	-	-	
8	CSI1-CLK_N	I	CSI	
9	CSI1-CLK_P	I	CSI	
10	GND	-	-	
11	CSI1-LN2_N	I	CSI	
12	CSI1-LN2_P	I	CSI	
13	GND	-	-	
14	CSI1-LN3_N	I	CSI	
15	CSI1-LN3_P	I	CSI	
16	GND	-	-	
17	CSI1-MCLK	I	-	
18	CSI1-IO	I/O	-	
19	GND	-	-	
20	CSI1-SCL	I	-	
21	CSI1-SDA	I/O	-	
22	3V3-MIPI	Power	-	Max 500 mA

Table 9: J11 Connector Pin Assignments

J11 Pin	Signal	Type	Standard	Notes
1	GND	-	-	
2	CSI2-LN0_N	I	CSI	
3	CSI2-LN0_P	I	CSI	
4	GND	-	-	
5	CSI2-LN1_N	I	CSI	
6	CSI2-LN1_P	I	CSI	
7	GND	-	-	
8	CSI2-CLK_N	I	CSI	
9	CSI2-CLK_P	I	CSI	
10	GND	-	-	
11	CSI2-LN2_N	I	CSI	
12	CSI2-LN2_P	I	CSI	
13	GND	-	-	
14	CSI2-LN3_N	I	CSI	
15	CSI2-LN3_P	I	CSI	
16	GND	-	-	
17	CSI2-MCLK	I	-	
18	CSI2-IO	I/O	-	
19	GND	-	-	
20	CSI2-SCL	I	-	
21	CSI2-SDA	I/O	-	
22	3V3-MIPI	Power	-	Max 500 mA

Table 10: J12 Connector Pin Assignments

J12 Pin	Signal	Type	Standard	Notes
1	GND	-	-	
2	CSI3-LN0_N	I	CSI	
3	CSI3-LN0_P	I	CSI	
4	GND	-	-	
5	CSI3-LN1_N	I	CSI	
6	CSI3-LN1_P	I	CSI	
7	GND	-	-	
8	CSI3-CLK_N	I	CSI	
9	CSI3-CLK_P	I	CSI	
10	GND	-	-	
11	CSI3-LN2_N	I	CSI	
12	CSI3-LN2_P	I	CSI	
13	GND	-	-	
14	CSI3-LN3_N	I	CSI	
15	CSI3-LN3_P	I	CSI	
16	GND	-	-	
17	CSI3-MCLK	I	-	
18	CSI3-IO	I/O	-	
19	GND	-	-	
20	**CSI3-SCL**	I	-	
21	**CSI3-SDA**	I/O	-	
22	3V3-MIPI	Power	-	Max 500 mA

Table 11: J13 Connector Pin Assignments

J13 Pin	Signal	Type	Standard	Notes
1	GND	-	-	
2	CSI4-LN0_N	I	CSI	
3	CSI4-LN0_P	I	CSI	
4	GND	-	-	
5	CSI4-LN1_N	I	CSI	
6	CSI4-LN1_P	I	CSI	
7	GND	-	-	
8	CSI4-CLK_N	I	CSI	
9	CSI4-CLK_P	I	CSI	
10	GND	-	-	
11	CSI4-LN2_N	I	CSI	
12	CSI4-LN2_P	I	CSI	
13	GND	-	-	
14	CSI4-LN3_N	I	CSI	
15	CSI4-LN3_P	I	CSI	
16	GND	-	-	
17	CSI4-MCLK	I	-	
18	CSI4-IO	I/O	-	
19	GND	-	-	
20	**CSI3-SCL**	I	-	
21	**CSI3-SDA**	I/O	-	
22	3V3-MIPI	Power	-	Max 500 mA

GPS Expansion Port – J18

The GPS expansion port provides the necessary connections required to support the multiband GNSS receiver Qualcomm SDR735. This includes power, control and differential data signals. This connector is a Samtec ERF8-020-05.0-L-DV-TR high-speed board- to-board connector. Table 5 defines the connector, J18, pinout which contains signals that are routed from the MitySOM-QC6490/5430 to this connector.

Table 12: J18 GPS Expansion Port Pin Description

Pin	Schematic Signal	SOM Pin	Type	Standard	Notes
1	GND	-	Power	-	
2	38M4-76M8-CLK0	-	O	-	
3	QLINK-CLK_P	BM12	O	LVDS	
4	GND	-	Power	-	
5	QLINK-CLK_N	BK12	O	LVDS	
6	GND	-	Power	-	
7	GND	-	Power	-	
8	QLINK-L0_N	BJ13	I/O	LVDS	
9	GND	-	Power	-	
10	QLINK-L0_P	BL13	I/O	LVDS	
11	QLINK-L1_N	BH16	I/O	LVDS	
12	GND	-	Power	-	
13	QLINK-L1_P	BK16	I/O	LVDS	
14	GND	-	Power	-	
15	GND	-	Power	-	
16	QLINK-L2_P	BK14	I/O	LVDS	
17	GND	-	Power	-	
18	QLINK-L2_N	BH14	I/O	LVDS	
19	QLINK-L3_P	BJ15	I/O	LVDS	
20	GND	-	Power	-	
21	QLINK-L3_N	BL15	I/O	LVDS	
22	GND	-	Power	-	
23	GND	-	Power	-	
24	QLINK-L4_P	BJ11	I/O	LVDS	
25	GND	-	Power	-	
26	QLINK-L4_N	BL11	I/O	LVDS	
27	1V8-DGNSS	-	Power	-	Max 500 mA
28	GND	-	Power	-	
29	0V875-DGNSS	-	Power	-	Max 500 mA
30	0V8-AGNSS	-	Power	-	Max 1 A
31	1V2-AGNSS	-	Power	-	Max 1 A
32	1V7-AGNSS	-	Power	-	Max 500 mA
33	0V8-DGNSS	-	Power	-	Max 1 A
34	GNSS-L1-EN	BJ3	O	LVCMOS 1.8V	
35	QL0-REQ	BP12	I	LVCMOS 1.8V	
36	GNSS-L25-EN	BJ1	O	LVCMOS 1.8V	
37	QL0-EN	BN15	O	LVCMOS 1.8V	
38	RFFE4-CLK	BP6	O	-	
39	QL0-RST-B14	BR15	O	LVCMOS 1.8V	Boot Mode pins must be high impedance during power on / reset operations.
40	RFFE-DAT-B4	BM6	I/O	-	Boot Mode pins must be high impedance during power on / reset operations.

Expansion Port Interfaces – J21 and J22

The MitySOM-QC6490/54330 Development Kit provides two dual row 0.1” pitch 36-pin female general expansion connector on the bottom of the board. The connectors are Samtec’s SSM-118-L-DV connectors are used and mates with standard 0.1” dual row male headers.

This expansion interface can be used for many different add-on cards due to it having I2C, SPI, I2C, SoundWire, I2S and Slimbus signals directly from the MitySOM-QC6490/5430 module. There are additional signals to support parallel charging for the battery. A 1.8V and 3.3V supply pin is provided on the connector to support powering external cards. Table 13 and
Table 14 provides signal descriptions for each pin.

Table 13: J21 Connector Pin Assignments

Pin	Schematic Signal	SOM Pin	Type	Standard	Notes
1	3V7-BAT	-	Power	-	
2	VBUS-CHRG	-	Power	-	
3	3V7-BAT	-	Power	-	
4	VBUS-CHRG	-	Power	-	
5	GND	-	Power	-	
6	GND	-	Power	-	
7	SMB-SPMI-DAT	J1-B13	I/O	LVCMOS 1.8V	
8	1V8-EXP	-	Power	-	
9	SMB-SPMI-CLK	J1-B12		LVCMOS 1.8V	
10	3V3-EXP	-	Power	-	
11	GND	-	Power	-	
12	GND	-	Power	-	
13	SMB-EN	J1-B20	O	LVCMOS 1.8V	
14	GND	-	Power	-	
15	SMB-STAT	J1-C15	I/O	LVCMOS 1.8V	
16	Q0-0-L0	J2-H7	I/O	LVCMOS 1.8V	
17	SMB-THERM	J1-B15	AI	-	
18	GPIO-43-DP-HPD	J1-F19	I/O	LVCMOS 1.8V	
19	SMB-ISNS	J1-B18	AI	-	
20	GPIO-128-B10	J2-B19	I/O	LVCMOS 1.8V	Boot Mode pins must be high impedance during power on / reset operations.
21	SMB-OVP-DRV	-	I	-	
22	LQ-2-L0	J1-C2	I/O	LVCMOS 1.8V	
23	SMB-OVP-SNS	-	O	-	
24	LQ-2-L1	J1-C3	I/O	LVCMOS 1.8V	
25	GND	-	Power	-	
26	LQ-2-L2	J1-B3	I/O	LVCMOS 1.8V	
27	PWM1	J1-B10	O	LVCMOS 1.8V	
28	LQ-2-L3	J1-C4	I/O	LVCMOS 1.8V	
29	Q0-4-L0	J2-C5	I/O	LVCMOS 1.8V	
30	LQ-5-L0-L2	J2-A8	I/O	LVCMOS 1.8V	
31	Q1-3-L2	J1-C7	I/O	LVCMOS 1.8V	
32	LQ-5-L1-L3	J2-C11	I/O	LVCMOS 1.8V	
33	Q0-4-L2	J2-E5	I/O	LVCMOS 1.8V	
34	LQ-6-L2	J2-A11	I/O	LVCMOS 1.8V	
35	Q0-4-L3	J2-A5	I/O	LVCMOS 1.8V	
36	LQ-6-L3	J2-C8	I/O	LVCMOS 1.8V	

Table 14: J22 Connector Pin Assignments

Pin	Schematic Signal	SOM Pin	Type	Standard	Notes
1	3V3-EXP	-	Power	-	
2	1V8-EXP	-	Power	-	
3	3V3-EXP	-	Power	-	
4	1V8-EXP	-	Power	-	
5	19M2-CLK	J1-G20	Power	-	
6	GND	-	Power	-	
7	GND	-	Power	-	
8	SLIMBUS-CLK	J1-B7	Power	-	
9	Q1-1-L0	J1-E9	Power	-	
10	SLIMBUS-DAT	J1-B8	Power	-	
11	Q1-1-L1	J1-E8	O	LVCMOS 1.8V	
12	I2S1-WS	J1-B5	I/O	LVCMOS 1.8V	
13	Q1-1-L2-4-L6	J1-F6	I/O	LVCMOS 1.8V	
14	I2S1-D0	J1-C6	I/O	LVCMOS 1.8V	
15	Q1-1-L3	J1-E7	AI	-	
16	I2S1-CLK	J1-C5	I/O	LVCMOS 1.8V	
17	GND	-	Power	-	
18	I2S1-D1	J1-B6	I/O	LVCMOS 1.8V	Boot Mode pins must be high impedance during power on / reset operations.
19	38M4-76M8-CLK1	J1-I20		LVCMOS 1.8V	
20	GND	-	Power	-	
21	GND	-	Power	-	
22	SW0-TX-CLK	J1-D10	I/O	LVCMOS 1.8V	
23	GND	-	Power	-	
24	SW0-TX-D0	J1-D9	I/O	LVCMOS 1.8V	
25	LQ-0-L0	J2-E8	O	LVCMOS 1.8V	
26	SW0-TX-D1	J1-D8	I/O	LVCMOS 1.8V	
27	LQ-0-L1	J1-C1	I/O	LVCMOS 1.8V	
28	SW0-RX-CLK	J1-D7	I/O	LVCMOS 1.8V	
29	LQ-1-L0-2-L4	J1-B1	I/O	LVCMOS 1.8V	
30	SW0-RX-D0	J1-D9	I/O	LVCMOS 1.8V	
31	LQ-1-L1	J1-B2	I/O	LVCMOS 1.8V	
32	SW0-RX-D1	J1-D8	I/O	LVCMOS 1.8V	
33	Q1-5-L2-4-L5	J1-F7	I/O	LVCMOS 1.8V	
34	Q1-5-L3-4-L4	J1-E4	I/O	LVCMOS 1.8V	
35	GND	-	Power	-	
36	GND	-	Power	-	

Note that many of these signals are pin-muxed in the CPU and may be available for a variety of functions. Review the MitySOM-QC6490/5430 datasheet for additional information.

Wi-Fi and Bluetooth M.2 Connector – J16

The MitySOM-QC6490/5430 Development Kit provides an M.2 E-key connector for a Wi-fi/BT module, specifically the Silex SX-PCEAX-M2. This connection follows standard pin-out as shown in Table 15 below.

Table 15: J16 M.2 E-key connector

Pin	Signal	Type	Standard	Notes
1	GND	Power	-	
2	3V3-WIFI	Power	-	
3	USB-BT_P	I/O		
4	3V3-WIFI	Power	-	
5	USB-BT_N	I/O		
6	NC	-	-	
7	GND	Power	-	
8	NC	-	-	
9	NC	-	-	
10	NC	-	-	
11	NC	-	-	
12	NC	-	-	
13	NC	-	-	
14	NC	-	-	
15	NC	-	-	
16	NC	-	-	
17	NC	-	-	
18	GND	Power	-	
19	NC	-	-	
20	NC	-	-	
21	NC	-	-	
22	NC	-	-	
23	NC	-	-	
24-31	Notch	-	-	
32	NC	-	-	
33	GND	Power	-	
34	NC	-	-	
35	PCIE0-TX_P	O		
36	NC	-	-	
37	PCIE0-TX_N	O		
38	NC	-	-	
39	GND	Power	-	
40	NC	-	-	
41	PCIE0-RX_P	I		
42	NC	-	-	
43	PCIE0-RX_N	I		
44	NC	-	-	
45	GND	Power	-	
46	NC	-	-	
47	PCIE-REFCLK_P	O		
48	NC	-	-	
49	PCIE-REFCLK_N	O		
50	NC	-	-	
51	GND	Power	-	
52	PCIE0-RESn	O		
53	PCIE0-CLKREQn	I		
54	NC	-	-	
55	PCIE0-WAKEn	I		
56	NC	-	-	
57	GND	Power	-	

58	NC	-	-	
59	NC	-	-	
60	NC	-	-	
61	NC	-	-	
62	NC	-	-	
63	GND	Power	-	
64	NC	-	-	
65	NC	-	-	
66	NC	-	-	
67	NC	-	-	
68	NC	-	-	
69	GND	Power	-	
70	NC	-	-	
71	NC	-	-	
72	3V3-WIFI	Power	-	
73	NC	-	-	
74	3V3-WIFI	Power	-	
75	GND	Power	-	

Audio Input/Output Interface – J8 & J23

The MitySOM-QC6490/5430 Development Kit provides both a biased microphone and L/R stereo speaker connections. The 3.5mm/1/8” connections are through J8 with the pinouts shown in Table 16 as per the CTIA standard. Additionally, the left and right lines in as well as the left and right lines out are pinned out to a 5-pin header, J23, as shown in Table 17.

Table 16: J8 Audio Output Pin Assignments

Pin	Signal	Type	Standard	Notes
Tip	Audio Out Left	O		Unbalanced audio output
Inner Ring	Audio Out Right	O		Unbalanced audio output
Outer Ring	VGND	Power		Audio Ground
Sleeve	MIC	I		Audio input

Table 17: J23 Audio Output Pin Assignments

Pin	Signal	Type	Standard	Notes
Tip	Audio Out Left	O		Unbalanced audio output
Inner Ring	Audio Out Right	O		Unbalanced audio output
Outer Ring	VGND	Power		Audio Ground
Sleeve	MIC	I		Audio input

The SGTL5000XNLA3 Audio Codec is connected to the I2S0 interface on the QCS6490/5430 processor.

Boot Configuration Switches – S1

The boot mode, as determined by the 5 Boot Mode pins of the QCS6490/5430 processor. Using one 6-position dip switch, S1, each boot configuration pin on the SOM is connected to a weak pull-down (10kΩ), '0', unless a switch is turned on which will add a relatively strong pullup (1kΩ) to the configuration pin, '1'. Table 18 describes the switch connections to the Boot Mode pins. Table 19 describes the various boot sequences tied to the boot pins. Note that currently on booting from the UFS or the eMMC is supported.

Table 18: S1 Jumper Connections

Switch	Position	Default	Connection	Notes
S1	1	OFF	B0-IO118	On sets BOOT0 high, Off sets BOOT0 low.
S1	2	OFF	B1-IO120	On sets BOOT1 high, Off sets BOOT1 low.
S1	3	OFF	B2-IO122	On sets BOOT2 high, Off sets BOOT2 low.
S1	4	OFF	B3-IO124	On sets BOOT3 high, Off sets BOOT3 low.
S1	5	OFF	NC	
S1	6	OFF	BUSB-IO82	On sets FORCE-USB-BOOT high, Off sets FORCE-USB-BOOT low.

Table 19: S1 Boot Sequence

Boot Sequence	BOOT3	BOOT2	BOOT1	BOOT0
Watchdog Enabled	X	X	X	0
Watchdog Disabled	X	X	X	1
UFS, SDC2, EDL	0	0	0	X
eMMC, SDC2, EDL	0	0	1	X
SDC2, EDL	0	1	0	X
USB	0	1	1	X
UFS, EDL	1	1	0	X
eMMC, EDL	1	1	1	X

TI JTAG Interface – J3

The JTAG interface is meant to interface with the default JTAG pod, the Lauterbach Trace32 Micro Trace for Cortex-M. Table 20 lists the connections to the JTAG interface connector. Additionally, PS-HOLD, MODE-0 and MODE-1 should be pulled up to 1V8-BOOT for JTAG communication. See Table 30 for switch connections.

Table 20: J3 JTAG Pin Assignments

Pin	Schematic Signal	SOM Pin	Type	Standard	Notes
1	1V8-SOM	-	Power	-	
2	JTAG-TMS	J1-D12	O	LVCMOS 1.8	
3	GND	-	Power	-	
4	JTAG-TCK	J1-D15	O	LVCMOS 1.8	
5	GND	-	Power	-	
6	JTAG-TDO	J1-D13	O	LVCMOS 1.8	
7	GND	-	Power	-	
8	JTAG-TDI	J1-D14	O	LVCMOS 1.8	
9	GND	-	Power	-	
10	JTAG-TRSTn	J1-D11	O	LVCMOS 1.8	

PCI Express Slot – J17

The Gen 3.1 PCI Express slot is a 64-pin PCIe x4 slot. Two PCIe channels are supported on this slot. A connector is a Molex 0877159106 connector that interfaces with any PCIe x1 or x4 card. The pinout of this slot is described in Table 21. Note that the QC5430 Feature Pack 1 does not support the PCIE1 interface, all other variants of the MitySOM-QC6490/5430 do support the PCIE1 interface.

Table 21: J17 PCIe Slot Pin Assignments

Pin	Schematic Signal	SOM Pin	Type	Standard	Notes
A1	GND	-	Power	-	
A2	12V-DC	-	Power	-	
A3	12V-DC	-	Power	-	
A4	GND	-	Power	-	
A5	GND	-	Power	-	
A6	NC	-	-	-	
A7	NC	-	-	-	
A8	NC	-	-	-	
A9	3V3-PCIE	-	Power	-	
A10	3V3-PCIE	-	Power	-	
A11	PCIE1-RESn	J2-G9	O	LVCMOS 3.3V	
A12	GND	-	Power	-	
A13	PCIE1-REFCLK_P	J1-I13	O		
A14	PCIE1-REFCLK_N	J1-I12	O		
A15	GND	-	Power	-	
A16	PCIE1-RX0_P	J1-H3	I		
A17	PCIE1-RX0_N	J1-H3	I		
A18	GND	-	Power	-	
A19	NC	-	-	-	
A20	GND	-	Power	-	
A21	PCIE1-RX1_P	J1-G13	I		
A22	PCIE1-RX1_N	J1-G12	I		
A23	GND	-	Power	-	
A24	GND	-	Power	-	
A25	NC	-	-	-	
A26	NC	-	-	-	
A27	GND	-	Power	-	
A28	GND	-	Power	-	
A29	NC	-	-	-	
A30	NC	-	-	-	
A31	GND	-	Power	-	
A32	NC	-	-	-	
B1	12V-DC	-	Power	-	
B2	12V-DC	-	Power	-	
B3	12V-DC	-	Power	-	
B4	GND	-	Power	-	
B5	PCIE1-I2C-SCL	J2-B2	I/O		
B6	PCIE1-I2C-SDA	J2-B5	O		
B7	GND	-	Power	-	
B8	3V3-PCIE	-	Power	-	
B9	3V3-PCIE	-	Power	-	
B10	3V3-PCIE	-	Power	-	
B11	PCIE1-WAKEn	J2-G10	O	LVCMOS 3.3V	
B12	NC	-	-	-	
B13	GND	-	Power	-	
B14	PCIE1-TX0_P	J1-I9	O		
B15	PCIE1-TX0_N	J1-I8	O		
B16	GND	-	Power	-	

B17	PCIE1-X1-PRSNTn	J2-B8	I	LVCMOS 3.3V	
B18	GND	-	Power	-	
B19	PCIE1-TX1_P	J1-H6	O		
B20	PCIE1-TX1_N	J1-H7	O		
B21	GND	-	Power	-	
B22	GND	-	Power	-	
B23	NC	-	-	-	
B24	NC	-	-	-	
B25	GND	-	Power	-	
B26	GND	-	Power	-	
B27	NC	-	-	-	
B28	NC	-	-	-	
B29	GND	-	Power	-	
B30	NC	-	-	-	
B31	PCIE1-X4-PRSNTn	J2-B11	I	LVCMOS 3.3V	
B32	GND	-	Power	-	

USB Debug Interface – J5

The USB debug interface provides a stream of ASCII data used for communicating to and debugging the QC6490/5430 SOM. The DEBUG-UART interface is passed to a UART to USB bridge IC FT230XS-U (U5) to a micro-USB socket for connection to a host PC. The pinout of this slot is described in Table 22.

Table 22: J5 USB Debug Pin Assignments

Pin	Schematic Signal	SOM Pin	Type	Standard	Notes
1	CONS-VBUS	-	Power	-	
2	D_N	-	I/O	-	
3	D_P	-	I/O	-	
4	NC	-	-	-	
5	GND	-	Power	-	

RTC Coin Cell Receptacle – BH1

Battery holder BH1 is meant to hold a 6.8mm 3V coin cell for the RTC. Note that the SOM recharges the RTC line so a rechargeable lithium-ion coin cell is recommended.

Battery Connector – J20

The battery connector is meant to connect a 3.7V rechargeable lithium ion battery. The connector is a Samtec IPL1-105-01-L-D-K. This connector also acts as the switch between DC supply or battery operation with USBC charging. If no plug is installed in this receptacle, the SOM is supplied via a 4V DC voltage, and the respective pull-down resistances are supplied to BATT-THERM and BATT-ID. If a plug is installed in this connector, the SOM is supplied via the battery voltage and charged via the USBC plug. Note that the mating plug for the J20 connector should have pin 1 tied to pin 6 as this acts as the detect signal.

Table 23: J20 Battery Pin Assignments

Pin	Schematic Signal	SOM Pin	Type	Standard	Notes
1	DETECT	-	I	-	This pin should be tied to pin 6 of the mating plug
2	VBAT-SNS_P	J1-C16	Power	-	Tied to battery pack +
3	BATT_ID	J1-B19	I	-	
4	BATT_THERM	J1-B17	AI	-	100kΩ NTC thermistor to GND placed on battery
5	VBAT-SNS_N	J1-C17	Power	-	Tied to battery pack – post protection FETS
6	BATT-CONN	-	Power	-	Tied to battery pack +. This pin should be tied to pin 1 of the mating plug
7	BATT-CONN	-	Power	-	Tied to battery pack +
8	BATT-CONN	-	Power	-	Tied to battery pack +
9	GND	-	Power	-	Tied to battery pack -
10	GND	-	Power	-	Tied to battery pack -

Power Control – S5-S10, S14

To support applications for low power implementations, almost every interface on the development board has a toggleable load switch to enable/disable power. Additionally, power to each of these interfaces can be supplied from the on-board DC power supplies or from the SOM which runs off the battery. The switches all have weak pulldowns (10kΩ) and relatively strong pull ups (1kΩ) which can be connected through hardware switches. This allows the SOM to have control over power distribution regardless of the switch positions. If only hardware control is desired, the IOs should be configured as inputs or Hi-Z. The pinouts of these switches are described in the tables below.
NOTE: 3.3V from the SOM should not be used to power any interface on Rev 1 or 2 of the development board as the SOM presents a voltage anywhere from 3.3V to 4V which could result in unexpected behavior or damage to downstream ICs. Rev 3 of the development board and beyond fixes this problem.

Table 24: S5 eMMC and Wifi Power Control

Switch Position	Schematic Signal	SOM Pin	GPIO Number	Notes
1	MEM-EN	J1-E14	109	Low to disable power, high to enable 1.8V and 3.3V eMMC supply
2	MEM-SOM	J1-E15	110	Low to supply 1.8V via SOM, high to supply 1.8V and 3.3V via DC
3	3V3-WIFI-EN	J1-B9	34	Low to disable power, high to enable 3.3V Wi-Fi supply
4	3V3-WIFI-SOM	J1-C9	35	Low to supply 3.3V via DC, high to supply 3.3V via SOM

Table 25: S6 USB 2.0 Power Control

Switch Position	Schematic Signal	SOM Pin	GPIO Number	Notes
1	3V3-USB2.0-EN	J1-F4	56	Low to disable power, high to enable 3.3V USB 2.0 supply
2	3V3- USB2.0-SOM	J1-E5	57	Low to supply 3.3V via DC, high to supply 3.3V via SOM
3	5V- USB2.0-EN	J1-F5	58	Low to disable power, high to enable 5V USB 2.0 supply
4	5V- USB2.0-SOM	J1-E6	59	Low to supply 5V via DC, high to supply 5V via SOM

Table 26: S7 USBC and Audio Power Control

Switch Position	Schematic Signal	SOM Pin	GPIO Number	Notes
1	1V8-USBC-EN	J1-E1	52	Low to disable power, high to enable 1.8V USBC supply
2	1V8-USBC-SOM	J1-E2	53	Low to supply 1.8V via DC, high to supply 1.8V via SOM
3	1V8-AUD-EN	J1-C12	48	Low to disable power, high to enable 1.8V USBC supply
4	1V8-AUD-SOM	J1-G1	49	Low to supply 1.8V via DC, high to supply 1.8V via SOM

Table 27: S8 CSI and DSI Power Control

Switch Position	Schematic Signal	SOM Pin	GPIO Number	Notes
1	1V8-CSI-EN	J1-E19	113	Low to disable power, high to enable 1.8V CSI/DSI supply
2	1V8-CSI-SOM	J1-E20	114	Low to supply 1.8V via DC, high to supply 1.8V via SOM
3	3V3-CSI-SOM	J1-D19	115	Both low to disable power, SOM high DC low to supply 3.3V via SOM, SOM low DC high to supply 3.3V via DC, both high to automatically select
4	3V3-CSI-DC	J1-D20	116	

Table 28: S9 DP and PCIe Power Control

Switch Position	Schematic Signal	SOM Pin	GPIO Number	Notes
1	3V3-DP-EN	J1-C10	50	Low to disable power, high to enable 3.3V DP supply
2	3V3-DP-SOM	J1-F3	51	Low to supply 3.3V via DC, high to supply 3.3V via SOM
3	3V3-PCIE-SOM	J1-C13	42	Both low to disable power, SOM high DC low to supply 3.3V via SOM, SOM low DC high to supply 3.3V via DC, both high to automatically select
4	3V3-PCIE-DC	J1-C11	43	

Table 29: S10 Expansion Power Control

Switch Position	Schematic Signal	SOM Pin	GPIO Number	Notes
1	1V8-EXP-EN	J2-A2	12	Low to disable power, high to enable 1.8V expansion supply
2	1V8-EXP-SOM	J2-G2	13	Low to supply 1.8V via DC, high to supply 1.8V via SOM
3	3V3-EXP-EN	J2-E2	14	Low to disable power, high to enable 3.3V expansion supply
4	3V3-EXP-SOM	J2-G5	15	Low to supply 3.3V via DC, high to supply 3.3V via SOM

Table 30: S14 Wi-Fi and RTC Power Control

Switch Position	Schematic Signal	SOM Pin	GPIO Number	Notes
1	PS-HOLD	J1-F20	-	Pull this pin to 1V8-BOOT for JTAG communication else leave floating
2	MODE-0	J1-E16	-	Pull this pin to 1V8-BOOT for JTAG communication else leave floating
3	MODE-1	J2-B20	-	Pull this pin to 1V8-BOOT for JTAG communication else leave floating
4	VRTC	J2-C2	-	Close this switch to connect coin cell to VRTC

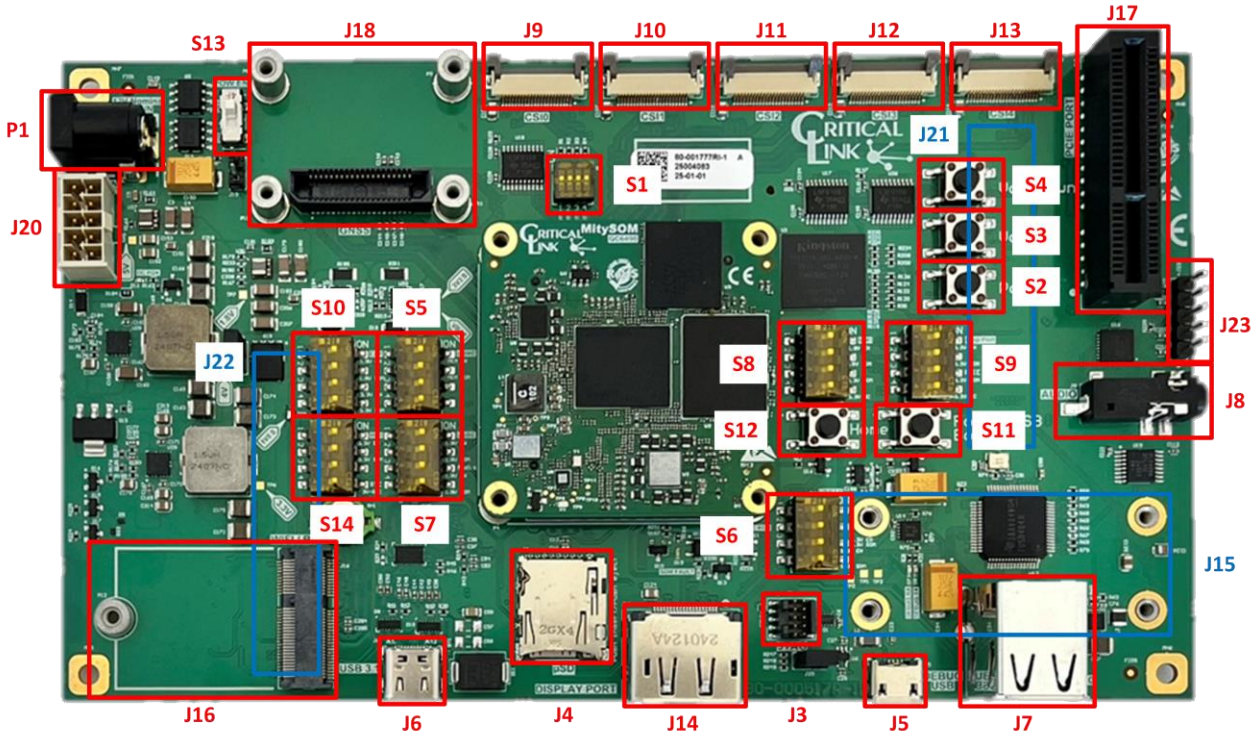
Included Components

The following table lists the components that are included with a MitySOM-QC6490/5430 Development Kit. See Table 32 for specific development kit ordering information and Table 33 for expansion kit ordering information.

Table 31: Included Items

Description	Interface Port	Qty. Included
MitySOM-QC6490/5430 Development Kit Board	n/a	Qty. 1
MitySOM-QC6490/5430 Module	J1 & J2	Qty. 1
12V 10A AC to DC Supply	P1	Qty. 1
USB-A to Micro-USB cable	J5	Qty. 1
USB-A to USB-C cable	J6	Qty. 1

MitySOM-QC6490 Development Kit Board with MitySOM-QC6490 Module



ORDERING INFORMATION

Development Kits

The following table lists the standard MitySOM-QC6490/5430 Development Kit configurations. For shipping status, availability, and lead time of these or other configurations please contact Critical Link at info@criticallink.com.

Table 32: Standard Model Numbers

Development Kit Model	Module Included	Module Operating Temp
80-001819RL-1	6490-EX-3X8-RL	-25 to 80° C
80-001820RL-1	5430-AX-2X4-RL	-25 to 80° C

Expansions Kits

The following table lists the standard expansion kits for the above development kits. For shipping status, availability, and lead time of these or other configurations please contact Critical Link at info@criticallink.com.

Table 33: Standard Expansion Kit Numbers

Expansion Kit Model	Desc	Included	Interface Port
80-001770RI-1	GNSS Expansion	Critical Link QC6490 GNSS Expansion Board 80-001770RI	J18
80-001771RI-1	Display Expansion	Critical Link QC6490 Display Expansion Board 80-001771RI Focus LCDs Capacitive touch LCD E40RC-FS1000-C	J15

MECHANICAL INTERFACE DESCRIPTION

Main Board Interface / Mounting

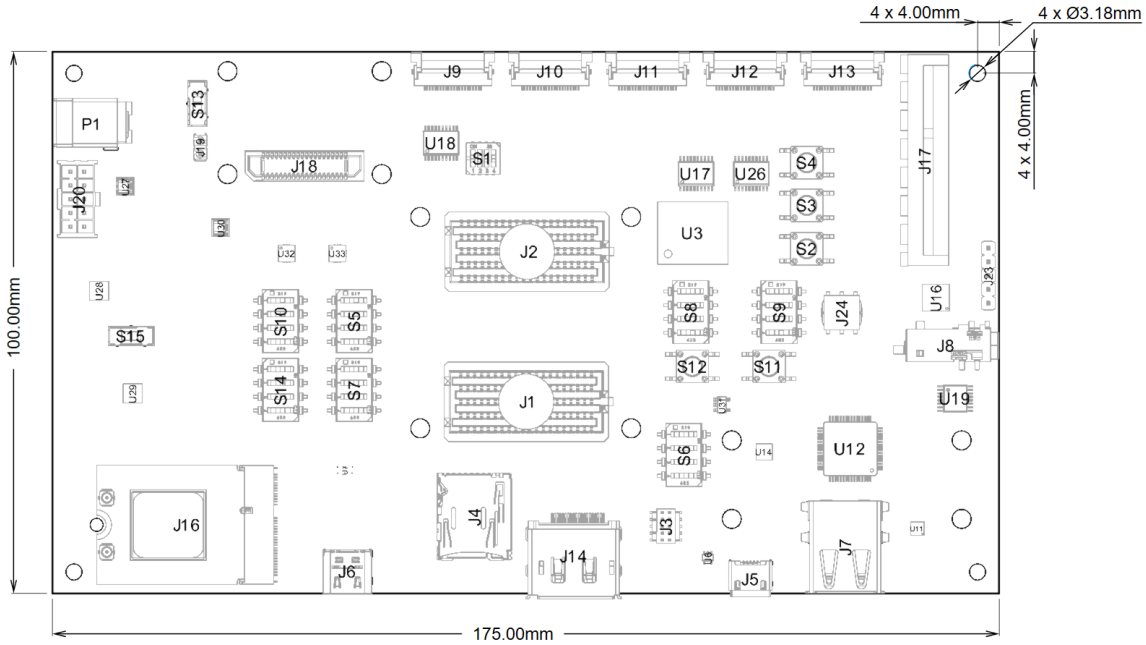


Figure 2: MitySOM-QC6490/5430 Development Kit Outline and Mounting Hole Locations (Top View, millimeters)

REVISION HISTORY

Date	Rev	Change Description
26-SEP-2025	A	Initial revision.