FPGA System on Modules

Feature	MitySOM-A5E Std	MitySOM-A5E Std	MitySOM-A5E Mini	MitySOM-A5E Mini	MitySBC-A5E	MitySBC-A5E	MitySOM-C10G	MitySOM-C10L	MitySOM-AM57(F)[7]	MityDSP-L138F-A7 [7]	MitySOM-A10S	MitySOM-5CSX
Technology	Altera Agilex 5	Altera Agilex 5	Altera Agilex 5	Altera Agilex 5	Altera Agilex 5	Altera Agilex 5	Altera Cyclone 10 GX	Altera Cyclone 10 LP	TI Sitara AM57x + Xilinx Artix-7	TI OMAP-L138 + Xilinx Artix-7	Altera Arria 10	Altera Cyclone V
DSP Processor	**None**	**None**	**None**	**None**	**None**	**None**	**None**	**None**	**Up to 2 C66x**	**C674x**	**None**	**None**
Max Speed	---	---	---	---	---	---	---	---	750 MHz	456 MHz	---	---
L1 Program Cache	---	---	---	---	---	---	---	---	32 KB (per core)	32 KB	---	---
L1 Data Cache	---	---	---	---	---	---	---	---	32 KB (per core)	32 KB	---	---
Internal RAM	---	---	---	---	---	---	---	---	288 KB	256 KB	---	---
ARM Processor	**Cortex-A76 & Cortex-A55**	**Cortex-A76 & Cortex-A55**	**Cortex-A76 & Cortex-A55**	**Cortex-A76 & Cortex-A55**	**Cortex-A76 & Cortex-A55**	**Cortex-A76 & Cortex-A55**	**NIOS II Softcore**	**NIOS II Softcore**	**Cortex-A15**	**ARM926EJ-S**	**Cortex-A9**	**Cortex-A9**
Cores	**Dual / Dual**	**Dual / Dual**	**Dual / Dual**	**Dual / Dual**	**Dual / Dual**	**Dual / Dual**	**N/A**	**N/A**	**Dual**	**Single**	**Dual**	**Single/Dual**
Max Speed	1800 / 1500 MHz	1400 / 1250 MHz	1800 / 1500 MHz	1400 / 1250 MHz	1800 / 1500 MHz	1400 / 1250 MHz	---	---	1500 MHz	456 MHz	1500 MHz	925 MHz
L1 Program Cache	64 KB / 64 KB	64 KB / 64 KB	64 KB / 64 KB	64 KB / 64 KB	64 KB / 64 KB	64 KB / 64 KB	---	---	32 KB (per core)	16 KB	32 KB (per core)	32 KB (per core)
L1 Data Cache	64 KB / 64 KB	64 KB / 64 KB	64 KB / 64 KB	64 KB / 64 KB	64 KB / 64 KB	64 KB / 64 KB	---	---	32 KB (per core)	16 KB	32 KB (per core)	32 KB (per core)
L2 Cache	256 KB / 128 KB	256 KB / 128 KB	256 KB / 128 KB	256 KB / 128 KB	256 KB / 128 KB	256 KB / 128 KB	---	---	2 MB (shared)	256 KB	512 KB (shared)	512 KB (shared)
Internal RAM	2 MB	2 MB	2 MB	2 MB	2 MB	2 MB	---	---	2.5 MB	8 KB	256 KB	64 KB
FPGA	**Agilex 5 (Device Group A)**	**Agilex 5 (Device Group B)**	**Agilex 5 (Device Group A)**	**Agilex 5 (Device Group B)**	**Agilex 5 (Device Group A)**	**Agilex 5 (Device Group B)**	**Cyclone 10 GX**	**Cyclone 10 LP**	**Artix-7 XC7A50T or XC7A15T**	**Artix-7 XC7A50T or XC7A15T**	**Arria 10SX**	**Cyclone V SoC**
Slices	up to 656 KLE	up to 656 KLE	up to 656 KLE	up to 656 KLE	up to 656 KLE	up to 656 KLE	up to 220,000 LE	up to 81,264 LE	up to 52,160 LE	up to 52,160 LE	up to 480,000 LE	up to 110,000 LE
Logic Cells	up to 222,400 ALM	up to 222,400 ALM	up to 222,400 ALM	up to 222,400 ALM	up to 222,400 ALM	up to 222,400 ALM	up to 80,330 ALM	---	up to 8150 ALM	up to 8150 ALM	up to 183,590 ALM	up to 41,509 ALM
Block RAM	up to 31.46 Mb	up to 31.46 Mb	up to 31.46 Mb	up to 31.46 Mb	up to 31.46 Mb	up to 31.46 Mb	up to 1.69Mb MLAB	up to 2,745Kb	up to 2.7Mb MLAB	up to 2.7Mb MLAB	up to 4.2Mb MLAB	up to 621Kb MLABs
Memory												
Max CPU RAM	8 GB LPDDR4	8 GB LPDDR4	8 GB LPDDR4	8 GB LPDDR4	8 GB LPDDR4	8 GB LPDDR4	1GB DDR3L	32MB HyperRAM	4 GB DDR3	256 MB DDR2	6 GB DDR4	4 GB DDR3
CPU RAM Throughput	14.9 GB / sec	10.6 GB / sec	14.9 GB / sec	10.6 GB / sec	14.9 GB / sec	10.6 GB / sec	7.45 GB/sec	200 MB/sec	up to 5.3 GB/sec	600 MB/sec	8.5 GB/sec	TBD
Max NOR FLASH	32 MB	32 MB	32 MB	32 MB	32 MB	32 MB	32 MB	32 MB	32 MB	16 MB	---	48 MB
Max NAND FLASH	N/A	N/A	N/A	N/A	64 GB	64 GB	---	---	N/A	512 MB	8 GB	---
Max FPGA RAM	8 GB LPDDR4	8 GB LPDDR4	N/A	N/A	8 GB LPDDR4	8 GB LPDDR4	---	---	N/A	N/A	2 GB	512 MB
FPGA RAM Throughput	14.9 GB / sec	10.6 GB / sec	N/A	N/A	14.9 GB / sec	10.6 GB / sec	---	---	N/A	N/A	4.26 GB/sec	TBD
Interface	**Dual Board to Board**	**Dual Board to Board**	**Single Board to Board**	**Single Board to Board**	**N/A**	**N/A**	**SO-DIMM DDR4**	**SO-DIMM DDR4**	**MXM 3.0 Type**	**SO-DIMM-200**	**Board to Board**	**MXM 3.0 Type**
Required Voltage	+5 to +12V	+5 to +12V	+5 to +12V	+5 to +12V	+12V	+12V	5V	5V	5V	3.3V	5V or 12V	5V
Avail FPGA I/O	up to 408	up to 408	up to 204	up to 204	up to 196	up to 196	up to 192	up to 192	up to 96	96	up to 168	up to 137
Peripherals												
Ethernet MAC	3x 10/100/ 1000/2500	3x 10/100/ 1000/2500	2x 10/100/1000	2x 10/100/1000	1x 10/100/ 1000/2500; 1x 10/100/1000	1x 10/100/ 1000/2500; 1x 10/100/1000	N/A	N/A	2 x PRU 10/100, 2 x 10/100/1000	10/100	3 x 10/100/1000	2 x 10/100/1000
McBSP Ports	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	2	N/A	N/A
LCD	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1	1	N/A	N/A
VPIF	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1	N/A	N/A
MMC/SD	1	1	1	1	1	1	N/A	N/A	3	1	1	1
SATA	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1	1	N/A	N/A
I2C	5	5	5	5	5	3	N/A	N/A	3	2[6]	5	4
SPI	2	2	2	2	2	0	N/A	N/A	3	2[6]	2 Master/2 Slave	2
USB	1 x 2.0 OTG; 1 x 3.1	1 x 2.0 OTG; 1 x 3.1	1 x 2.0 OTG; 1 x 3.1	1 x 2.0 OTG; 1 x 3.1	1 x 2.0 OTG; 1 x 3.1	1 x 2.0 OTG; 1 x 3.1	N/A	N/A	1 x 2.0; 1 x 3.0	2	1	2
UARTS	2	2	2	2	1	1	N/A	N/A	10	3[6]	2	2
CAN	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	2	N/A	N/A	2
PCIe	6 x4 Gen 4	6 x4 Gen 4	3 x4 Gen 4	3 x4 Gen 4	x8 Gen 3	x8 Gen 3	PCIe x 4	N/A	N/A	N/A	PCIe x 8	PCIe x4
MIPI	15 x4 CSI or DSI	15 x4 CSI or DSI	1 x4 CSI or DSI	1 x4 CSI or DSI	8 x4 CSI	8 x4 CSI	N/A	N/A	N/A	N/A	N/A	N/A
Transceivers	24 x 28.1 Gbps	24 x 17.16 Gbps	12 x 28.1 Gbps	12 x 17.16 Gbps	8 x 28.1 Gbps	8 x 17.6 Gbps	12 x 12.5 Gbps	N/A	2	N/A	12 x 11.3 Gbps	6 x 3.125 Gbps
Availability	**Production 2026**	**Production 2026**	**In Production**	**In Production**	**In Production**	**In Production**	**In Production**	**In Production**	**In Production**	**In Production**	**In Production**	**In Production**
Introduction Date	**2024**	**2024**	**2024**	**2024**	**2024**	**2024**	**2023**	**2022**	**2020**	**2022**	**2018**	**2013**

Notes:

1. FPGA and CPU share RAM via DSP EMIF, 100 MHz clock rate maximum.
2. LCD interface core is available for the FPGA to drive local and remote LCD display.
3. Soft FPGA MAC cores are available for 10/100 Mbit Ethernet Phy Control.
4. Spartan-6 features a 6 input LUT allowing for significantly more logic in the same number of slices when compared to a Spartan-3.
5. TMS6455 Option Including 8 Rocket I/O ports is available upon request.
6. The listed peripheral interfaces are available from the DSP/ARM. Additional interfaces can be created in modules with FPGA's.
7. These modules are available with or without the FPGA.
8. The Quad core Cortex-A78 is comprised of 1 core with 64 KB L1I and 64 KB L1D caches, and 3 cores with 32 KB L1I and 32 KB L1D caches

ARM System on Modules

Feature	MitySOM-QC6490	MitySOM-QC5430	MitySOM-AM62P	MitySOM-AM62A	MitySOM-AM62	MitySOM-AM57(F)[7]	MityDSP-L138F-A7 [7]	MitySOM-335x	MityDSP-L138(F)[7]
Technology	Qualcomm Dragonwing	Qualcomm Dragonwing	TI Sitara AM62Px	TI Sitara AM62Ax	TI Sitara AM62xx	TI Sitara AM57x + Xilinx Artix-7	TI OMAP-L138 + Xilinx Artix-7	TI Sitara AM335x	TI OMAP-L138 + Xilinx SPARTAN-6
DSP Processor	**Hexagon DSP**	**Hexagon DSP**	**None**	**C7x**	**None**	**Up to 2 C66x**	**C674x**	**None**	**C674x**
Max Speed	Up to 1382.4MHz	Up to 1382.4MHz	---	Up to 40 GFLOPS	---	750 MHz	456 MHz	---	456 MHz
L1 Program Cache	32kB	32kB	---	64 KB	---	32 KB (per core)	32 KB	---	32 KB
L1 Data Cache	32kB	32kB	---	32 KB	---	32 KB (per core)	32 KB	---	32 KB
Internal RAM	2MB of vTCM	2MB of vTCM	---	1.24MB SRAM	---	288 KB	256 KB	---	256 KB
ARM Processor	**Cortex-A78 & Cortex-A55**	**Cortex-A78 & Cortex-A55**	**Cortex-A53**	**Cortex-A53**	**Cortex-A53**	**Cortex-A15**	**ARM926EJ-S**	**Cortex-A8**	**ARM926EJ-S**
Cores	**Quad / Quad**	**up to Quad / Quad**	**Quad**	**Quad**	**Quad**	**Dual**	**Single**	**Single**	**Single**
Max Speed	2.7 GHz	2.4 GHz	1400 MHz	1400 MHz	1400 MHz	1500 MHz	456 MHz	1000 MHz	456 MHz
L1 Program Cache	Up to 64KB[8] / 32KB	Up to 64KB[8] / 32KB	32 KB	32 KB	32 KB	32 KB (per core)	16 KB	32 KB	16 KB
L1 Data Cache	Up to 64KB[8] / 32KB	Up to 64KB[8] / 32KB	32 KB	32 KB	32 KB	32 KB (per core)	16 KB	32 KB	16 KB
L2 Cache	256 KB / 128 KB	256 KB / 128 KB	512 KB	512 KB	512 KB	2 MB (shared)	256 KB	256 KB	256 KB
Internal RAM	172kB IMEM, 512kB GMEM	172kB IMEM, 512kB GMEM	---	---	---	2.5 MB	8 KB	64 KB	8 KB
FPGA	**None**	**None**	**None**	**None**	**None**	**Artix-7 XC7A50T or XC7A15T**	**Artix-7 XC7A50T or XC7A15T**	**None**	**XC6SLX45 or XC6SLX16 (optional)[4]**
Slices	---	---	---	---	---	up to 52,160 LE	up to 52,160 LE	---	up to 6,822
Logic Cells	---	---	---	---	---	up to 8150 ALM	up to 8150 ALM	---	up to 43,661
Block RAM	---	---	---	---	---	up to 2.7Mb MLAB	up to 2.7Mb MLAB	---	up to 2,088 Kb
Memory									
Max CPU RAM	8 GB LPDDR5	8 GB LPDDR5	8 GB LPDDR4	16 GB LPDDR4	4 GB DDR4	4 GB DDR3	256 MB DDR2	1 GB	256 MB
CPU RAM Throughput	25.6 GB / sec	25.6 GB / sec	13.2 GB/sec	14.9 GB/sec	3.2 GB/sec	up to 5.3 GB/sec	600 MB/sec	800 MB/sec	532 MB/sec
Max NOR FLASH	N/A	N/A	256 MB	256 MB	256 MB	32 MB	16 MB	8 M	8 M
Max NAND FLASH	256 GB	256 GB	256 GB	128 GB	128 GB	N/A	512 MB	1 GB	512 MB
Max FPGA RAM	N/A	N/A	---	---	---	N/A	N/A	---	N/A
FPGA RAM Throughput	N/A	N/A	---	---	---	N/A	N/A	---	N/A
Interface	**Dual Board to Board**	**Dual Board to Board**	**SO-DIMM DDR4**	**SO-DIMM DDR4**	**SO-DIMM DDR4**	**MXM 3.0 Type**	**SO-DIMM-200**	**SO-DIMM-204**	**SO-DIMM-200**
Required Voltage	+4, +5V	+4, +5V	3.3V	3.3V	3.3V	5V	3.3V	3.3V - 5V	3.3V
Avail FPGA I/O	N/A	N/A	---	---	---	up to 96	96	---	88
Peripherals									
Ethernet MAC	N/A	N/A	2 x 10/100/1000	2 x 10/100/1000	2 x 10/100/1000	2 x PRU 10/100, 2 x 10/100/1000	10/100	2 x 10/100/1000	10/100
McBSP Ports	N/A	N/A	N/A	N/A	N/A	N/A	2	N/A	2
LCD	N/A	N/A	1	1	2	1	1	1	1
VPIF	N/A	N/A	N/A	N/A	N/A	N/A	1	N/A	1
MMC/SD	N/A	N/A	2	2	2	3	1	3	1
SATA	N/A	N/A	N/A	N/A	N/A	1	1	N/A	1
I2C	7	7	4	3	3	3	2[6]	2	2[6]
SPI	3	3	3	3	3	3	2[6]	2	2[6]
USB	1 x 2.0 OTG; 1 x 3.1	1 x 2.0 OTG; 1 x 3.1	2	2	2	1 x 2.0; 1 x 3.0	2	2	2
UARTS	3	3	7	7	7	10	3[6]	6	3[6]
CAN	N/A	N/A	3	3	3	2	N/A	2	N/A
PCIe	2 x Gen 3	2 x Gen 3	N/A	N/A	N/A	N/A	N/A	N/A	N/A
MIPI	1 x4 DSI, 5 x4 CSI	1 x4 DSI, 5 x4 CSI	1 x4 CSI, 1 x4 DSI	1 x4 CSI	1	N/A	N/A	N/A	N/A
Transceivers	N/A	N/A	N/A	N/A	N/A	2	N/A	N/A	N/A
Availability	**Production 2026**	**Production 2026**	**Production 2025**	**In Production**	**In Production**	**In Production**	**In Production**	**In Production**	**In Production**
Introduction Date	**2025**	**2025**	**2023**	**2023**	**2022**	**2020**	**2022**	**2012**	**2010**

Notes:

1. FPGA and CPU share RAM via DSP EMIF, 100 MHz clock rate maximum.
2. LCD interface core is available for the FPGA to drive local and remote LCD display.
3. Soft FPGA MAC cores are available for 10/100 Mbit Ethernet Phy Control.
4. Spartan-6 features a 6 input LUT allowing for significantly more logic in the same number of slices when compared to a Spartan-3.
5. TMS6455 Option Including 8 Rocket I/O ports is available upon request.
6. The listed peripheral interfaces are available from the DSP/ARM. Additional interfaces can be created in modules with FPGA's.
7. These modules are available with or without the FPGA.
8. The Quad core Cortex-A78 is comprised of 1 core with 64 KB L1I and 64 KB L1D caches, and 3 cores with 32 KB L1I and 32 KB L1D caches