MitySOM™ Document

Document: MitySOM-C10x Carrier Board Design Guide

Revision: 1.1

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1 Overview

1.1 MitySOM-C10x Fast Facts for Getting Started

Facts	MitySOM-C10G, MitySOM-C10L
Required connectors placed on carrier board[1]	**C10G and C10L**: TE Connectivity 2309413-1: 260 position card edge receptacle **C10G**: Samtec ERF5-060-05.0-L-DV-TR: 120 position fine-pitch hi-speed header
Input Voltages supplied from carrier board	+5V: to SOM on-board power supplies
Supported I/O standards	Refer to MitySOM-C10L and MitySOM-C10G datasheets
I/O Bank Voltages	**C10L**: +1.2V to +3.3V, user defined from Carrier Board interface **C10G**: +1.8V, powered from SOM on-board supply
Total number of FPGA I/O's	**C10L**: up to 180 direct connect I/O (3 Banks, 60 I/O+4 clock inputs per bank) **C10G**: up to 192 direct connect I/O (4 Banks, 48 per bank)
Number of LVDS capable I/O's	**C10L**: up to 38 true, 28 emulated pairs **C10G**: up to 70 pairs
Muti-gigabit transceivers	**C10L**: none **C10G**: up to 12 pairs RX, 12 pairs TX, 4 pair CLK
SOC Peripherals**	Program / Data Storage: • **C10G:** Up to 1 GB DDR3L SDRAM, up to 32 MB serial NOR FLASH • **C10L**: 32 MB HyperRAM, up to 32 MB serial NOR FLASH FPGA fabric options: • **C10L:** 16k to 80k logic elements (LE) • **C10G:** 105k to 220k logic elements (LE) • Speed grades from -6 to -8
[1] use specified part or equivalent	

1.2 Introduction

The MitySOM-C10L and MitySOM-C10G modules (collectively referred to as MitySOM-C10x) are System-On-Modules (SOMs) designed to be easy to integrate into an end-user embedded system. The MitySOM-C10x modules integrate crucial elements of an FPGA-based embedded system using an established design framework with a common set of core libraries. End-user design of the application PCB is also simplified, freeing the SOM end user to concentrate on application-specific interfaces and peripheral devices. The learning curve associated with designing hardware for a high-speed embedded digital system from scratch is greatly reduced.

Developers are encouraged to review the MitySOM-C10x Development Kit design schematics, available on the Critical Link support site. The Development Kit has been designed using Altium Designer, the FPGA vendor's tool suite and is qualified utilizing a full software support package available for the interfaces and devices on the board. Customers may contact Critical Link for access to Altium CAD design files and FPGA demonstration project files for the development kit. Review of customer designs by Critical Link may be scheduled by e-mailing: support@criticallink.com

1.3 MitySOM-C10x Family Modules

The MitySOM-C10x family of modules are based on Intel (Altera) Cyclone 10 LP or GX FPGA devices. See the "fast facts" in section 1.1 of this document and refer to the manufacturer's FPGA overview and datasheet documents for the C10LP and C10GX devices for details.

Both MitySOM-C10x SOM types includes a power supply & management subsystem, RAM, NOR FLASH memory, and interfaces to a carrier board with a 260-pin SO-DIMM DDR4-style card-edge receptable. The MitySOM-C10G also interfaces multi-gigabit transceivers to the carrier board via a 120-position, fine-pitch, connector set.

MitySOM-C10x products are available with options for RAM and FLASH memory depth, FPGA size, speed grade and operating temperature range. Please visit the "MITYSOM-C10L" or "MITYSOM-C10G" product page at criticallink.com or contact Critical Link for the current list of orderable MitySOM-C10x part numbers.

1.4 SOM Dimensions

The dimensions of the MitySOM-C10L and MitySOM-C10G are shown in the mechanical outline drawings below. Note that the widths of the two SOM types is the same, but the length of the C10L SOM is half of the C10G SOM.

See section 1.5 for location of fastener mounting holes (not shown in Figure 1 or Figure 2).

Figure 1, part 1 of 2:

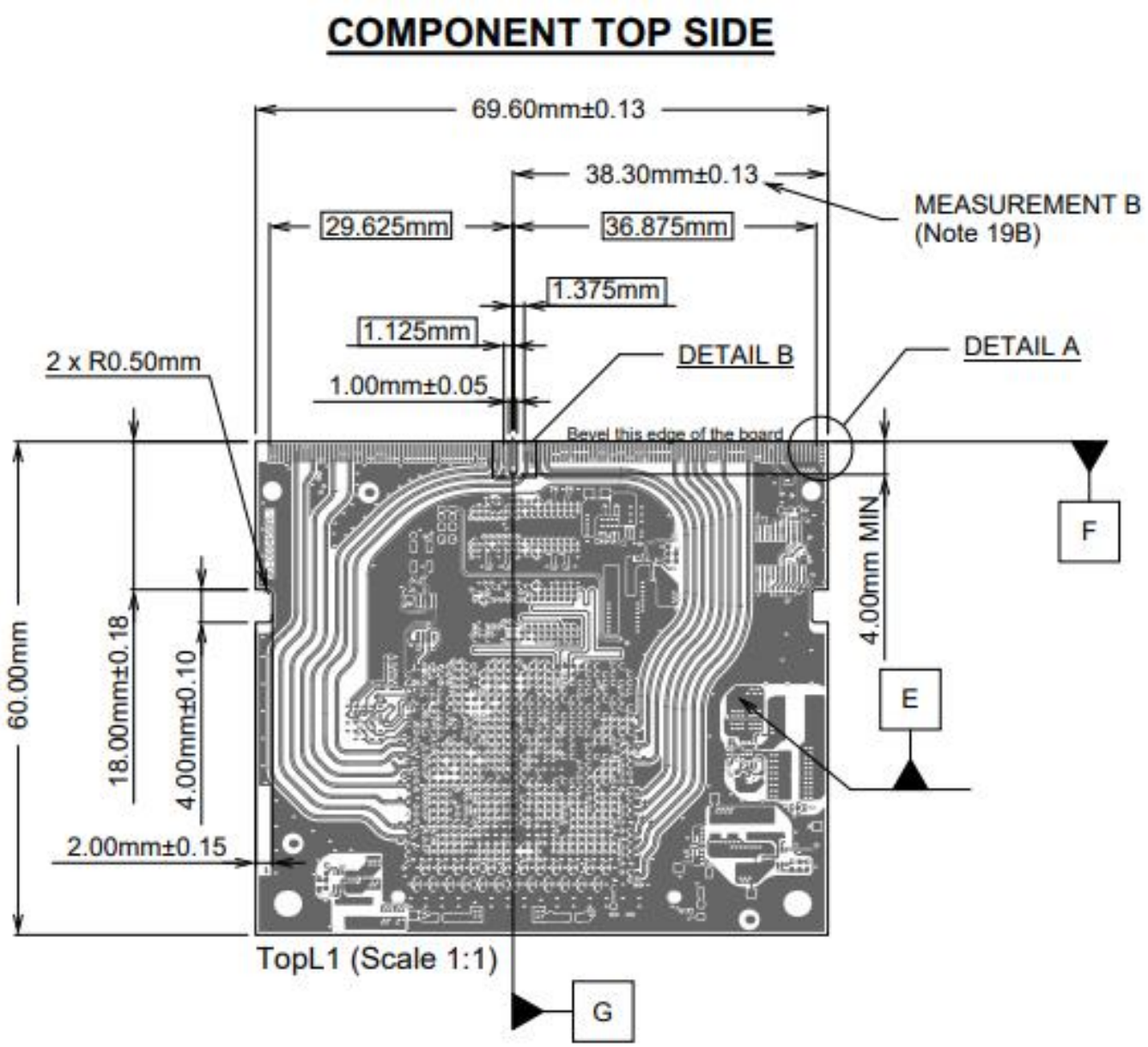

Figure 1, part 2 of 2:

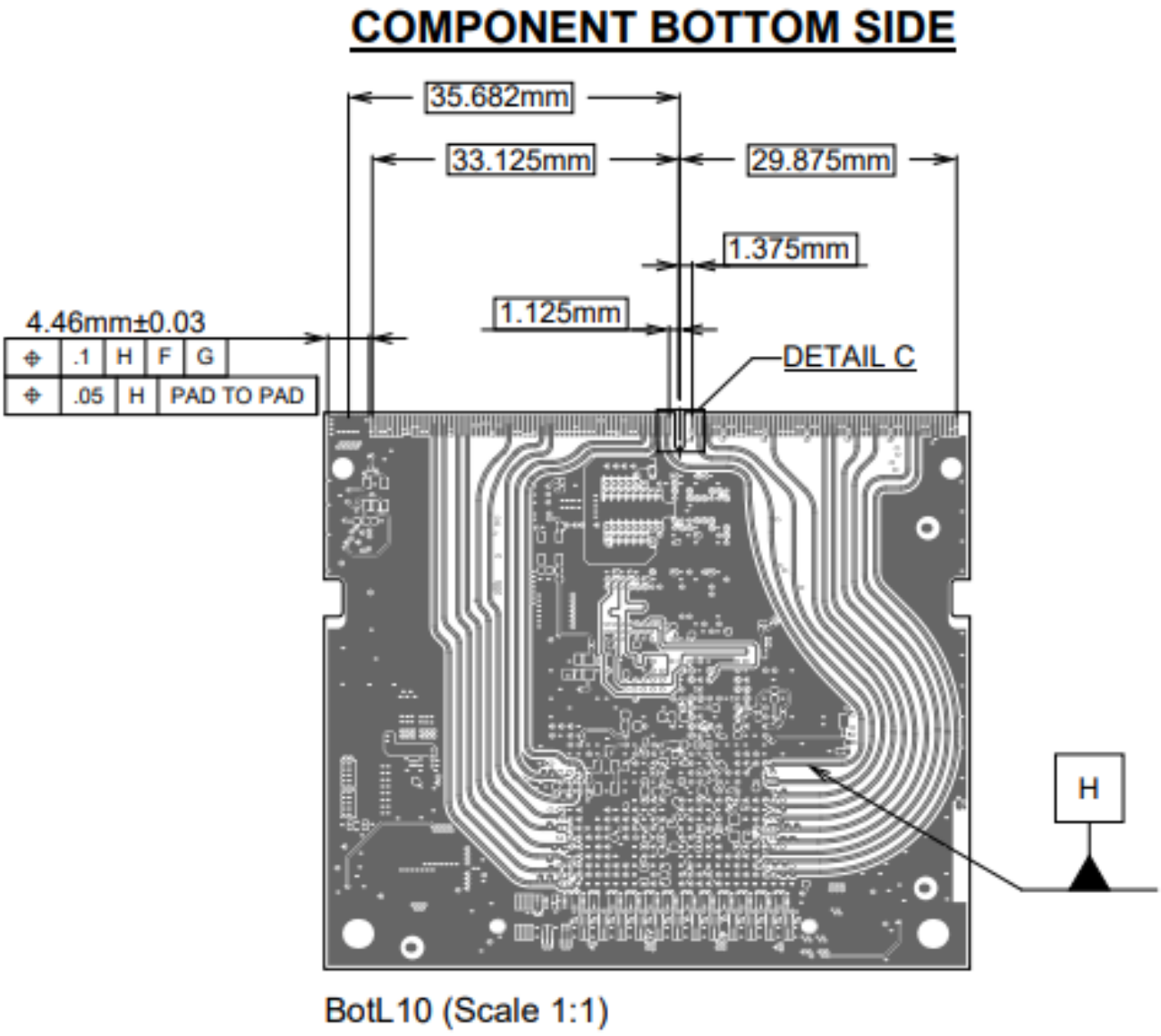

Figure 1: MitySOM-C10G Top and Bottom Side Mechanical Outlines

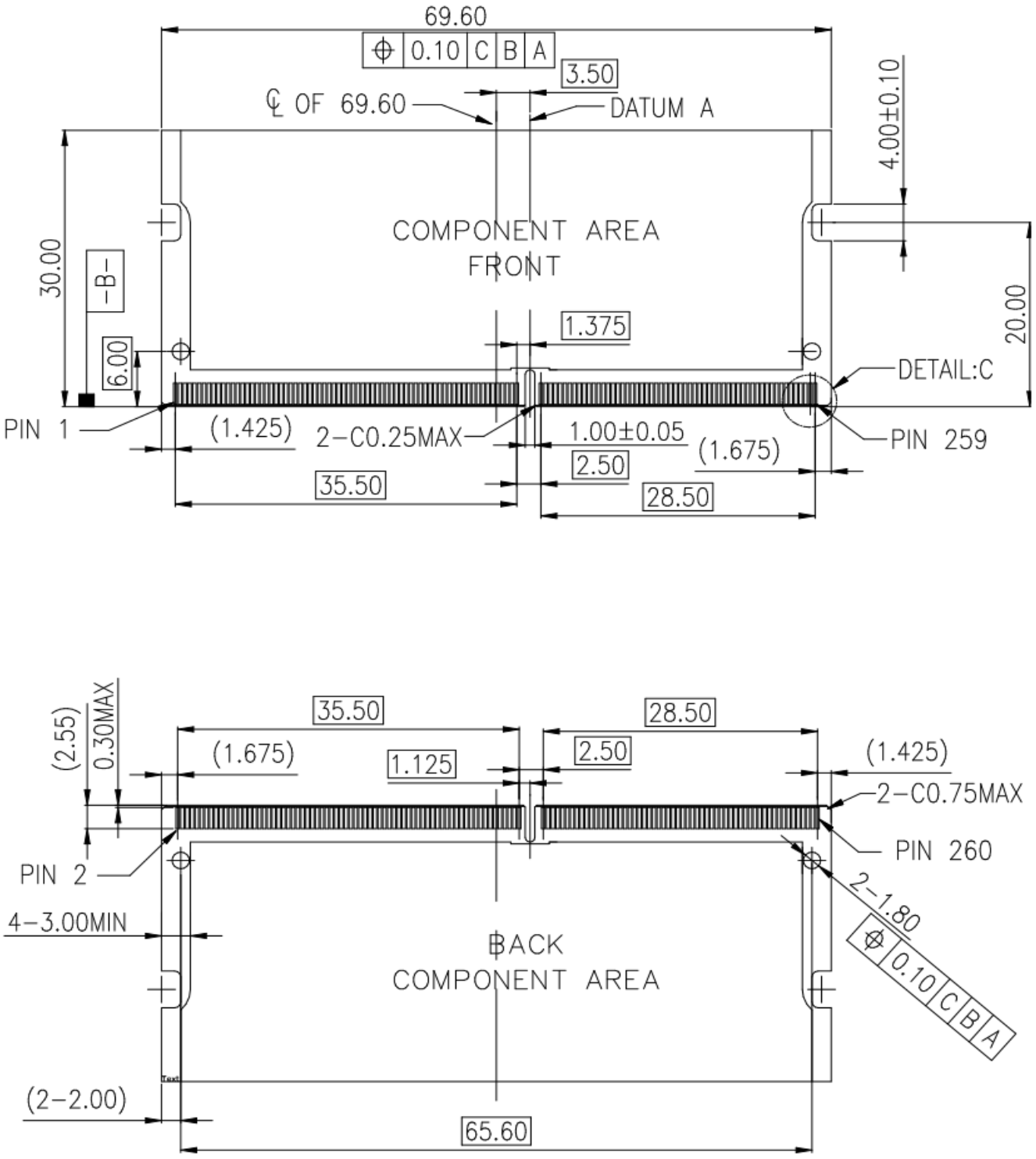

Figure 2: MitySOM-C10L: DDR4 form factor
Top and Bottom Side Mechanical Outlines
(fastener mounting holes not shown)

1.5 Carrier Board: SOM Outline

The primary 260-pin SO-DIMM type card-edge receptacle installed on the carrier board has tension spring clips which snap into grooves along the side edges of the SOM. This is primary means of retention for the SOM. Additional support and retention provided by fasteners into carrier board-mounted spacers or standoffs is recommended.

Fastener mounting holes on the carrier board, at the opposite end of the SOM from the SO-DIMM receptacle, should be sized for installation of 7 mm high threaded spacers or stand-offs.

Recommended spacer part number: Würth Electronik 971070354 or equivalent.

The 7 mm spacer height matches the board-to-board distance between the carrier board and SOM when the SOM is fully seated into the recommended SO-DIMM style card edge connector (and also, for the C10G SOM, the Samtec 120-position connector set).

The mechanical outline of the MitySOM-C10G is illustrated in Figure 3 and shows the location of the bottom side-mounted 120-pin fine-pitch plug-type connector (identified as ERF5-060-05.0-L-DV-TR) and placement of the mounting holes. *Note: MitySOM-C10L does not require the secondary 120-pin connector.*

Measurements are referenced to the alignment features of the 260 position card-edge receptacle connector (identified as 2309413-1).

- Blue measurements correspond to the mounting holes for the SOM;
- Green measurements are for the secondary connector alignment holes.

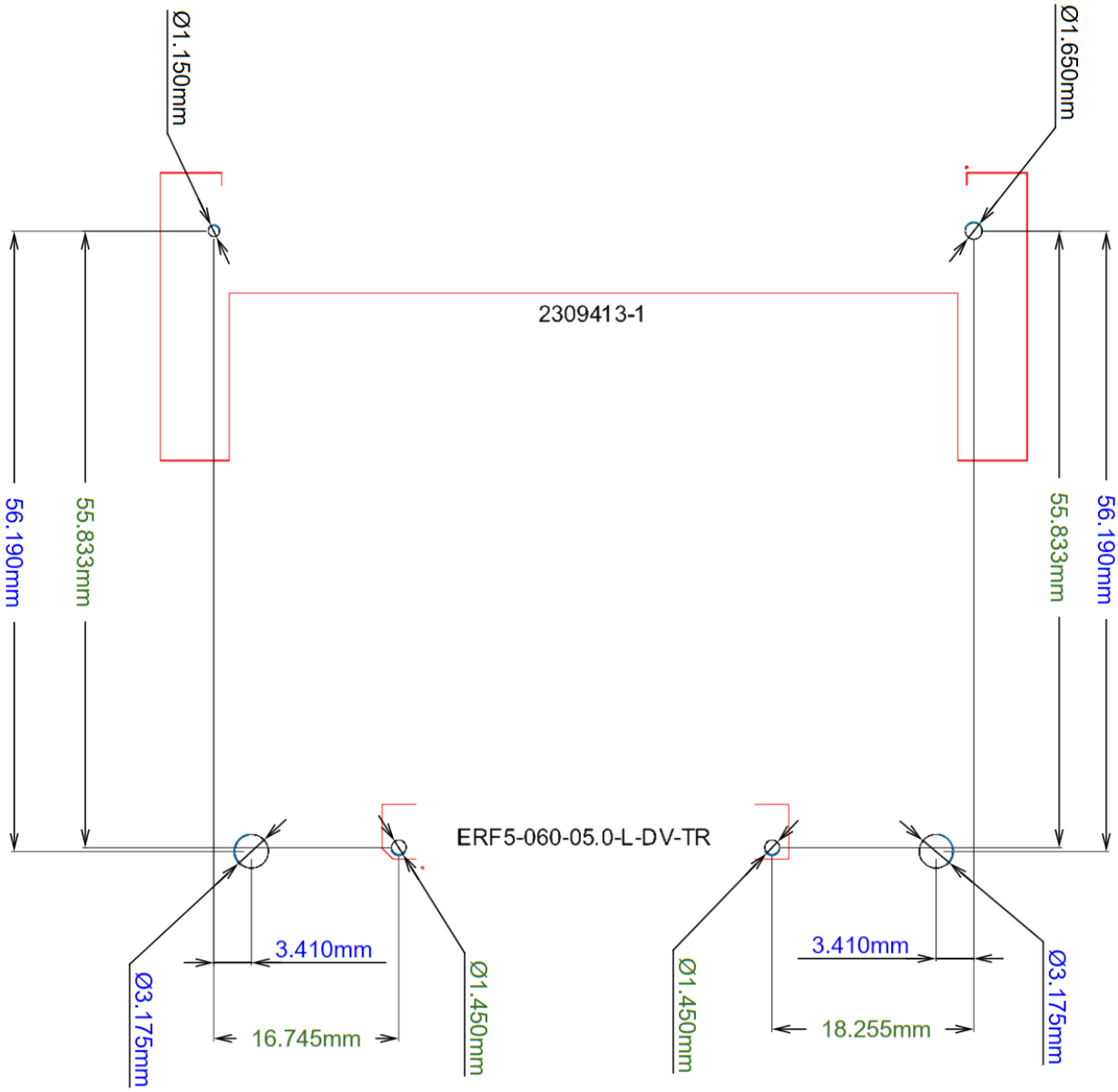

Figure 3: MitySOM-C10G -- fastener mounting holes, 120-pin bottom side secondary connector locations

Notes:

- MitySOM-C10L fastener mounting holes are placed 30.0 mm closer to SO-DIMM card-edge receptacle (on Y or vertical axis in Figure 3): at 26.190 mm (blue measurement) from reference point.
- Carrier Board designs for MitySOM-C10L need not support the secondary 120-pin connector (green measurements).

1.6 Reference Documents and Links

From Critical Link LLC:

MitySOM-C10L Product Page:
https://www.criticallink.com/product/mitysom-c10l/

MitySOM-C10G Product Page:
https://www.criticallink.com/product/mitysom-c10g/

MitySOM-C10x Support (Wiki):
https://support.criticallink.com/redmine/projects/mitysom_c10l/wiki/Wiki

MitySOM-C10L Data Sheet:
https://www.criticallink.com/wp-content/uploads/MitySOM-C10L-Datasheet.pdf

MitySOM-C10G Data Sheet:
https://www.criticallink.com/wp-content/uploads/MitySOM-C10G-Datasheet.pdf

MitySOM-C10x Family Development Kit Product Page:
https://www.criticallink.com/product/mitysom-c10l-development-kit/

From Intel / Altera:

Cyclone 10 LP Device Datasheet
Intel document: C10LP51002, ID: 683251, version 2022.10.31
https://www.intel.com/content/www/us/en/docs/programmable/683251/current/device-datasheet.html

Cyclone 10 LP Device Overview
Intel document: C10LP51001, ID: 683879, version 2022.05.27
https://www.intel.com/content/www/us/en/docs/programmable/683879/current/device-overview.html

Cyclone 10 GX Device Datasheet
Intel document: C10GX51002, ID: 683828, version 2022.02.14
https://www.intel.com/content/www/us/en/docs/programmable/683828/current/device-datasheet.html

Cyclone 10 GX Device Overview
Intel document: C10GX51001, ID: 683485, version 2019.04.01
https://www.intel.com/content/www/us/en/docs/programmable/683485/current/device-overview.html

2 Connectors

MitySOM-C10x modules utilize a connector set to physically interface with the end user's application board ("SOM Carrier" or "Carrier" board). Recommended sources for carrier board connectors are listed below in bold type.

- 260 position, SO-DIMM DDR4-style card edge connector provides primary access to SOM I/O:
  - SOM board: 'gold finger' pads spaced at 0.5 mm pitch on top and bottom sides along board edge, with pad gap for 'key' notch, no physical connector
  - Board-to-board spacing = 7.0 mm
  - **Carrier board card edge receptacle: TE Connectivity 2309413-1**
- C10G SOM only: 120-position (dual row, 60 positions per row), 0.5 mm pitch, 7.0 mm mated height, high speed-capable connector set provides access to additional multi-gigabit transceiver I/O for C10G SOM only:
  - SOM board plug-type connector: Samtec ERM5-060-02.0-L-DV-TR
  - **Carrier board receptacle-type connector: Samtec ERF5-060-05.0-L-DV-TR**

This connector set was chosen for its high density, compact size, ease of procurement, and low cost. With the SO-DIMM DDR4-style card edge connector, a physical socket component is only required on the carrier board. The connector set allows the MitySOM-C10x module to lay flat, parallel to the carrier board surface with a 7.0 mm board-to-board distance. The mounting method is similar to installation of expansion memory and interface cards into compact equipment like laptop computers.

2.1 SO-DIMM Card-edge Compatibility

The 260-pin SO-DIMM interface, consisting of a set of card-edge placed "gold finger" pads on top and bottom sides of a plug-in board, and a mating receptacle connector on a host or carrier board, was developed for DDR4 high-speed memory expansion cards. **Please note that MitySOM-C10x modules are NOT electrically compatible with the SO-DIMM socket standard**, and intermixing modules/sockets from the two standards would very likely cause permanent damage to one or both sides of the inteface.

A MitySOM-C10x module must only be installed into a board which is designed for compatibility with the SOM's pin-out and electrical characteristics.

The carrier board footprint for the SO-DIMM-style card-edge receptacle compatible with a MitySOM-C10x module must provide individual PCB pads for all 260 available connector pins. Developers of carrier board designs may request SOM connector footprints from Critical Link which are compatible with Altium Designer.

2.2 MitySOM-C10x Pin-out

Tables 1 and 2 contain a summary of MitySOM-C10x connector pin mapping which includes:

- Connector pin assignment
- Signal Type: Power, I/O or reserved
- C10L and C10G SOM net names
- Differences in LVDS polarity between C10L and C10G (highlighted in yellow for C10G SOM)

Primary (Card-Edge) Receptacle

Top Edge Connector				Bottom Edge Connector			
Pin	**Type**	**C10L SOM Signal**	**C10G SOM Signal**	**Pin**	**Type**	**C10L SOM Signal**	**C10G SOM Signal**
1				2			
3				4			
5				6			
7	Power	+5V	+5V	8	Power	GND	GND
9				10			
11				12			
13				14			
15	RSVD	RESERVED	PROC_RST	16	In	TDI	TDI
17	RSVD	RESERVED	NC	18	Out	TDO	TDO
19	Out	+2.5V_JTAG	+1.8V_JTAG	20	In	TCK	TCK
21	Out	POWER_GOOD	PWR_OK	22	In	TMS	TMS
23	I/O	NCONFIG	NCONFIG.AC8	24	Out	CONF_DONE	CONF_DONE
25	Power	VCCIO4_5	RESERVED	26	Power	VCCIO2_3	RESERVED
27				28			
29	Power	GND	GND	30	Power	GND	GND
31				32			
33	I/O	B2_DIFFCLK1_P	B2K_LVDS_16_P	34	I/O	B3_IO_PLL1_CLKOUT_P	B2K_LVDS_18_P
35	I/O	B2_DIFFCLK1_N	B2K_LVDS_16_N	36	I/O	B3_IO_PLL1_CLKOUT_N	B2K_LVDS_18_N
37	I/O	B2_DIO25_P	B2K_LVDS_15_P	38	I/O	B3_DIO8_P	B2L_DIFFIO_15_N
39	I/O	B2_DIO25_N	B2K_LVDS_15_N	40	I/O	B3_DIO8_N	B2L_DIFFIO_15_P
41	I/O	B2_DIO24_P	B2K_LVDS_14_N	42	I/O	B3_DIO9_P	B2L_DIFFIO_8_N
43	I/O	B2_DIO24_N	B2K_LVDS_14_P	44	I/O	B3_DIO9_N	B2L_DIFFIO_8_P
45	I/O	B2_DIO21_P	B2K_LVDS_13_P	46	I/O	B3_DIO10_P	B2L_DIFFIO_10_P
47	I/O	B2_DIO21_N	B2K_LVDS_13_N	48	I/O	B3_DIO10_N	B2L_DIFFIO_10_N
49	Power	GND	GND	50	Power	GND	GND
51	I/O	B2_DIO20_N	B2K_LVDS_11_N	52	I/O	B3_DIO12_P	B2L_DIFFIO_7_P
53	I/O	B2_DIO20_P	B2K_LVDS_11_P	54	I/O	B3_DIO12_N	B2L_DIFFIO_7_N
55	I/O	B2_DIO18_N	B2K_LVDS_17_N	56	I/O	B3_DIO15_P	B2L_DIFFIO_22_P
57	I/O	B2_DIO18_P	B2K_LVDS_17_P	58	I/O	B3_DIO15_N	B2L_DIFFIO_22_N

59	I/O	B2_DIO17_N	B2K_LVDS_8_P	60	I/O	B3_DIO16_P	B2L_DIFFIO_6_P
61	I/O	B2_DIO17_P	B2K_LVDS_8_N	62	I/O	B3_DIO16_N	B2L_DIFFIO_6_N
63	I/O	B2_DIO16_N	B2K_LVDS_7_P	64	I/O	B3_DIO11_P	B2L_DIFFIO_13_P
65	I/O	B2_DIO16_P	B2K_LVDS_7_N	66	I/O	B3_DIO11_N	B2L_DIFFIO_13_N
67	Power	GND	GND	68	Power	GND	GND
69	I/O	B2_DIO19_P_DPCLK1	B2K_LVDS_23_N	70	I/O	B3_DIFFCLK6_P	B2L_DIFFIO_12_N
71	I/O	B2_DIO19_N	B2K_LVDS_23_P	72	I/O	B3_DIFFCLK6_N	B2L_DIFFIO_12_P
73	I/O	B2_DIO14_P	B2L_DIFFIO_4_P	74	I/O	B3_DIO17_P	B2L_DIFFIO_19_P
75	I/O	B2_DIO14_N	B2L_DIFFIO_4_N	76	I/O	B3_DIO17_N	B2L_DIFFIO_19_N
77	I/O	B2_DIO15_P	B2K_LVDS_9_P	78	I/O	B3_IO29	B2L_DIFFIO_20_N
79	I/O	B2_DIO15_N	B2K_LVDS_9_N	80	I/O	B3_IO12	B2L_DIFFIO_20_P
81	I/O	B2_DIO13_P	B2K_LVDS_10_N	82	I/O	B3_IO16	B2K_LVDS_21_N
83	I/O	B2_DIO13_N	B2K_LVDS_10_P	84	I/O	B3_IO6	B2K_LVDS_21_P
85	Power	GND	GND	86	Power	GND	GND
87	I/O	B2_IO15	B2L_DIFFIO_5_P	88	I/O	B3_IO13	B2L_DIFFIO_23_P
89	I/O	B2_IO22_RUP1	B2L_DIFFIO_5_N	90	I/O	B3_DIO18_P	B2L_DIFFIO_23_N
91	I/O	B2_IO22_RDN1	B2L_DIFFIO_1_P	92	I/O	B3_DIO18_N	B2K_LVDS_12_N
93	I/O	B2_IO37	B2L_DIFFIO_1_N	94	I/O	B3_IO44	B2K_LVDS_12_P
95	I/O	B2_IO38_CDPCLK1	B2L_DIFFIO_16_P	96	I/O	B3_IO26	B2L_DIFFIO_9_N
97	I/O	B2_IO39	B2L_DIFFIO_16_N	98	I/O	B3_IO31	B2L_DIFFIO_9_P
99	I/O	B2_IO22	B2K_LVDS_22_P	100	I/O	B3_IO33	B2L_DIFFIO_11_P
101	I/O	B2_IO23	B2K_LVDS_22_N	102	I/O	B3_IO39	B2L_DIFFIO_11_N
103	Power	GND	GND	104	Power	GND	GND
105	I/O	B5_DIO34_N_CDPCLK4	B2K_LVDS_6_N	106	I/O	B4_DIFFCLK7_P	B2L_DIFFIO_24_P
107	I/O	B5_DIO34_P	B2K_LVDS_6_P	108	I/O	B4_DIFFCLK7_N	B2L_DIFFIO_24_N
109	I/O	B5_DIO35_N	B2K_LVDS_3_P	110	I/O	B4_DIO19_P	B2L_DIFFIO_21_P
111	I/O	B5_DIO35_P	B2K_LVDS_3_N	112	I/O	B4_DIO19_N	B2L_DIFFIO_21_N
113	I/O	B5_DIO33_N	B2K_LVDS_2_P	114	I/O	B4_DIO20_P	B2K_LVDS_1_P
115	I/O	B5_DIO33_P	B2K_LVDS_2_N	116	I/O	B4_DIO20_N	B2K_LVDS_1_N
117	I/O	B5_DIO31_N	B2L_DIFFIO_14_N	118	I/O	B4_DIO22_P	B2L_DIFFIO_18_P
119	I/O	B5_DIO31_P	B2L_DIFFIO_14_P	120	I/O	B4_DIO22_N	B2L_DIFFIO_18_N
121	Power	GND	GND	122	Power	GND	GND
123	I/O	B5_DIO28_N	B2L_DIFFIO_2_N	124	I/O	B4_DIO24_P	B2L_DIFFIO_3_P

125	I/O	B5_DIO28_P	B2L_DIFFIO_2_P	126	KEY	B4_DIO24_N	B2L_DIFFIO_3_N
127	I/O	B5_DIO27_N	B2K_LVDS_5_P	128	KEY	B4_DIO30_P	B2L_DIFFIO_17_P
129	I/O	B5_DIO27_P	B2K_LVDS_5_N	130	KEY	B4_DIO30_N	B2L_DIFFIO_17_N
131	I/O	B5_DIFFCLK3_P	B2K_LVDS_24_P	132	KEY	B4_DIO21_P	B2K_LVDS_20_N
133	I/O	B5_DIFFCLK3_N	B2K_LVDS_24_N	134	Power	B4_DIO21_N	B2K_LVDS_20_P
135	I/O	B5_DIO25_N	B2K_LVDS_4_P	136	Power	B4_DIO29_P	B2K_LVDS_19_P
137	I/O	B5_DIO25_P	B2K_LVDS_4_N	138	I/O	B4_DIO29_N	B2K_LVDS_19_N
139	Power	GND	GND	140	Power	GND	GND
141	I/O	B5_DIO26_N	B2J_LVDS_4_N	142	I/O	B4_DIO27_P	B2A_LVDS_4_N
143	I/O	B5_DIO26_P	B2J_LVDS_4_P	144	I/O	B4_DIO27_N	B2A_LVDS_4_P
145	Power	GND	GND	146	Power	GND	GND
147	I/O	B5_DIO32_N	B2J_LVDS_5_N	148	I/O	B4_DIO31_P	B2A_LVDS_6_P
149	I/O	B5_DIO32_P	B2J_LVDS_5_P	150	I/O	B4_DIO31_N	B2A_LVDS_6_N
151	I/O	B5_DIO24_N	B2J_LVDS_6_P	152	I/O	B4_IO5	B2A_LVDS_2_N
153	I/O	B5_DIO24_P	B2J_LVDS_6_N	154	I/O	B4_IO10	B2A_LVDS_2_P
155	I/O	B5_DIO21_N	B2A_LVDS_1_N	156	I/O	B4_IO15	B2A_LVDS_23_P
157	I/O	B5_DIO21_P	B2A_LVDS_1_P	158	I/O	B4_IO18	B2A_LVDS_23_N
159	Power	GND	GND	160	Power	GND	GND
161	I/O	B5_DIO20_N	B2J_LVDS_1_N	162	I/O	B4_IO_PLL4_CLKOUT_P	B2A_LVDS_19_N
163	I/O	B5_DIO20_P	B2J_LVDS_1_P	164	I/O	B4_IO_PLL4_CLKOUT_N	B2A_LVDS_19_P
165	I/O	B5_DIO23_N	B2A_LVDS_5_N	166	I/O	B4_IO36	B2A_LVDS_13_N
167	I/O	B5_DIO23_P	B2A_LVDS_5_P	168	I/O	B4_IO22	B2A_LVDS_13_P
169	I/O	B5_DIO19_N	B2J_LVDS_10_N	170	I/O	B4_IO23	B2A_LVDS_24_N
171	I/O	B5_DIO19_P	B2J_LVDS_10_P	172	I/O	B4_IO24	B2A_LVDS_24_P
173	I/O	B5_IO37	B2A_LVDS_9_P	174	I/O	B5_IO5_RDN3	B2A_LVDS_21_N
175	I/O	B5_IO23	B2A_LVDS_9_N	176	I/O	B5_IO44	B2A_LVDS_21_P
177	Power	GND	GND	178	Power	GND	GND
179	I/O	B6_IO6_VREFB6N1	B2A_LVDS_12_P	180	I/O	B8_IO_PLL3_CLKOUT_P	B2A_LVDS_3_N
181	I/O	B6_IO25_VREFB6N0	B2A_LVDS_12_N	182	I/O	B8_IO_PLL3_CLKOUT_N	B2A_LVDS_3_P
183	I/O	B6_IO8	B2A_LVDS_11_N	184	I/O	B8_IO30	B2A_LVDS_15_P
185	I/O	B6_IO40	B2A_LVDS_11_P	186	I/O	B8_IO27	B2A_LVDS_15_N
187	I/O	B6_DIO17_P	B2A_LVDS_8_P	188	I/O	B8_IO24	B2J_LVDS_13_N
189	I/O	B6_DIO17_N	B2A_LVDS_8_N	190	I/O	B8_IO23	B2J_LVDS_13_P

191	I/O	B6_DIO16_P	B2A_LVDS_7_P	192	I/O	B8_DIO8	B2J_LVDS_15_N
193	I/O	B6_DIO16_N	B2A_LVDS_7_N	194	I/O	B8_IO2	B2J_LVDS_15_P
195	Power	GND	GND	196	Power	GND	GND
197	I/O	B6_DIFFCLK2_N	B2J_LVDS_18_P	198	I/O	B8_DIFFCLK4_P	B2J_LVDS_22_P
199	I/O	B6_DIFFCLK2_P	B2J_LVDS_18_N	200	I/O	B8_DIFFCLK4_N	B2J_LVDS_22_N
201	I/O	B6_DIO15_P	B2J_LVDS_16_N	202	I/O	B8_DIO6_P	B2A_LVDS_17_N
203	I/O	B6_DIO15_N	B2J_LVDS_16_P	204	I/O	B8_DIO6_N	B2A_LVDS_17_P
205	I/O	B6_DIO13_P	B2A_LVDS_20_P	206	I/O	B8_DIO14_P	B2A_LVDS_16_P
207	I/O	B6_DIO13_N	B2A_LVDS_20_N	208	I/O	B8_DIO14_N	B2A_LVDS_16_N
209	I/O	B6_DIO11_P	B2J_LVDS_23_N	210	I/O	B8_DIO13_P	B2J_LVDS_11_N
211	I/O	B6_DIO11_N	B2J_LVDS_23_P	212	I/O	B8_DIO13_N	B2J_LVDS_11_P
213	Power	GND	GND	214	Power	GND	GND
215	I/O	B6_DIO9_P	B2J_LVDS_12_P	216	I/O	B8_DIO12_P	B2A_LVDS_10_P
217	I/O	B6_DIO9_N	B2J_LVDS_12_N	218	I/O	B8_DIO12_N	B2A_LVDS_10_N
219	I/O	B6_DIO7_P	B2J_LVDS_3_N	220	I/O	B8_DIO9_P	B2J_LVDS_9_P
221	I/O	B6_DIO7_N	B2J_LVDS_3_P	222	I/O	B8_DIO9_N	B2J_LVDS_9_N
223	I/O	B6_DIO4_P	B2J_LVDS_7_N	224	I/O	B8_DIO11_P	B2A_LVDS_14_N
225	I/O	B6_DIO4_N	B2J_LVDS_7_P	226	I/O	B8_DIO11_N	B2A_LVDS_14_P
227	I/O	B6_DIO3_P	B2J_LVDS_2_N	228	I/O	B8_DIO10_P	B2J_LVDS_21_N
229	I/O	B6_DIO3_N	B2J_LVDS_2_P	230	I/O	B8_DIO10_N	B2J_LVDS_21_P
231	Power	GND	GND	232	Power	GND	GND
233	I/O	B6_DIO2_P	B2J_LVDS_19_P	234	I/O	B8_DIO1_P	B2A_LVDS_22_P
235	I/O	B6_DIO2_N	B2J_LVDS_19_N	236	I/O	B8_DIO1_N	B2A_LVDS_22_N
237	I/O	B6_DIO6_P	B2J_LVDS_14_N	238	I/O	B8_DIO5_P	B2J_LVDS_24_N
239	I/O	B6_DIO6_N	B2J_LVDS_14_P	240	I/O	B8_DIO5_N	B2J_LVDS_24_P
241	I/O	B6_DIO10_P	B2J_LVDS_18_N	242	I/O	B8_DIO3_P	B2J_LVDS_20_N
243	I/O	B6_DIO10_N	B2J_LVDS_18_P	244	I/O	B8_DIO3_N	B2J_LVDS_20_P
245	I/O	B6_DIO5_P	B2J_LVDS_17_N	246	I/O	B8_DIO2_P	B2J_LVDS_8_P
247	I/O	B6_DIO5_N	B2J_LVDS_17_P	248	I/O	B8_DIO2_N	B2J_LVDS_8_N
249 251	Power	GND	GND	250 252	Power	GND	GND
253	Power	NC	NC	254	Power	VCCIO6_8	NC
255		NC	NC	256			

257	I/O	NC	SCL_1V8	258	Analog	NC	ADC0
259	I/O	NC	SDA_1V8	260	Analog	NC	ADC1

Table 1: MitySOM-C10x Card-edge Pin-out

Table 1 Notes:

yellow highlighted entries show LVDS pair polarity swap (_P, _N) between C10L and C10G SOM types
VCCIO (Power type) for C10L SOM I/O banks is supplied by carrier board: range is between +1.2V and +3.3V
VCCIO for C10G SOM I/O banks is fixed at +1.8V
Refer to SOM datasheet(s) for additional notes.

Secondary (Samtec) Connector Set (C10G only)

The secondary 120-position connector set carries multi-gigabit transceiver (MGT) signals between the C10G SOM and the carrier board.
The C10L SOM does not support MGT signals and the secondary connector set described below is not populated.

Odd-numbered row				Even-numbered row			
Pin	**Type**	**C10G SOM Signal pair**	**polarity**	**Pin**	**Type**	**C10G SOM Signal pair**	**polarity**
1	MGT pair	GXB_1C_TX0_	N	2	Power	GND	
3			P	4			
5	Power	GND		6	MGT pair	GXB_1C_RX0_	N
7				8			P
9	MGT pair	GXB_1C_TX1_	N	10	Power	GND	
11			P	12			
13	Power	GND		14	MGT pair	GXB_1C_RX1_	N
15				16			P
17	MGT pair	GXB_1C_TX2_	N	18	Power	GND	
19			P	20			
21	Power	GND		22	MGT pair	GXB_1C_RX2_	N
23				24			P

25	MGT pair	GXB_1C_TX3_	N	26	Power	GND	
27			P	28			
29	Power	GND		30	MGT pair	GXB_1C_RX3_	N
31				32			P
33	MGT pair	GXB_1C_TX4_	N	34	Power	GND	
35			P	36			
37	Power	GND		38	MGT pair	GXB_1C_RX4_	N
39				40			P
41	MGT pair	GXB_1C_TX5_	N	42	Power	GND	
43			P	44			
45	Power	GND		46	MGT pair	GXB_1C_RX5_	N
47				48			P
49	MGT pair	GXB_1D_TX0_	N	50	Power	GND	
51			P	52			
53	Power	GND		54	MGT pair	GXB_1D_RX0_	N
55				56			P
57	MGT pair	GXB_1D_TX1_	N	58	Power	GND	
59			P	60			
61	Power	GND		62	MGT pair	GXB_1D_RX1_	N
63				64			P
65	MGT pair	GXB_1D_TX2_	N	66	Power	GND	
67			P	68			
69	Power	GND		70	MGT pair	GXB_1D_RX2_	N
71				72			P
73	MGT pair	GXB_1D_TX3_	N	74	Power	GND	
75			P	76			
77	Power	GND		78	MGT pair	GXB_1D_RX3_	N
79				80			P
81	MGT pair	GXB_1D_TX4_	N	82	Power	GND	
83			P	84			
85	Power	GND		86	MGT pair	GXB_1D_RX4_	N
87				88			P

89 91	MGT pair	GXB_1D_TX5_	N P	90 92	Power	GND	
93 95	Power	GND		94 96	MGT pair	GXB_1D_RX5_	N P
97 99	MGT pair	REFCLK_1C_BOT_	P N	98 100	Power	GND	
101 103	Power	GND		102 104	MGT pair	REFCLK_1D_BOT_	P N
105 107	MGT pair	REFCLK_1C_TOP_	P N	106 108	Power	GND	
109 111	Power	GND		110 112	MGT pair	REFCLK_1D_TOP_	P N
113 115 117 119	reserved	N/C		114 116 118 120	reserved	N/C	

Table 2: MitySOM-C10G Secondary Connector

3 Electrical Requirements

The following sections describe the various electrical requirements for the MitySOM-C10x modules.

3.1 Power Interface

Input Power Specification

MitySOM-C10x modules are powered from the Carrier Board via the card-edge connector as described below :

- +5.0 VDC ± 3% supply connects to the SOM's +5VIN pins. This is used to power on-board supplies outputting +1.2V, +1.8V, +2.5V and +3.3V to supply the C10x FPGA core, on-board memory and other peripherals. FPGA Bank I/O voltage is generated on the C10G SOM; see next paragraph for FPGA Bank I/O for the C10L SOM.
- FPGA Bank I/O voltages for the C10L SOM connect to the VCCIO_XX pins. There are 3 sets of bank voltages: Banks 2 & 3, 4 & 5, 6 & 8. These bank I/O voltages are sourced from active sources on the carrier board (+1.2, +1.8, +2.5 or +3.3 VDC). Bulk decoupling capacitance must be provided for these supplies on the carrier board.

See Table 7 of the appropriate MitySOM-C10x SOM datasheet for input power specifications.

SOM Power Control, Status, Reset, FPGA Config/Done

MitySOM-C10x modules require no external power sequencing control; supply management is performed on the SOM to support proper power sequencing of the on-board DDR3 and FPGA core voltages.

A POWER_GOOD status signal is provided to the carrier board interface on pin 21 of the card-edge connector to indicate when SOM on-board power supplies are operating within specifications. POWER_GOOD is a +5V logic level signal, active high.

A CONF_DONE status signal from the SOM indicates when the C10x FPGA has completed its configuration process. CONF_DONE is provided to the carrier board interface on pin 24 of the card-edge connector. The logic level is determined by FPGA I/O Bank 6 & 8 voltage for the C10L SOM and is a +1.8V level logic signal for the C10G SOM. The carrier board designer may find this signal to be useful as a control for enabling tri-state buffers, transceivers or other devices which connect to FPGA I/O.

An NCONFIG input on pin 23 of the card-edge connector allows the carrier board to initiate FPGA configuration by pulling this signal to GND. NCONFIG is pulled up to +1.8V on the C10G SOM and to VCCIO6_8 on the C10L SOM.

For the C10G SOM only, an active low external reset may be provided to the SOM from the carrier board on pin 15 of the card-edge connector. This may be useful when connected to a push-button reset which makes a connection to circuit ground (GND). The C10L SOM does not support an external reset input.

Carrier Board Power and Control

The carrier board is responsible for sourcing a +5V power source to the SOM and sources for FPGA Bank I/O voltages. See Figure 8 for a block diagram of a typical power section for a carrier board designed to support the MitySOM-C10x.

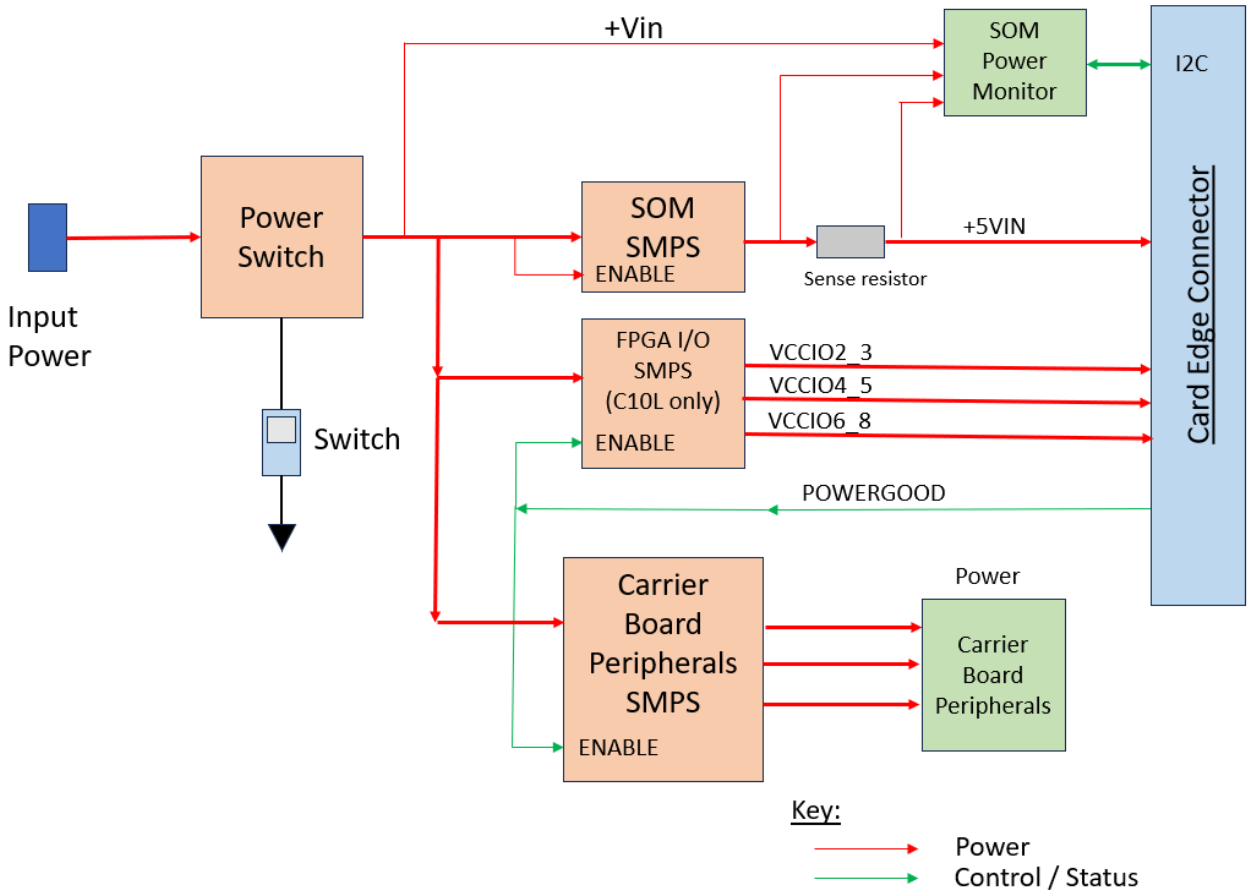

Figure 4: Carrier Board Power Section Block Diagram

Features of Carrier Board Power Section (refer to Figure 4 above):

- Input power, such as +12 VDC, is provided from an external source via a power jack or header, as shown in Figure 4.
- An optional power on/off switch circuit allows power to be removed from the carrier board and SOM without unplugging the external power source.
- As shown, DC-DC converters, or switched mode power supplies (SMPS) are typically used to source power for the SOM, FPGA Bank I/O and peripheral devices.
    - The SMPS sourcing +5V to the SOM is enabled when (switched) input power is applied.
    - FPGA Bank I/O (VCCIO_xx) for C10L SOM is sourced from the carrier board.
    - Other SMPS circuits are enabled by the POWERGOOD signal from the SOM. Using POWERGOOD to enable the peripheral device power ensures that the has completed its

power-up sequence before the carrier board powers up signals which interface with SOM I/O.

- A SOM power monitor (shown) and voltage monitor for other DC voltages (not shown), readable by the SOM over a digital serial interface like I^2C, is optional, but recommended, especially during early stage development.

SOM power usage is highly dependent on the user's application. It is advisable to over-design the capacity of power supply sourcing +5VIN for early stage/prototype development, then optimize the size of the power source circuitry according to the application / end user needs during later stages of development.

3.2 Recommended Capacitance

All MitySOM-C10x family modules include some power supply rail bypass capacitors on-board, however additional capacitance is recommended on the carrier board to minimize the ripple effect caused by changing load currents. It is recommended to place at least 20 µF in bulk capacitors nearby the main +5V supply pins in addition to whatever bulk capacitance is recommended for the SOM +5V supply design. For each of the other power supplies on the carrier board, at least 10 µF in bulk capacitors is recommended. Please note that this is the minimum recommended amount of bulk capacitance, and more is typically better. SMPS controller device datasheets often specify amounts of bulk capacitance and recommend smaller decoupling capacitors placed around the board.

3.3 SOM I/O Interfaces

Voltage Domains

C10L SOM: Each of 3 FPGA I/O banks (64 I/O per bank) are powered by separate VCCIO inputs from the carrier board. See Figure 4 above for I/O bank voltage net names. The range of each VCCIO is +1.2 to +3.3 V.

C10G SOM: The 4 FPGA I/O Banks (48 I/O per bank) are powered by +1.8V sourced on the SOM. A bank reference voltage (for high-speed transceivers) of 0.9 V is also sourced on the SOM.

Protection

I/O signals which interface external to the SOM+Carrier board set must be protected to ensure that no out-of-range voltage conditions occur on all I/O pins which direct connect to the C10x FPGA. The carrier board should contain the necessary protection/isolation circuits as required for overvoltage, surge and ESD protection. Please refer to the Intel C10LP or C10GX datasheets for details about maximum voltage ranges for I/O domains as the maximum ranges are different.

3.4 FPGA Configuration / FLASH Programming

The MitySOM-C10x is set up to load the FPGA from an on-board FLASH device. This on-board FLASH device is blank when delivered from Critical Link or its distributors. Programming of the configuration FLASH device requires access to a JTAG port via the carrier board. The JTAG interface consists of 4 signals (TMS, TCK, TDI, TDO) and power/ground for the JTAG pod. JTAG programming pods interface to a host computer over USB or other interfaces and also to the target board (carrier board). There is a variety of pod-to-target board interfaces. See below for carrier board connector type and connection recommendations for Intel and Xilinx JTAG pods.

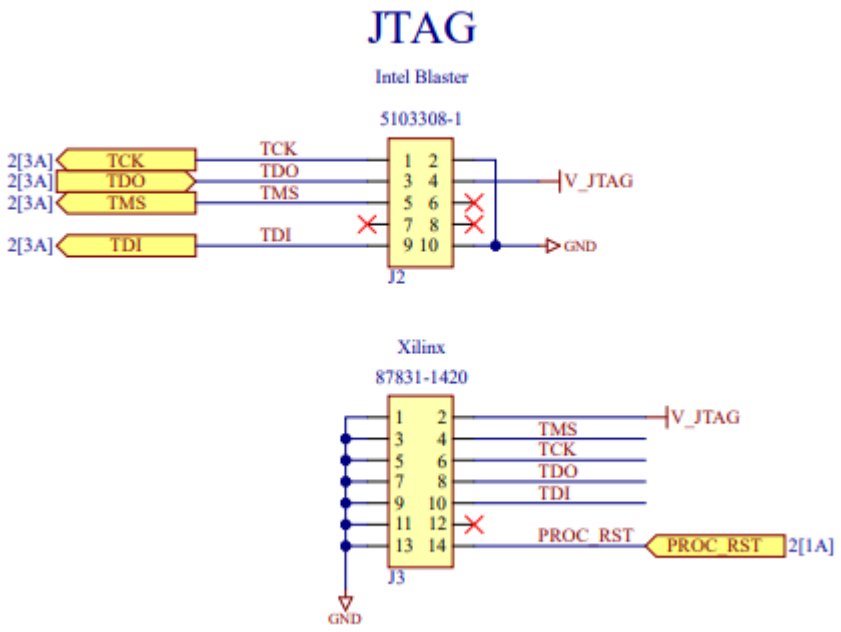

Figure 5. Carrier Board JTAG Port: Intel and Xilinx types

A JTAG programming pod and QUARTUS Programmer GUI utility running on a host computer are used to program an FPGA bitstream image into on-board FLASH using the JTAG interface.

Alternately, if support for a JTAG interface is not desired on the carrier board, configuration FLASH may be programmed using a separate programming station prior to the SOM being installed onto the carrier board. A Critical Link C10x Development Kit is suitable for use as a SOM programming station.

3.5 Multi-gigabit Transceivers (C10G SOM only)

On the MitySOM-C10G module, multi-gigabit transceiver (MGT) signal pairs interface viathe secondary Samtec connector set to the carrier board. It is recommended that the carrier board implement in-line capacitors on the TX pairs, as illustrated in Figure 7 below. (J10 is the carrier board side of the Samtec connector set.)

Matched length attributes for each MGT signal pair are also recommended for the carrier board PCB design.

For reference clock signal pairs sourced on the carrier board, a low-skew clock buffer is recommended. See Figure 6 for an example of a clock buffer device which may be configured via I^2C interface.

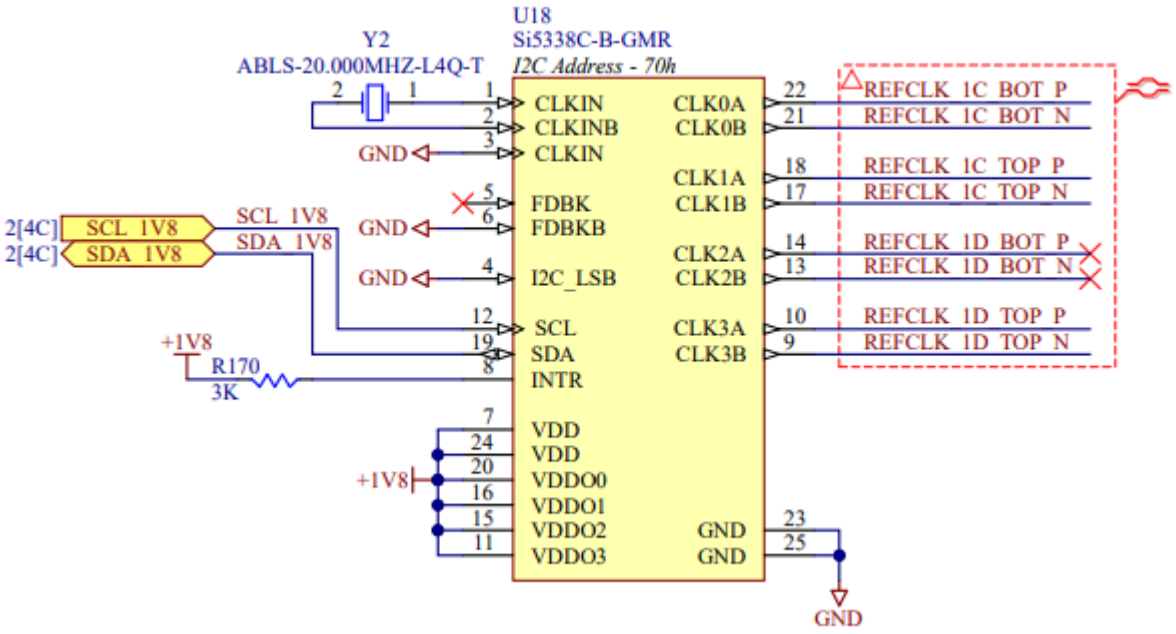

Figure 6. Carrier Board Example: MGT Reference Clock Buffer

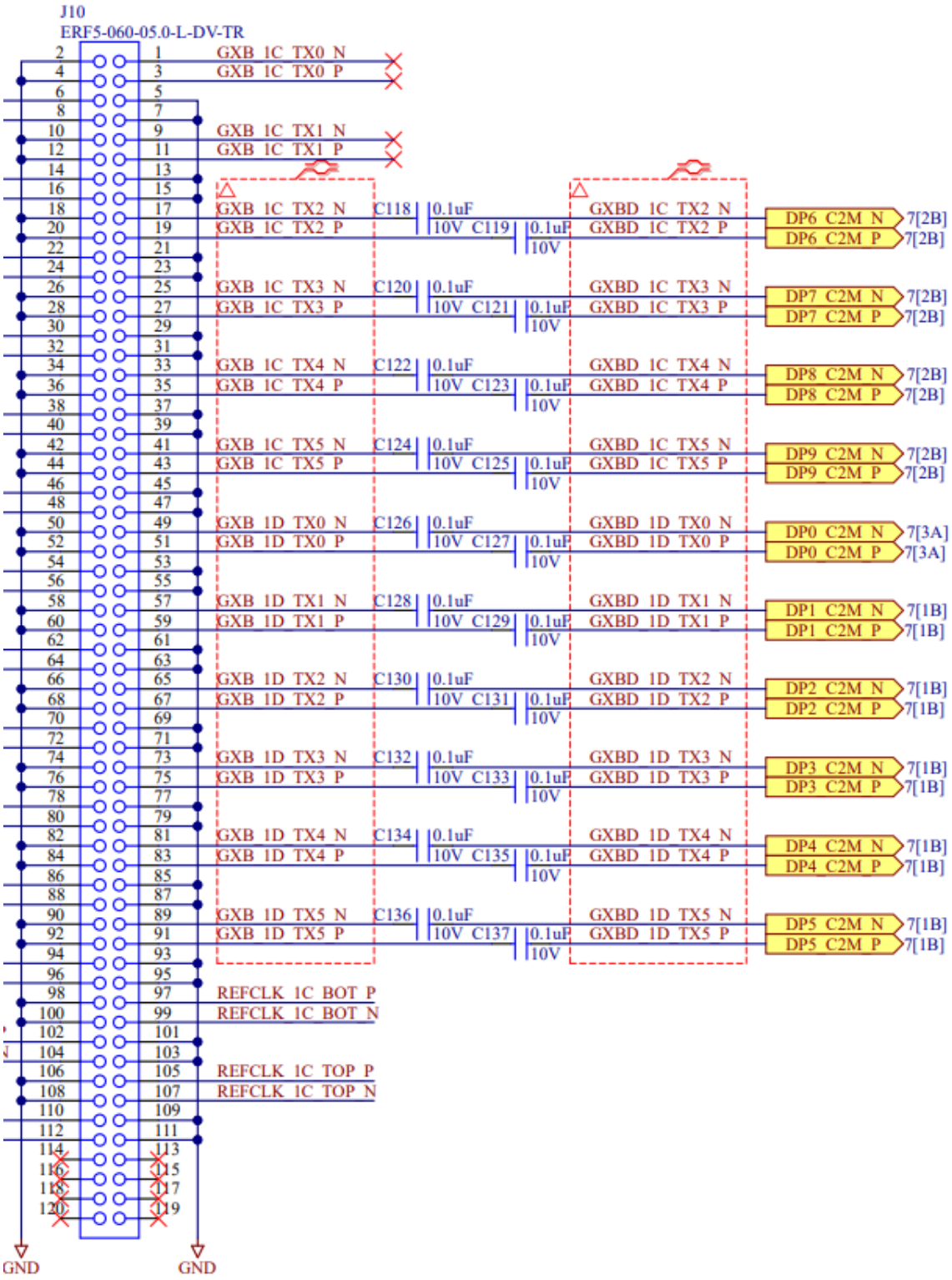

Figure 7. Carrier Board example: insert in-line capacitors on MGT TX pairs

Note: Pins 1, 3, 9, 11 shown as no connects; this applies to Development Board design.
User's carrier board design may use these MGT TX pairs. See Table 2 for secondary connector pin-out.

4 Peripheral Interface Examples

The sections below provide examples of peripheral interfaces which may be useful available to the MitySOM-C10x Carrier Board designer. Since a C10x SOM is FPGA-based, the peripheral possibilities are numerous. The Cyclone10 FPGA series do not include direct-connect capabilities for common interfaces like USB, Ethernet, or UARTs, but FPGA IP modules combined with interface transceivers may be utilized to emulate many features found on System-On-Chip devices which include microprocessors and support for common peripherals.

Some examples below reference the C10x Development Kit board. For assistance with integrating other interfaces or peripherals, please reach out to Critical Link for guidance. Altium Designer files from Critical Link may be available on request.

4.1 Serial UARTs

Universal Asynchronous Receive/Transmit (UART) ports are recommended during development to stream console data to a software / firmware development system.

Figure 8 below shows a UART-to-USB converter, which allows for a serial connection via a common USB cable to a USB port on a remote computer. This is often preferable to an RS-232 interface over a D-sub 9-pin connector due to the prevalence of USB ports and absence of RS-232 ports on modern laptop computers. In the example below, the USB transceiver (U2) is powered at VCC (pin 12) by VBUS (+5V) sourced from an external host computer.

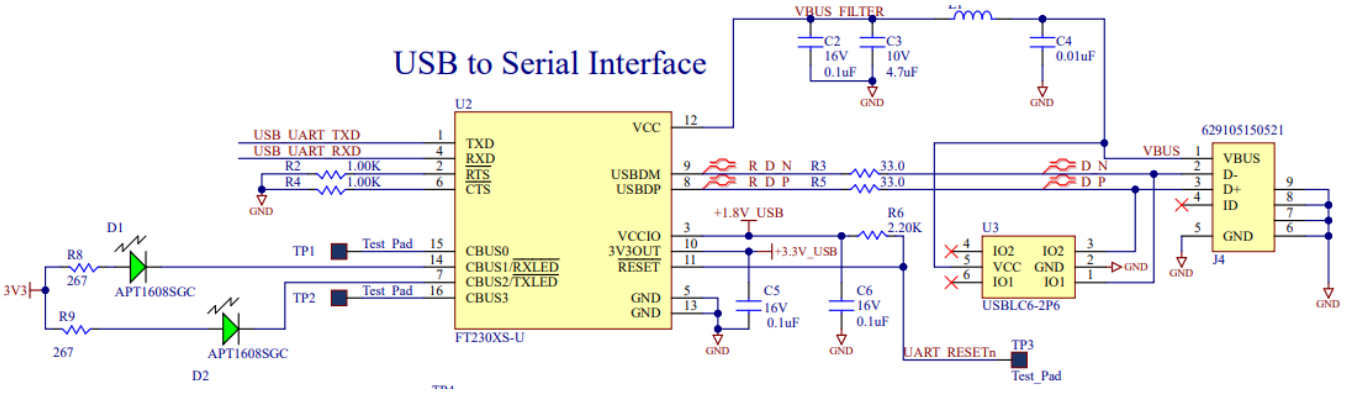

Figure 8. Carrier Board example: UART-to-USB serial port

4.2 10/100/1000 Ethernet

An example of a Gigabit-capable Ethernet uses reduced gigabit media independent interfaces (RGMII) to connect to a physical interface (PHY) device. 10/100 MB Ethernet uses reduced media independent interfaces (RMII). Critical Link's C10x Development Board includes a reference design for a 10/100/1000 device. See Figure 9 for primary connections to a Microchip KSZ9131 PHY device and RJ-45 jack with integrated magnetics and LEDs.

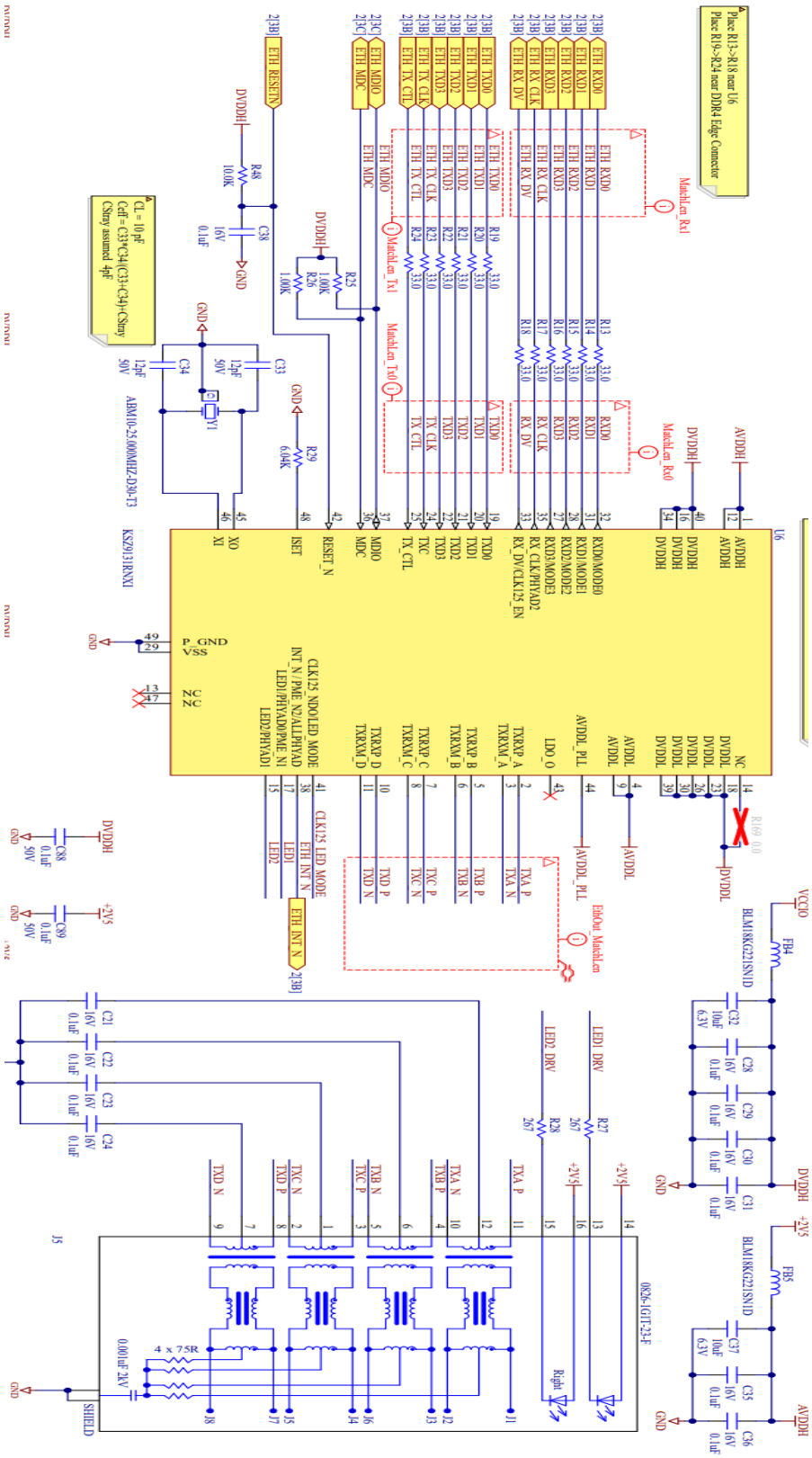

Figure 9. Carrier Board example: 10/100/1000 Ethernet

4.3 C10x Reserved I/O

Not all available FPGA I/O pads are available to the application design at the carrier board interface. Some FPGA I/O are reserved on the SOM for connections to on-board LEDs, serial FLASH, SRAM or DDR RAM, EEPROM and other reference/calibration/test points. See the datasheets for the MitySOM-C10L and MitySOM-C10G for FPGA pads which are reserved. The FPGA design constraints must avoid using these reserved I/O pads.

5 Mechanical Requirements

The following sections describe some of the mechanical requirements of incorporating a MitySOM-C10x module in a carrier board design. See also sections 1.4 and 1.5 of this document which describe the SOM dimensions, connector set and placement requirements.

5.1 Module Clearance

As described elsewhere in this document, all C10x SOM types use an SO-DIMM DDR4-style card edge mated to a receptacle on the carrier board for the primary electrical and mechanical attachment to the carrier board. A secondary 120-position high density Samtec connector set provides additional I/O for the C10G SOM, locking the SOM into position. This connector set positions the SOM parallel to the carrier board, and as such there is limited clearance between the SOM and the carrier board. Therefore, avoid placing high-profile carrier board components underneath the SOM. However, it is possible to utilize most of this space for low-profile components. Please refer to Figure 10 for under-SOM vertical headroom.

A STEP model and an Altium Designer footprint of the SOM is available from the Critical Link support site, and users are encouraged to verify clearance if making use of the space under the module.

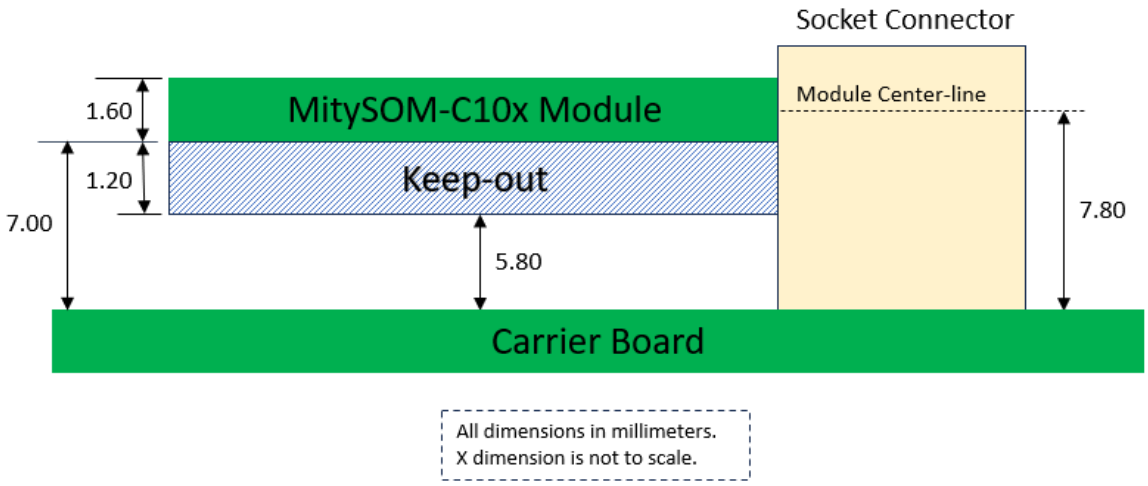

Figure 10: MitySOM-C10x Module Clearance - Side View (card-edge receptacle shown)

5.2 Mounting Methods

The modules feature an additional optional mechanical attachment method. A hard mechanical attachment by board-to-board standoffs and screw hardware may be used to mount the module. The corners of the free-floating edge of the SOMs feature mounting holes that are compatible with M3 size mounting hardware. The mechanical drawing in Figure 11 below illustrates the mechanical requirements of this optional attachment method.

Suggested standoff part (on carrier board): Würth Electronik 971070354 or equivalent.

Description: Hex spacer stud with metric thread internal/external, M3 threads X 5.00 hex faces X 7.00 H, 3.175 (0.125") hole, 6.75 (0.266") pad diam.

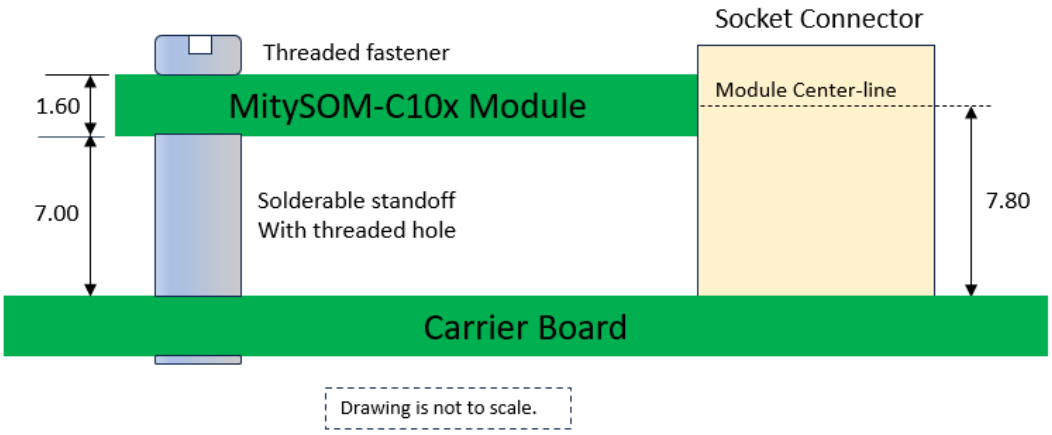

Figure 11: 7.0 mm height standoff mounting: side view (card-edge receptacle shown)

5.3 Shock & Vibration

For customers who are interested in using MitySOM-C10x modules in rugged environments, the mounting attachment method discussed in section 5.2 above enable these SOMs to tolerate much greater mechanical shock and vibration forces than without any additional mounting support.

5.4 Thermal Management

The MitySOM-C10x family of SOMs have no specific requirements regarding thermal management. Depending on clock speeds, number of logic elements (percentage of FPGA fabric) and peripherals in use, a C10x SOM may be operated without heat sinks or air flow, and inside tight enclosures. Customer qualification and testing of SOM device temperatures in the end application is highly recommended. Monitoring the SOM temperature during product development using thermocouples or infrared camera is recommended. It may be necessary or prudent to add thermal management devices to the SOM and/or enclosure or lower the operating temperature specification of the end product.

6 Board Layout Recommendations

The following sections discuss topics for successful board layouts incorporating any module.

6.1 Placement

Placement of the module site is crucial to a successful carrier board layout. Because the module connector footprint is fine-pitch and dual-row, it is generally best to place the connector fairly centered in the overall board layout. This placement allows traces to be routed out from both sides of the connector, using mainly top-side copper tracks. The use of less signal layers, and therefore less vias, generally results in a more compact design with better signal integrity than a board using many layers and vias. Of course, central placement is not always possible because of other mechanical constraints.

Mechanically, enough space must be allocated for the full extension of the module. Although it is possible for a module to hang over the edge of its carrier board, this may not be desirable if additional mechanical attachment methods are desired for ruggedness, as discussed in section 5.2. Another thing to keep in mind with placement on the carrier board and in enclosures is the cam-in action of the MitySOM modules into their respective sockets. The modules are generally installed at an angle of about 25° to 30° before swinging down to locked position. Enclosure designs should accommodate this motion.

6.2 Pin-out and Routing

Care must be taken when routing the MitySOM-C10x high speed interfaces – specifically differential pairs, matched length signals, LVDS signals, signals with controlled impedance requirements, clock lines and gigabit Ethernet PHY signals, where applicable. Please refer to the FPGA and peripheral device datasheet or application notes for guidance related to PCB layout.

6.3 Access issues

Given that it is possible and often desirable to make best use of available space by placing components underneath the MitySOM-C10x module (refer to section 5.1), hardware and software engineers who will be debugging code on the platform could find themselves in a tough situation if the component they need to access is blocked by the installed MitySOM-C10x module. Because of these situations it is advisable to either not use the space under the MitySOM-C10x module for active components that might need live probing with the SOM installed, or only place circuits there that are already tried and tested by engineers on other platforms. If an obscured circuit does need to be probed, it may be necessary to solder temporary wires onto probe points. An even better solution would be to design the board with bottom-side test points, at least in the vicinity of the SOM, when possible, on a given design.

6.4 PCB/PCA Technology

The MitySOM-C10x modules do not have any specific requirements about the PCB technology used for a carrier board. The required socket connectors are available as RoHS compliant and may be used in both leaded and lead-free assembly processes. The only recommendation is to fabricate the carrier board thick enough to rigidly support the MitySOM-C10x card-edge receptacle connector. In practice, FR-4 with a common finished thickness of 0.062 inches is adequate for all types of MitySOM-C10x modules.

6.5 PCB Footprints

Figures 12 and 13 show the recommended PCB footprint for the TE Connectivity 2309413-1 card edge receptacle and the Samtec ERF5-060-05.0-L-DV-TR secondary “Hi-Speed” connector. The figures are copied directly from the part drawing. Carrier board designers are advised to check with manufacturers and distributors for the latest versions, application notes or product change notices.

Altium Designer footprints for the MitySOM-C10x modules are available from Critical Link on request for Altium users.

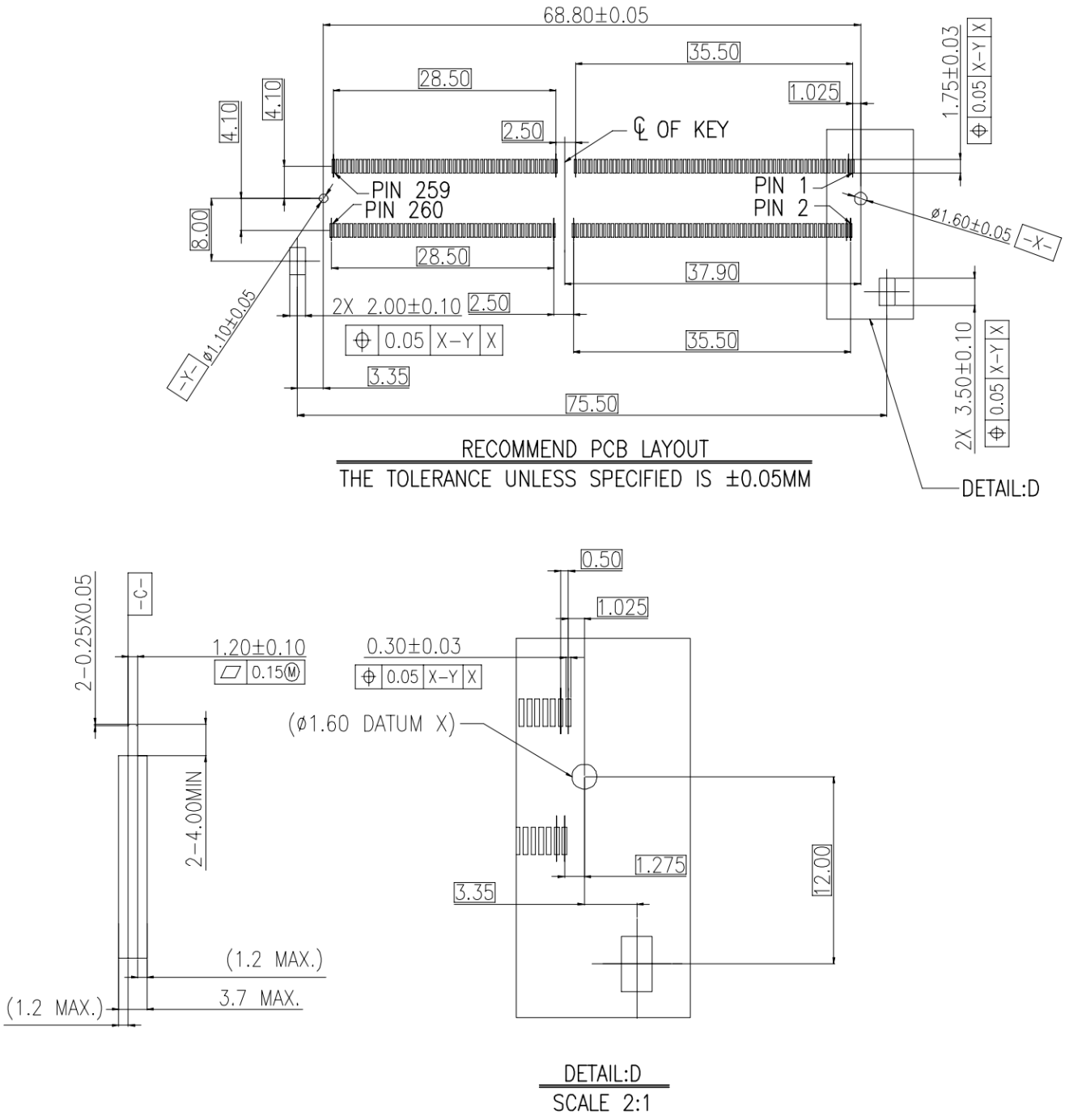

Figure 12: TE Connectivity 2309413-1 Recommended PCB Footprint

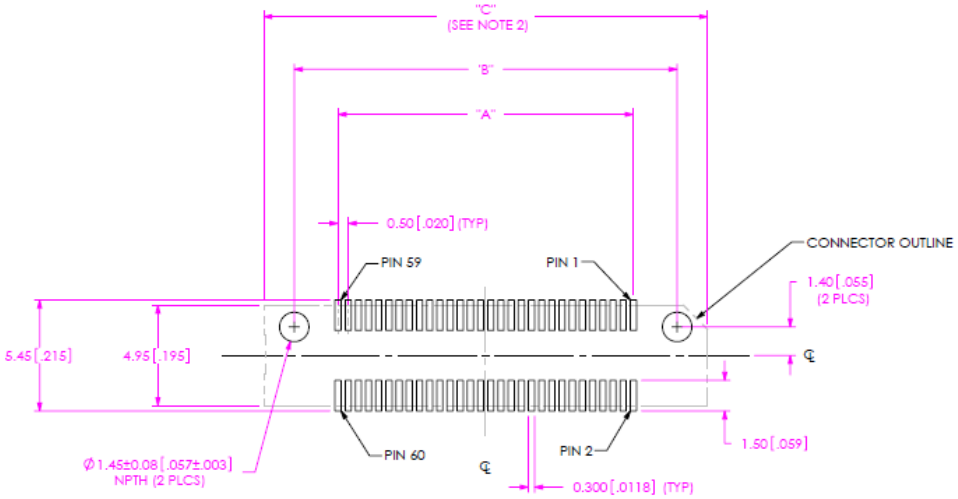

FIG 1
-030 POSITION SHOWN

NOTES:
1. ALL DIMENSIONS ARE SYMMETRIC ABOUT THE CENTERLINE, EXCEPT AS SHOWN.
2. CONNECTOR ENELOPE DIMENSIONS. OTHER COMPONENTS PLACED ON PCB SHALL AVOID THIS ZONE.

TABLE 1

POSITION	"A"	"B"	"C"
-005	2.00 [0.079]	6.30 [0.248]	9.30 [0.366]
-010	4.50 [0.177]	8.80 [0.346]	11.80 [0.465]
-020	9.50 [0.374]	13.80 [0.543]	16.80 [0.661]
-030	14.50 [0.571]	18.80 [0.740]	21.80 [0.858]
-040	19.50 [0.768]	23.80 [0.937]	26.80 [1.055]
-050	24.50 [0.965]	28.80 [1.134]	31.80 [1.252]
-060	29.50 [1.161]	33.80 [1.330]	36.80 [1.449]
-070	34.50 [1.358]	38.80 [1.527]	41.80 [1.646]
-075	37.00 [1.457]	41.30 [1.626]	44.30 [1.744]

Figure 13: Samtec ERF5-060-05.0-L-DV-TR Recommended PCB Footprint

(Note: 2x30 connector shown; adjust per Table 1 for 2x60 connector)

7 Revision History

Revision	Date	Description of Changes
1.0	10-May-2024	Initial Revision
1.1	17-September-2024	Correct pin-out of even # pins 2-24 on secondary Samtec connector; add note to Figure 7, update Rev. to 1.1