FEATURES

MitySOM-C10x Development Board:
C10G variant 80-001695RH

MitySOM-C10G SoM Module

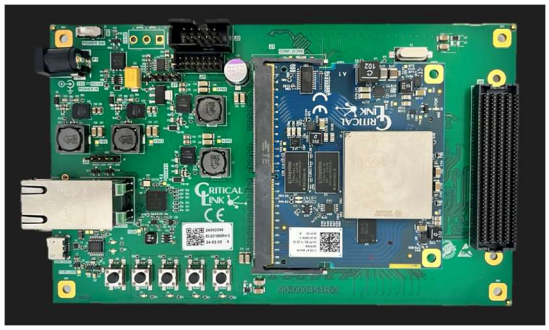
Integrated +5V/+3.3V/+2.5V/1.8V Power Supplies

Digital Interfaces:

- 10/100/1000 Mb Ethernet Interface
- Debug UART to USB
- USB-Blaster JTAG Port
- FMC Low Pin Count Interface
- 5 Pushbuttons
- 4 LEDs.

Expansion

- 400 Pin FPGA Mezzanine Card Low Pin Count (FMC LPC)
- 2x60 pin Expansion Headers



Software and Documentation

- Reference Quartus Project
- Reference QSPI Flash Image
- Development Board Schematics
- Development Board Gerber Files
- Development Board BOM

APPLICATIONS

- MitySOM-C10G Evaluation
- Test and Measurement
- Factory Automation
- Industrial Automation
- Embedded Instrumentation
- Test and Measurement
- Rapid Prototyping

DESCRIPTION

The MitySOM-C10G Development Kit provides all the hardware and software support for system designers and developers to evaluate the Critical Link MitySOM-C10G System on Module. The MitySOM-C10G Development Kit comes complete with a MitySOM-C10G module that meets your project's needs.

The MitySOM-C10G Development Kit includes on-board Debug UART to USB converter and 10/100/1000 Gb Ethernet communication interfaces, FMC LPC connector that is compatible with a wide range of existing add-on cards, and two 60 pin dual row connectors that provide additional IO expansion options. All powered from a single 12VDC input (adapter included) with onboard +3.3V/+5V/2.5V/1.8V power supplies.

A block diagram of the MitySOM-C10G Development Kit is illustrated in Figure 1. Control of the on-board interface hardware and connected Expansion IO cards require proper configuration of the MitySOM-C10G module.

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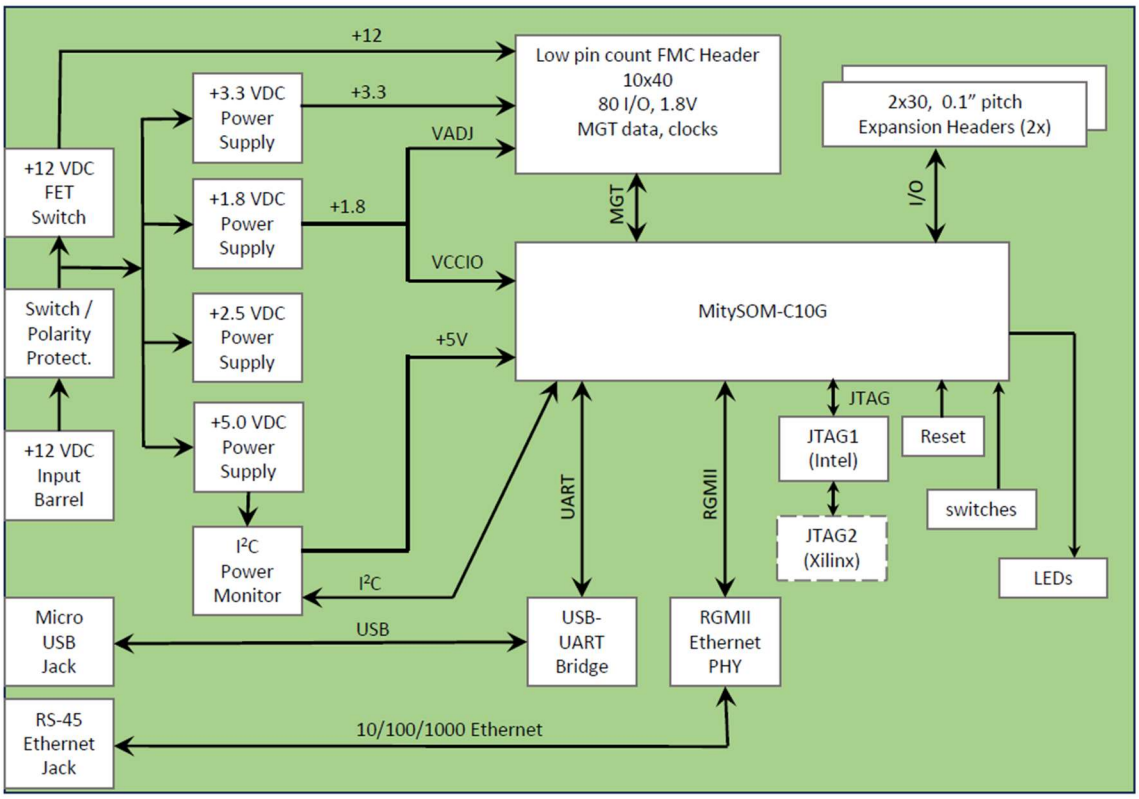

Figure 1: MitySOM-C10G Development Kit Block Diagram

Additional details about the Cyclone 10 GX FPGA, available peripheral IP, its features and FPGA IO details are provided in the data sheet at the Intel website.

> Intel document: C10GX51001, ID: 683485, version 2019.04.01
> https://www.intel.com/content/www/us/en/docs/programmable/683485/current/device-overview.html

Feature Descriptions

Electrical Interface Descriptions

Debug UART to USB Interface Description

The on-board UART to USB Bridge, FTDI FT230X, provides a serial interface at data rates up to 115,200 baud. The USB serial interface, J4 - Console, is routed to the MitySOM-C10G general IO pins. It allows for general module debug and console interaction if a NIOS soft core is instantiated in the FPGA.

When connected to a Windows PC no drivers are required as Windows Update is used to obtain the drivers.

Intel USB-Blaster JTAG Interface

To support programming the MitySOM-C10G, the C10G Development Kit includes J2, which is a USB-Blaster compatible interface. J3 is a reserved connector.

Gigabit Ethernet Interface Description

The on-board Ethernet interface features a Micrel KSZ9131 Ethernet PHY capable of running at 10/100/1000Mbit including link auto-negotiation and RGMII/MDIO capability. An industry standard RJ-45 connector, J5, is provided for external connection. This PHY and MDIO interface is connected to general IO pins on the Cyclone 10GX FPGA of the MitySOM-C10G.

FMC LPC Interface Description

The FPGA Mezzanine Card Low Pin Count (FMC LPC) interface, J6, allows for the use of add-on cards that are designed for the Intel Cyclone 10GX FPGA on the MitySOM-C10G module. Several “off the shelf” boards/kits are available from third parties that are compatible with this interface.

Dual Row 60 pin expansion Interface Description

Two 60 pin female 0.1” dual row headers, P2 and P3, are available for developing expansion interfaces and are connected to the VCCIO power, system +5V, and spare FPGA IO pins of the MitySOM-C10G module.

Reconfigure Switch Description

The C10G Development Kit has a cold reset button that can be used to reconfigure the Intel Cyclone 10GX FPGA from on-board QSPI Flash (if programmed). This button is located at S1.

General Switch Description

The C10G Development Kit includes 4 general purpose normally open push button inputs connected to the Cyclone 10GX FPGA on the SOM. These are switches S2, S3, S4, and S5.

User LEDs

The C10G Development Kit includes 4 general purpose LEDs connected to the Cyclone 10GX FPGA on the SOM. These are LEDs D3, D4, D5, and D6.

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IO voltage Select Switch Description

Important Note: VCCIO Voltage selector switch S7 is not installed on the C10G variant of the Development Kit. VCCIO = +1.8V to the MitySOM-C10GX FPGA bank IO pins.

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact Critical Link at info@criticallink.com.

Table 1: Absolute Maximums

Parameter	Min	Max	Units
Operating Supply Voltage	10.8	13.2	V
Operating Temperature for MitySOM-C10G/Baseboard	0	70	C
Operating Temperature for AC to DC Power Supply	0	50	C
Storage Temperature	-40	85	C
Humidity	0	95	% Non-condensing

ELECTRICAL CHARACTERISTICS

Table 2: Electrical Characteristics

Symbol	Parameter	Conditions	Typical	Limit	Units (Limits)
Maximum Power Supply Output					
I_{Max}	12V Supply (AC Adapter) all components			5.0	A
I_{Max}	12.0V Supply[1] for external components			1.0	A
I_{Max}	3.3V Supply[1] for external components			2.0	A
I_{Max}	1.8V Supply[1] for external components			4.0	A
Power Dissipation					
V_S	Supply Voltage		12±5%		V
I_S	Supply Current[2]		800		mA

Notes:

1. The maximum current supplied to external components should be limited to the specified maximum for all externally connected power supplies
2. FMC cards not attached, FPGA programmed, RS-232 and Ethernet are enabled and active.

ELECTRICAL INTERFACE DESCRIPTIONS

Input Power – P1

The MitySOM-C10G Development Kit power interface, P1, requires a single +12Volt power supply. An input supply rating of at least 3A is recommended.

Table 3: Input Power Interface Pin Description

Signal	P1 Position
+12V	1
GND	2

Main Power Switch – S6

An input power switch is present on the Development Kit, S6, which controls the power input to the development kit, including the module, on or off, from P1.

FPGA IO Bank Voltage Power Switch – S7

S7 is not installed on the C10G variant of the Development Kit; it is bypassed with a jumper at R80. VCCIO = +1.8V

Push Button Switches (S1-S5)

The MitySOM-C10G Development Kit includes 5 debounced normally open push buttons connected to the MitySOM-C10G FPGA according to Table 4. When activated, these buttons will connect the reference signal to ground. When released, these signals are pulled high to VCCIO.

Table 4 Push Button Functions

Switch ID	Dev Kit Signal	SoM J1 pin	C10GX FPGA Ball
S1	nCONFIG	23	AC8
S2	SW_1	88	C17
S3	SW_2	90	C16
S4	SW_3	92	E15
S5	SW_4	94	D15

Debug LED Interface (D3 - D6)

The MitySOM-C10G Development Kit includes 4 debug LEDs according to Table 5. The LED signal should be driven to GND / low to activate the LED. To disable the LED, drive the signal high or tri-state it.

Table 5 LED Interface

ID	Dev Kit Signal	SoM J1 pin	C10GX FPGA Ball
D3	LED_1	96	F22
D4	LED_2	98	E22
D5	LED_3	100	F21
D6	LED_4	102	G21

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USB-Blaster JTAG Interface – J2

The USB-Blaster interface pin out for J2 is shown in Table 6 below.

Table 6 J2 USB Blaster JTAG Interface

J2-Pin	Dev Kit Signal	SoM J1 pin	C10GX FPGA Ball
1	TCK	20	Y9
2	GND	-	-
3	TDO	18	W10
4	V_JTAG	19	+1.8V
5	TMS	22	AH6
6	N/C	-	-
7	N/C	-	-
8	N/C	-	-
9	TDI	16	AC10
10	GND	-	-

Debug/Boot UART to USB Interface – J4

The Micro-USB pin out for J4 is shown in Table 7 below.

Table 7: J4 Micro USB Connector Pin Assignments

Pin	Signal	Type	Standard	Notes
1	VBUS	Power	-	
2	D-	I/O	USB 2.0	USB data minus line
3	D+	I/O	USB 2.0	USB data plus line
4	GND	GND	-	
5	SHIELD	GND	-	

The FTDI FT230XS-U UART to USB controller, used to drive J4 on the Development Kit board is connected to general FPGA IO pins on the MitySOM-C10G, as shown in Table 8 below.

Table 8 USB Controller to UART Interface

FTD230XS Signal	Dev Kit Signal	SoM J1 pin	C10GX FPGA Ball
TXD	UART0_RX	74	D19
RXD	UART0_TX	76	D18
RTS#	No Connect	No Connect	
CTS#	No Connect – 1.1k to GND resistor	No Connect	

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Expansion Interface 1 – P2

Table 9 describes the pin-out of the P2 interface on the MitySOM-C10G development board. The I/O "type" is in reference to the signal direction from the SoM/development board or a power input pin.

Table 9: P2 Pin Assignments

P2 Pin	Dev Kit Signal	SoM J1 pin	C10GX FPGA Ball	Type	Notes and SoM Signal
1	GND	-	-	POWER	
2	VCCIO	-	-	POWER	Note 2
3	+5V	-	-	POWER	Note 1; JP3 installed
4	VCCIO	-	-	POWER	Note 2
5	GND	-	-	POWER	
6	GND	-	-	POWER	
7	EXT1_DIO1_N	83	B19	IO	B2K_LVDS_10_P
8	EXT1_DIO2_N	79	C15	IO	B2K_LVDS_9_N
9	EXT1_DIO1_P	81	B18	IO	B2K_LVDS_10_N
10	EXT1_DIO2_P	77	B16	IO	B2K_LVDS_9_P
11	EXT1_DIO3_N	75	F18	IO	B2L_DIFFIO_4_N
12	EXT1_DIO10_N	71	A12	IO	B2K_LVDS_23_P
13	EXT1_DIO3_P	73	F17	IO	B2L_DIFFIO_4_P
14	EXT1_DIO10_P	69	A13	IO	B2K_LVDS_23_N
15	EXT1_DIO11_N	63	A17	IO	B2K_LVDS_7_P
16	EXT1_DIO8_N	59	A19	IO	B2K_LVDS_8_P
17	EXT1_DIO11_P	65	A16	IO	B2K_LVDS_7_N
18	EXT1_DIO8_P	61	A18	IO	B2K_LVDS_8_N
19	EXT1_DIO9_N	55	A22	IO	B2K_LVDS_17_N
20	EXT1_DIO6_N	51	C20	IO	B2K_LVDS_11_N
21	EXT1_DIO9_P	57	A21	IO	B2K_LVDS_17_P
22	EXT1_DIO6_P	53	B20	IO	B2K_LVDS_11_P
23	EXT1_DIO7_N	47	A23	IO	B2K_LVDS_13_N
24	EXT1_DIO4_N	43	B21	IO	B2K_LVDS_14_P
25	EXT1_DIO7_P	45	A24	IO	B2K_LVDS_13_P
26	EXT1_DIO4_P	41	C21	IO	B2K_LVDS_14_N
27	EXT1_DIO5_P	37	B24	IO	B2K_LVDS_15_P
28	EXT1_CLK0_N	35	A26	I	B2K_LVDS_16_N
29	EXT1_DIO5_N	39	B23	IO	B2K_LVDS_15_N
30	EXT1_CLK0_P	33	A27	I	B2K_LVDS_16_P
31	EXT1_DIO25	128	K19	IO	B2L_DIFFIO_17_P
32	EXT1_DIO23	130	K20	IO	B2L_DIFFIO_17_N
33	EXT1_DIO26	124	J17	IO	B2L_DIFFIO_3_P
34	EXT1_DIO24	126	K17	IO	B2L_DIFFIO_3_N
35	EXT1_DIO29	118	K23	IO	B2L_DIFFIO_18_P
36	EXT1_DIO27	120	K22	IO	B2L_DIFFIO_18_N
37	EXT1_DIO30	114	B9	IO	B2K_LVDS_1_P
38	EXT1_DIO28	116	B8	IO	B2K_LVDS_1_N
39	EXT1_DIO33	112	F19	IO	B2L_DIFFIO_21_N
40	EXT1_DIO31	38	H22	IO	B2L_DIFFIO_15_N
41	EXT1_DIO34	110	E19	IO	B2L_DIFFIO_21_P
42	EXT1_DIO32	40	H21	IO	B2L_DIFFIO_15_P
43	EXT1_DIO37	99	A14	IO	B2K_LVDS_22_P
44	EXT1_DIO35	101	B13	IO	B2K_LVDS_22_N
45	EXT1_DIO38	95	H20	IO	B2L_DIFFIO_16_P
46	EXT1_DIO36	97	H21	IO	B2L_DIFFIO_16_N
47	EXT1_DIO41	91	H17	IO	B2L_DIFFIO_1_P

P2 Pin	Dev Kit Signal	SoM J1 pin	C10GX FPGA Ball	Type	Notes and SoM Signal
48	EXT1_DIO39	93	H16	IO	B2L_DIFFIO_1_N
49	EXT1_DIO42	87	G18	IO	B2L_DIFFIO_5_P
50	EXT1_DIO40	89	H18	IO	B2L_DIFFIO_5_N
51	EXT1_CLK1_P	70	G23	I	B2L_DIFFIO_12_N
52	SCL	84	B14	IO	B2K_LVDS_21_P
53	EXT1_CLK1_N	72	F23	I	B2L_DIFFIO_12_P
54	SDA	82	B15	IO	B2K_LVDS_21_N
55	GND	-	-	POWER	
56	GND	-	-	POWER	
57	NC	-	-		
58	NC	-	-		
59	NC	-	-		
60	GND	-	-	POWER	

Notes:

1. The maximum total current supplied to external components from the +5.0V supply should be limited to less than 2.0A. The maximum current allowed per connector pin is 1A.
2. The maximum total current supplied to external components from the VCCIO supply should be limited to less than 1.0A. The maximum current allowed per connector pin is 1A.
3. P2 connector part number: Samtec SSM-130-F-DV

Expansion Interface 2 – P3

Table 10 describes the pin-out of the P3 interface on the MitySOM-C10L development board. The I/O "type" is in reference to the signal direction from the SoM/development board or a power pin.

Table 10: P3 Pin Assignments

P3 Pin	Dev Kit Signal	SoM J1 pin	C10GX FPGA Ball	Type	Notes and SoM Signal
1	GND	-	-	POWER	
2	VCCIO	-	-	POWER	Note 2
3	+5V	-	-	POWER	Note 1; JP4 installed
4	VCCIO	-	-	POWER	Note 2
5	GND	-	-	POWER	
6	GND	-	-	POWER	
7	EXT2_DIO11_N	248	W21	IO	B2J_LVDS_8_N
8	EXT2_DIO9_N	240	AD22	IO	B2J_LVDS_24_P
9	EXT2_DIO11_P	246	W20	IO	B2J_LVDS_8_P
10	EXT2_DIO9_P	238	AC22	IO	B2J_LVDS_24_N
11	EXT2_DIO10_N	244	AE23	IO	B2J_LVDS_20_P
12	EXT2_DIO7_N	230	AA23	IO	B2J_LVDS_21_P
13	EXT2_DIO10_P	242	AD23	IO	B2J_LVDS_20_N
14	EXT2_DIO7_P	228	AA22	IO	B2J_LVDS_21_N
15	EXT2_DIO8_N	236	AB13	IO	B2A_LVDS_22_N
16	EXT2_DIO5_N	222	AB19	IO	B2J_LVDS_9_N
17	EXT2_DIO8_P	234	AC13	IO	B2A_LVDS_22_P
18	EXT2_DIO5_P	220	AB18	IO	B2J_LVDS_9_P
19	EXT2_DIO6_N	226	AD20	IO	B2A_LVDS_14_P
20	EXT2_DIO3_N	212	Y20	IO	B2J_LVDS_11_P

P3 Pin	Dev Kit Signal	SoM J1 pin	C10GX FPGA Ball	Type	Notes and SoM Signal
21	EXT2_DIO6_P	224	AD19	IO	B2A_LVDS_14_N
22	EXT2_DIO3_P	210	Y19	IO	B2J_LVDS_11_N
23	EXT2_DIO4_N	218	AE20	IO	B2A_LVDS_10_N
24	EXT2_DIO1_N	204	AE17	IO	B2A_LVDS_17_P
25	EXT2_DIO4_P	216	AE19	IO	B2A_LVDS_10_P
26	EXT2_DIO1_P	202	AD17	IO	B2A_LVDS_17_N
27	EXT2_DIO2_N	208	AC18	IO	B2A_LVDS_16_N
28	EXT2_CLK0_N	200	AB23	I	B2J_LVDS_22_N
29	EXT2_DIO2_P	206	AD18	IO	B2A_LVDS_16_P
30	EXT2_CLK0_P	198	AC23	I	B2J_LVDS_22_P
31	EXT2_DIO29	192	AB21	IO	B2J_LVDS_15_N
32	EXT2_DIO30	194	AC21	IO	B2J_LVDS_15_P
33	EXT2_DIO27	188	AB20	IO	B2J_LVDS_13_N
34	EXT2_DIO28	190	AC20	IO	B2J_LVDS_13_P
35	EXT2_DIO26	186	AC17	IO	B2A_LVDS_15_N
36	EXT2_DIO25	184	AC16	IO	B2A_LVDS_15_P
37	EXT2_DIO23	180	AD15	IO	B2A_LVDS_3_N
38	EXT2_DIO24	182	AE16	IO	B2A_LVDS_3_P
39	EXT2_DIO33	174	AB15	IO	B2A_LVDS_21_N
40	EXT2_DIO34	176	AC15	IO	B2A_LVDS_21_P
41	EXT2_DIO31	170	AC11	IO	B2A_LVDS_24_N
42	EXT2_DIO32	172	AC12	IO	B2A_LVDS_24_P
43	EXT2_DIO35	166	AA16	IO	B2A_LVDS_13_N
44	EXT2_DIO36	168	AB16	IO	B2A_LVDS_13_P
45	EXT2_DIO37	162	AA11	IO	B2A_LVDS_19_N
46	EXT2_DIO38	164	AB11	IO	B2A_LVDS_19_P
47	EXT2_DIO41	136	D14	IO	B2K_LVDS_19_P
48	EXT2_DIO42	138	E14	IO	B2K_LVDS_19_N
49	EXT2_DIO39	132	D13	IO	B2K_LVDS_20_N
50	EXT2_DIO40	134	C13	IO	B2K_LVDS_20_P
51	EXT2_CLK1_P	106	C18	I	B2L_DIFFIO_24_P
52	SCL	84	B14	IO	B2K_LVDS_21_P
53	EXT2_CLK1_N	108	D17	I	B2L_DIFFIO_24_N
54	SDA	82	B15	IO	B2K_LVDS_21_N
55	GND	-	-	POWER	
56	GND	-	-	POWER	
57	NC	-	-		
58	NC	-	-		
59	NC	-	-		
60	GND	-	-	POWER	

Notes:

1. The maximum total current supplied to external components from the +5.0V supply should be limited to less than 2.0A. The maximum current allowed per connector pin is 1A.
2. The maximum total current supplied to external components from the VCCIO supply should be limited to less than 1.0A. The maximum current allowed per connector pin is 1A.
3. P3 connector part number: Samtec SSM-130-F-DV

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FMC Interface- J6

Table 11 describes the pin-out of the FMC interface on the MitySOM-C10G development board. The I/O "type" is in reference to the signal direction from the SoM/development board or power pin.

- J6 part number: Samtec ASP-134486-01

Table 11.1: J6 FMC Connector Pin A1-A40 Assignments

J6 Pin	FMC / Dev Kit Signal	J10 Pin[1]	SOM Signal	FPGA Ball	Type
A1	GND	66	GND	-	POWER
A2	DP1_M2C_P	64	GXB_1D_RX1_P	M26	MGT
A3	DP1_M2C_N	62	GXB_1D_RX1_N	M25	MGT
A4	GND	60	GND	-	POWER
A5	GND	74	GND	-	POWER
A6	DP2_M2C_P	72	GXB_1D_RX2_P	K26	MGT
A7	DP2_M2C_N	70	GXB_1D_RX2_N	K25	MGT
A8	GND	68	GND	-	POWER
A9	GND	82	GND	-	POWER
A10	DP3_M2C_P	80	GXB_1D_RX3_P	H26	MGT
A11	DP3_M2C_N	78	GXB_1D_RX3_N	H25	MGT
A12	GND	76	GND	-	POWER
A13	GND	90	GND		POWER
A14	DP4_M2C_P	88	GXB_1D_RX4_P	F26	MGT
A15	DP4_M2C_N	86	GXB_1D_RX4_N	F25	MGT
A16	GND	84	GND	-	POWER
A17	GND	98	GND	-	POWER
A18	DP5_M2C_P	96	GXB_1D_RX5_P	D26	MGT
A19	DP5_M2C_N	94	GXB_1D_RX5_N	D25	MGT
A20	GND	92	GND	-	POWER
A21	GND	61	GND	-	POWER
A22	DP1_C2M_P	59	GXB_1D_TX1_P	N28	MGT
A23	DP1_C2M_N	57	GXB_1D_TX1_N	N27	MGT
A24	GND	55	GND	-	POWER
A25	GND	69	GND	-	POWER
A26	DP2_C2M_P	67	GXB_1D_TX2_P	L28	MGT
A27	DP2_C2M_N	65	GXB_1D_TX2_N	L27	MGT
A28	GND	63	GND	-	POWER
A29	GND	77	GND	-	POWER
A30	DP3_C2M_P	75	GXB_1D_TX3_P	J28	MGT
A31	DP3_C2M_N	73	GXB_1D_TX3_N	J27	MGT
A32	GND	71	GND	-	POWER
A33	GND	85	GND	-	POWER
A34	DP4_C2M_P	83	GXB_1D_TX4_P	G28	MGT
A35	DP4_C2M_N	81	GXB_1D_TX4_N	G27	MGT
A36	GND	79	GND	-	POWER
A37	GND	93	GND	-	POWER
A38	DP5_C2M_P	91	GXB_1D_TX5_P	E28	MGT
A39	DP5_C2M_N	89	GXB_1D_TX5_N	E27	MGT
A40	GND	87	GND	-	POWER

Note 1: J10 is the secondary SOM Samtec connector

Table 11.2: J6 FMC Connector Pin B1-B40 Assignments

J6 Pin	FMC / Dev Kit Signal	J10 Pin[1]	SOM Signal	FPGA Ball	Type
B1	CLK_DIR	N/C	-	-	config
B2	GND	52	GND	-	POWER
B3	GND	50	GND	-	POWER
B4 [2]	DP9_M2C_P	48	GXB_1C_RX5_P	T26	MGT
B5 [2]	DP9_M2C_N	46	GXB_1C_RX5_N	T25	MGT
B6	GND	44	GND	-	POWER
B7	GND	42	GND	-	POWER
B8	DP8_M2C_P	40	GXB_1C_RX4_P	V26	MGT
B9	DP8_M2C_N	38	GXB_1C_RX4_N	V25	MGT
B10	GND	36	GND	-	POWER
B11	GND	34	GND	-	POWER
B12 [2]	DP7_M2C_P	32	GXB_1C_RX3_P	Y26	MGT
B13 [2]	DP7_M2C_N	30	GXB_1C_RX3_N	Y25	MGT
B14	GND	28	GND	-	POWER
B15	GND	26	GND	-	POWER
B16 [2]	DP6_M2C_P	24	GXB_1C_RX2_P	AB26	MGT
B17 [2]	DP6_M2C_N	22	GXB_1C_RX2_N	AB25	MGT
B18	GND	20	GND	-	POWER
B19	GND	18	GND	-	POWER
B20	GBTCLK1_M2C_P	N/C	-	-	MGT
B21	GBTCLK1_M2C_N	N/C	-	-	MGT
B22	GND	47	GND	-	POWER
B23	GND	45	GND	-	POWER
B24 [2]	DP9_C2M_P	43	GXB_1C_TX5_P	U28	MGT
B25 [2]	DP9_C2M_N	41	GXB_1C_TX5_N	U27	MGT
B26	GND	39	GND	-	POWER
B27	GND	37	GND	-	POWER
B28 [2]	DP8_C2M_P	35	GXB_1C_TX4_P	W28	MGT
B29 [2]	DP8_C2M_N	33	GXB_1C_TX4_N	W27	MGT
B30	GND	31	GND	-	POWER
B31	GND	29	GND	-	POWER
B32	DP7_C2M_P	27	GXB_1C_TX3_P	AA28	MGT
B33	DP7_C2M_N	25	GXB_1C_TX3_N	AA27	MGT
B34	GND	23	GND	-	POWER
B35	GND	21	GND	-	POWER
B36	DP6_C2M_P	19	GXB_1C_TX2_P	AC28	MGT
B37	DP6_C2M_N	17	GXB_1C_TX2_N	AC27	MGT
B38	GND	15	GND	-	POWER
B39	GND	13	GND	-	POWER
B40	RES0	N/C	-	-	config

Note 1: J10 is the secondary SOM Samtec connector
Note 2: Rev. 3A Development kit boards only: _P and _N connections are swapped.

Table 11.3: J6 FMC Connector Pin C1-C40 Assignments

J6 Pin	FMC / Dev Kit Signal	SOM Pin[2]	SOM Signal	FPGA Ball	Type
C1	GND	J10-53	GND	-	POWER
C2	DP0_C2M_P	J10-51	GXB_1D_TX0_P	R28	MGT
C3	DP0_C2M_N	J10-49	GXB_1D_TX0_N	R27	MGT
C4	GND	J10-47	GND	-	POWER
C5	GND	J10-58	GND	-	POWER
C6	DP0_M2C_P	J10-56	GXB_1D_RX0_P	P26	MGT
C7	DP0_M2C_N	J10-54	GXB_1D_RX0_N	P25	MGT
C8	GND	J10-52	GND	-	POWER
C9	GND	-	GND	-	POWER
C10	LA06_P	J1-245	B2J_LVDS_17_N	AG21	IO
C11	LA06_N	J1-247	B2J_LVDS_17_P	AH22	IO
C12	GND	-	GND	-	POWER
C13	GND	-	GND	-	POWER
C14	LA10_P	J1-227	B2J_LVDS_2_N	AH17	IO
C15	LA10_N	J1-229	B2J_LVDS_2_P	AH18	IO
C16	GND	-	GND	-	POWER
C17	GND	-	GND	-	POWER
C18	LA14_P	J1-167	B2A_LVDS_5_P	AF12	IO
C19	LA14_N	J1-165	B2A_LVDS_5_N	AF11	IO
C20	GND	-	GND	-	POWER
C21	GND	-	GND	-	POWER
C22	LA18_P_CC	J1-149	B2J_LVDS_5_P	AH12	IO
C23	LA18_N_CC	J1-147	B2J_LVDS_5_N	AG11	IO
C24	GND	-	GND	-	POWER
C25	GND	-	GND	-	POWER
C26	LA27_P	J1-183	B2A_LVDS_11_N	AF16	IO
C27	LA27_N	J1-185	B2A_LVDS_11_P	AG16	IO
C28	GND	-	GND	-	POWER
C29	GND	-	GND	-	POWER
C30	SCL	J1-84[1]	B2K_LVDS_21_P	B14	O
C31	SDA	J1-82[1]	B2K_LVDS_21_N	B15	IO
C32	GND	-	GND	-	POWER
C33	GND	-	GND	-	POWER
C34	GA0	-	GND	-	config
C35	12P0V	-	+12V	-	POWER
C36	GND	-	GND	-	POWER
C37	12P0V	-	+12V	-	POWER
C38	GND	-	GND	-	POWER
C39	3P3V	-	+3.3V	-	POWER
C40	GND	-	GND	-	POWER

Note 1: SCL and SDA are level translated from VCCIO (1.8V) to +3.3V on the DevKit Carrier card.
Note 2: SOM Pin -- J1 is the primary card-edge connector; J10 is the secondary Samtec connector

Table 11.4: J6 FMC Connector Pin D1-D40 Assignments

J6 Pin	FMC / Dev Kit Signal	SOM Pin[1]	SOM Signal	FPGA Ball	Type
D1	PG_C2M	N/C	-	-	config
D2	GND	-	GND	-	POWER
D3	GND	-	GND	-	POWER
D4	GBTCLK0_M2C_P	J10-102	REFCLK_1D_BOT_P	R24	MGT
D5	GBTCLK0_M2C_N	J10-104	REFCLK_1D_BOT_N	R23	MGT
D6	GND	-	GND	-	POWER
D7	GND	-	GND	-	POWER
D8	LA01_P_CC	J1-191	B2A_LVDS_7_P	AG18	IO
D9	LA01_N_CC	J1-193	B2A_LVDS_7_N	AF19	IO
D10	GND	-	GND	-	POWER
D11	LA05_P	J1-215	B2J_LVDS_12_P	AA18	IO
D12	LA05_N	J1-217	B2J_LVDS_12_N	AA19	IO
D13	GND	-	GND	-	POWER
D14	LA09_P	J1-233	B2J_LVDS_19_P	AG23	IO
D15	LA09_N	J1-235	B2J_LVDS_19_N	AF23	IO
D16	GND	-	GND	-	POWER
D17	LA13_P	J1-171	B2J_LVDS_10_P	AA17	IO
D18	LA13_N	J1-169	B2J_LVDS_10_N	Y17	IO
D19	GND	-	GND	-	POWER
D20	LA17_P_CC	J1-143	B2J_LVDS_4_P	AH11	IO
D21	LA17_N_CC	J1-141	B2J_LVDS_4_N	AH10	IO
D22	GND	-	GND	-	POWER
D23	LA23_P	J1-129	B2K_LVDS_5_N	D8	IO
D24	LA23_N	J1-127	B2K_LVDS_5_P	C8	IO
D25	GND	-	GND	-	POWER
D26	LA26_P	J1-115	B2K_LVDS_2_N	C10	IO
D27	LA26_N	J1-113	B2K_LVDS_2_P	B10	IO
D28	GND	-	GND	-	POWER
D29	TCK	N/C	-	-	JTAG
D30	TDI	N/C	-	-	JTAG
D31	TDO	N/C	-	-	JTAG
D32	3P3VAUX	-	+3.3V	-	POWER
D33	TMS	N/C	-	-	JTAG
D34	TRST_L	-	+3.3V	-	JTAG
D35	GA1	-	GND	-	POWER
D36	3P3V	-	+3.3V	-	POWER
D37	GND	-	GND	-	POWER
D38	3P3V	-	+3.3V	-	POWER
D39	GND	-	GND	-	POWER
D40	3P3V	-	+3.3V	-	POWER

Note 1: SOM Pin -- J1 is the primary card-edge connector; J10 is the secondary Samtec connector

Table 11.5: J6 FMC Connector Pin E1-E40 Assignments

J6 Pin	FMC / Dev Kit Signal	SOM Pin	SOM Signal	FPGA Ball	Type
E1	GND	-	GND	-	POWER
E2	HA01_P_CC	-	N/C	-	IO
E3	HA01_N_CC	-	N/C	-	IO
E4	GND	-	GND	-	POWER
E5	GND	-	GND	-	POWER
E6	HA05_P	-	N/C	-	IO
E7	HA05_N	-	N/C	-	IO
E8	GND	-	GND	-	POWER
E9	HA09_P	-	N/C	-	IO
E10	HA09_N	-	N/C	-	IO
E11	GND	-	GND	-	POWER
E12	HA13_P	-	N/C	-	IO
E13	HA13_N	-	N/C	-	IO
E14	GND	-	GND	-	POWER
E15	HA16_P	-	N/C	-	IO
E16	HA16_N	-	N/C	-	IO
E17	GND	-	GND	-	POWER
E18	HA20_P	-	N/C	-	IO
E19	HA20_N	-	N/C	-	IO
E20	GND	-	GND	-	POWER
E21	HB03_P	-	N/C	-	IO
E22	HB03_N	-	N/C	-	IO
E23	GND	-	GND	-	POWER
E24	HB05_P	-	N/C	-	IO
E25	HB05_N	-	N/C	-	IO
E26	GND	-	GND	-	POWER
E27	HB09_P	-	N/C	-	IO
E28	HB09_N	-	N/C	-	IO
E29	GND	-	GND	-	POWER
E30	HB13_P	-	N/C	-	IO
E31	HB13_N	-	N/C	-	IO
E32	GND	-	GND	-	POWER
E33	HB19_P	-	N/C	-	IO
E34	HB19_N	-	N/C	-	IO
E35	GND	-	GND	-	POWER
E36	HB21_P	-	N/C	-	IO
E37	HB21_N	-	N/C	-	IO
E38	GND	-	GND	-	POWER
E39	VADJ	-	VCCIO	-	POWER
E40	GND	-	GND	-	POWER

Table 11.6: J6 FMC Connector Pin F1-F40 Assignments

J6 Pin	FMC / Dev Kit Signal	SOM Pin	SOM Signal	FPGA Ball	Type
F1	PG_M2C	-	N/C	-	config
F2	GND	-	GND	-	POWER
F3	GND	-	GND	-	POWER
F4	HA00_P_CC	-	N/C	-	IO
F5	HA00_N_CC	-	N/C	-	IO
F6	GND	-	GND	-	POWER
F7	HA04_P	-	N/C	-	IO
F8	HA04_N	-	N/C	-	IO
F9	GND	-	GND	-	POWER
F10	HA08_P	-	N/C	-	IO
F11	HA08_N	-	N/C	-	IO
F12	GND	-	GND	-	POWER
F13	HA12_P	-	N/C	-	IO
F14	HA12_N	-	N/C	-	IO
F15	GND	-	GND	-	POWER
F16	HA15_P	-	N/C	-	IO
F17	HA15_N	-	N/C	-	IO
F18	GND	-	GND	-	POWER
F19	HA19_P	-	N/C	-	IO
F20	HA19_N	-	N/C	-	IO
F21	GND	-	GND	-	POWER
F22	HB02_P	-	N/C	-	IO
F23	HB02_N	-	N/C	-	IO
F24	GND	-	GND	-	POWER
F25	HB04_P	-	N/C	-	IO
F26	HB04_N	-	N/C	-	IO
F27	GND	-	GND	-	POWER
F28	HB08_P	-	N/C	-	IO
F29	HB08_N	-	N/C	-	IO
F30	GND	-	GND	-	POWER
F31	HB12_P	-	N/C	-	IO
F32	HB12_N	-	N/C	-	IO
F33	GND	-	GND	-	POWER
F34	HB16_P	-	N/C	-	IO
F35	HB16_N	-	N/C	-	IO
F36	GND	-	GND	-	POWER
F37	HB20_P	-	N/C	-	IO
F38	HB20_N	-	N/C	-	IO
F39	GND	-	GND	-	POWER
F40	VADJ	-	VCCIO	-	POWER

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Table 11.7: J6 FMC Connector Pin G1-G40 Assignments

J6 Pin	FMC / Dev Kit Signal	J1 Pin[1]	SOM Signal	FPGA Ball	Type
G1	GND	-	GND	-	POWER
G2	CLK1_M2C_P	131	B2K_LVDS_24_P	A11	I
G3	CLK1_M2C_N	133	B2K_LVDS_24_N	B11	I
G4	GND	-	GND	-	POWER
G5	GND	-	GND	-	POWER
G6	LA00_P_CC	199	B2J_LVDS_18_N	AG20	I
G7	LA00_N_CC	197	B2J_LVDS_18_P	AG19	I
G8	GND	-	GND	-	POWER
G9	LA03_P	205	B2A_LVDS_20_P	AB14	IO
G10	LA03_N	207	B2A_LVDS_20_N	AA14	IO
G11	GND	-	GND	-	POWER
G12	LA08_P	219	B2J_LVDS_3_N	AH15	IO
G13	LA08_N	221	B2J_LVDS_3_P	AH16	IO
G14	GND	-	GND	-	POWER
G15	LA12_P	237	B2J_LVDS_14_N	AH20	IO
G16	LA12_N	239	B2J_LVDS_14_P	AH21	IO
G17	GND	-	GND	-	POWER
G18	LA16_P	163	B2J_LVDS_1_P	AG10	IO
G19	LA16_N	161	B2J_LVDS_1_N	AG9	IO
G20	GND	-	GND	-	POWER
G21	LA20_P	153	B2J_LVDS_6_N	AG13	IO
G22	LA20_N	151	B2J_LVDS_6_P	AH13	IO
G23	GND	-	GND	-	POWER
G24	LA22_P	125	B2L_DIFFIO_2_P	J18	IO
G25	LA22_N	123	B2L_DIFFIO_2_N	J19	IO
G26	GND	-	GND	-	POWER
G27	LA25_P	111	B2K_LVDS_3_N	C11	IO
G28	LA25_N	109	B2K_LVDS_3_P	C12	IO
G29	GND	-	GND	-	POWER
G30	LA29_P	179	B2A_LVDS_12_P	AG14	IO
G31	LA29_N	181	B2A_LVDS_12_N	AG15	IO
G32	GND	-	GND	-	POWER
G33	LA31_P	156	B2A_LVDS_23_P	AA12	IO
G34	LA31_N	158	B2A_LVDS_23_N	AA13	IO
G35	GND	-	GND	-	POWER
G36	LA33_P	148	B2A_LVDS_6_P	AD13	IO
G37	LA33_N	150	B2A_LVDS_6_N	AD14	IO
G38	GND	-	GND	-	POWER
G39	VADJ	-	VCCIO	-	POWER
G40	GND	-	GND	-	POWER

Note 1: J1 is the primary SOM card-edge connector

Table 11.8: J6 FMC Connector Pin H1-H40 Assignments

J6 Pin	FMC / Dev Kit Signal	J1 Pin[1]	SOM Signal	FPGA Ball	Type
H1	VREF_A_M2C	N/C	-	-	POWER
H2	PRSNT_M2C_L	N/C	-	-	config
H3	GND	-	GND	-	POWER
H4	CLK0_M2C_P	201	B2J_LVDS_16_N	AE21	I
H5	CLK0_M2C_N	203	B2J_LVDS_16_P	AF21	I
H6	GND	-	GND	-	POWER
H7	LA02_P	187	B2A_LVDS_8_P	AF17	IO
H8	LA02_N	189	B2A_LVDS_8_N	AF18	IO
H9	GND	-	GND	-	POWER
H10	LA04_P	209	B2J_LVDS_23_N	AE22	IO
H11	LA04_N	211	B2J_LVDS_23_P	AF22	IO
H12	GND	-	GND	-	POWER
H13	LA07_P	223	B2J_LVDS_7_N	Y21	IO
H14	LA07_N	225	B2J_LVDS_7_P	AA21	IO
H15	GND	-	GND	-	POWER
H16	LA11_P	241	B2A_LVDS_18_N	Y15	IO
H17	LA11_N	243	B2A_LVDS_18_P	Y16	IO
H18	GND	-	GND	-	POWER
H19	LA15_P	157	B2A_LVDS_1_P	AE11	IO
H20	LA15_N	155	B2A_LVDS_1_N	AE10	IO
H21	GND	-	GND	-	POWER
H22	LA19_P	137	B2K_LVDS_4_N	A8	IO
H23	LA19_N	135	B2K_LVDS_4_P	C8	IO
H24	GND	-	GND	-	POWER
H25	LA21_P	119	B2L_DIFFIO_14_P	J20	IO
H26	LA21_N	117	B2L_DIFFIO_14_N	K21	IO
H27	GND	-	GND	-	POWER
H28	LA24_P	107	B2K_LVDS_6_P	D9	IO
H29	LA24_N	105	B2K_LVDS_6_N	D10	IO
H30	GND	-	GND	-	POWER
H31	LA28_P	173	B2A_LVDS_9_P	AF13	IO
H32	LA28_N	175	B2A_LVDS_9_N	AF14	IO
H33	GND	-	GND	-	POWER
H34	LA30_P	152	B2A_LVDS_2_N	AE14	IO
H35	LA30_N	154	B2A_LVDS_2_P	AE15	IO
H36	GND	-	GND	-	POWER
H37	LA32_P	142	B2A_LVDS_4_N	AD12	IO
H38	LA32_N	144	B2A_LVDS_4_P	AE12	IO
H39	GND	-	GND	-	POWER
H40	VADJ	-	VCCIO	-	POWER

Note 1: J1 is the primary SOM card-edge connector

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Table 11.9: J6 FMC Connector Pin J1-J40 Assignments

J6 Pin	FMC / Dev Kit Signal	SOM Pin	SOM Signal	FPGA Ball	Type
J1	GND	-	GND	-	POWER
J2	CLK3_BIDIR_P	-	N/C	-	IO
J3	CLK3_BIDIR_N	-	N/C	-	IO
J4	GND	-	GND	-	POWER
J5	GND	-	GND	-	POWER
J6	HA03_P	-	N/C	-	IO
J7	HA03_N	-	N/C	-	IO
J8	GND	-	GND	-	POWER
J9	HA07_P	-	N/C	-	IO
J10	HA07_N	-	N/C	-	IO
J11	GND	-	GND	-	POWER
J12	HA11_P	-	N/C	-	IO
J13	HA11_N	-	N/C	-	IO
J14	GND	-	GND	-	POWER
J15	HA14_P	-	N/C	-	IO
J16	HA14_N	-	N/C	-	IO
J17	GND	-	GND	-	POWER
J18	HA18_P	-	N/C	-	IO
J19	HA18_N	-	N/C	-	IO
J20	GND	-	GND	-	POWER
J21	HA22_P	-	N/C	-	IO
J22	HA22_N	-	N/C	-	IO
J23	GND	-	GND	-	POWER
J24	HB01_P	-	N/C	-	IO
J25	HB01_N	-	N/C	-	IO
J26	GND	-	GND	-	POWER
J27	HB07_P	-	N/C	-	IO
J28	HB07_N	-	N/C	-	IO
J29	GND	-	GND	-	POWER
J30	HB11_P	-	N/C	-	IO
J31	HB11_N	-	N/C	-	IO
J32	GND	-	GND	-	POWER
J33	HB15_P	-	N/C	-	IO
J34	HB15_N	-	N/C	-	IO
J35	GND	-	GND	-	POWER
J36	HB18_P	-	N/C	-	IO
J37	HB18_N	-	N/C	-	IO
J38	GND	-	GND	-	POWER
J39	VIO_B_M2C	-	N/C	-	POWER
J40	GND	-	GND	-	POWER

Table 11.10: J6 FMC Connector Pin K1-K40 Assignments

J6 Pin	FMC / Dev Kit Signal	SOM Pin	SOM Signal	FPGA Ball	Type
K1	VREF_B_M2C	-	N/C	-	POWER
K2	GND	-	GND	-	POWER
K3	GND	-	GND	-	POWER
K4	CLK2_BIDIR_P	-	N/C	-	NC
K5	CLK2_BIDIR_N	-	N/C	-	NC
K6	GND	-	GND	-	POWER
K7	HA02_P	-	N/C	-	NC
K8	HA02_N	-	N/C	-	NC
K9	GND	-	GND	-	POWER
K10	HA06_P	-	N/C	-	NC
K11	HA06_N	-	N/C	-	NC
K12	GND	-	GND	-	POWER
K13	HA10_P	-	N/C	-	NC
K14	HA10_N	-	N/C	-	NC
K15	GND	-	GND	-	POWER
K16	HA17_P_CC	-	N/C	-	NC
K17	HA17_N_CC	-	N/C	-	NC
K18	GND	-	GND	-	POWER
K19	HA21_P	-	N/C	-	NC
K20	HA21_N	-	N/C	-	NC
K21	GND	-	GND	-	POWER
K22	HA23_P	-	N/C	-	NC
K23	HA23_N	-	N/C	-	NC
K24	GND	-	GND	-	POWER
K25	HB00_P_CC	-	N/C	-	NC
K26	HB00_N_CC	-	N/C	-	NC
K27	GND	-	GND	-	POWER
K28	HB06_P_CC	-	N/C	-	NC
K29	HB06_N_CC	-	N/C	-	NC
K30	GND	-	GND	-	POWER
K31	HB10_P	-	N/C	-	NC
K32	HB10_N	-	N/C	-	NC
K33	GND	-	GND	-	POWER
K34	HB14_P	-	N/C	-	NC
K35	HB14_N	-	N/C	-	NC
K36	GND	-	GND	-	POWER
K37	HB17_P_CC	-	N/C	-	NC
K38	HB17_N_CC	-	N/C	-	NC
K39	GND	-	GND	-	POWER
K40	VIO_B_M2C	-	N/C	-	POWER

Please see the following VITA documentation concerning the FMC specification (https://www.vita.com/fmc).

10/100/1000 Ethernet Interface – J5

The MitySOM-C10L Development Kit provides an RJ-45 connection for a Gigabit 10/100/1000 Ethernet connection. This connection follows standard TIA/EIA-568B pin-out as shown in Table 12 below.

Table 12: J5 Ethernet RJ45 Pin Assignments

Pin	Signal	Type
1	TXRXA_P	I/O
2	TXRXA_N	I/O
3	TXRXB_P	I/O
4	TXRXC_P	I/O
5	TXRXC_N	I/O
6	TXRXB_N	I/O
7	TXRXD_P	I/O
8	TXRXD_N	I/O

The Ethernet PHY located on the Development Kit, Micrel KSZ9131, will auto negotiate to the speed of the device it is connected to. The Ethernet PHY is connected to the module through FPGA IO pins as shown in Table 13 below.

Table 13: Ethernet PHY to SoM / FPGA Interface

Dev Kit Signal	J1 Pin[1]	SOM Signal	FPGA Ball
ETH_RXD0	54	B2L_DIFFIO_7_N	E21
ETH_RXD1	56	B2L_DIFFIO_22_P	D20
ETH_RXD2	58	B2L_DIFFIO_22_N	E20
ETH_RXD3	60	B2L_DIFFIO_6_P	G20
ETH_RX_CLK	62	B2L_DIFFIO_6_N	G19
ETH_RX_CTL	64	B2L_DIFFIO_13_P	J23
ETH_TXD0	42	B2L_DIFFIO_8_N	E23
ETH_TXD1	44	B2L_DIFFIO_8_P	D23
ETH_TXD2	46	B2L_DIFFIO_10_P	C23
ETH_TXD3	48	B2L_DIFFIO_10_N	C22
ETH_TX_CLK	34	B2K_LVDS_18_P	B26
ETH_TX_CTL	36	B2K_LVDS_18_N	B25
ETH_MDIO	78	B2L_DIFFIO_20_N	E17
ETH_MDC	80	B2L_DIFFIO_20_P	E16
ETH_RESETn	66	B2L_DIFFIO_13_N	H23
ETH_INT_N	52	B2L_DIFFIO_7_P	D22

Note 1: J1 is the primary SOM card-edge connector

MECHANICAL INTERFACE DESCRIPTION

Main Board Interface / Mounting

Four mounting holes are available for mounting standoffs to the devkit PCB.

Figure 2 shows the location of the mounting holes as well as the location holes for the FMC interface (J6). Refer to the MitySOM-C10G datasheet for locations of the PEM nut positions (P6 and P7) with respect to the SODIMM DDR4 connector.

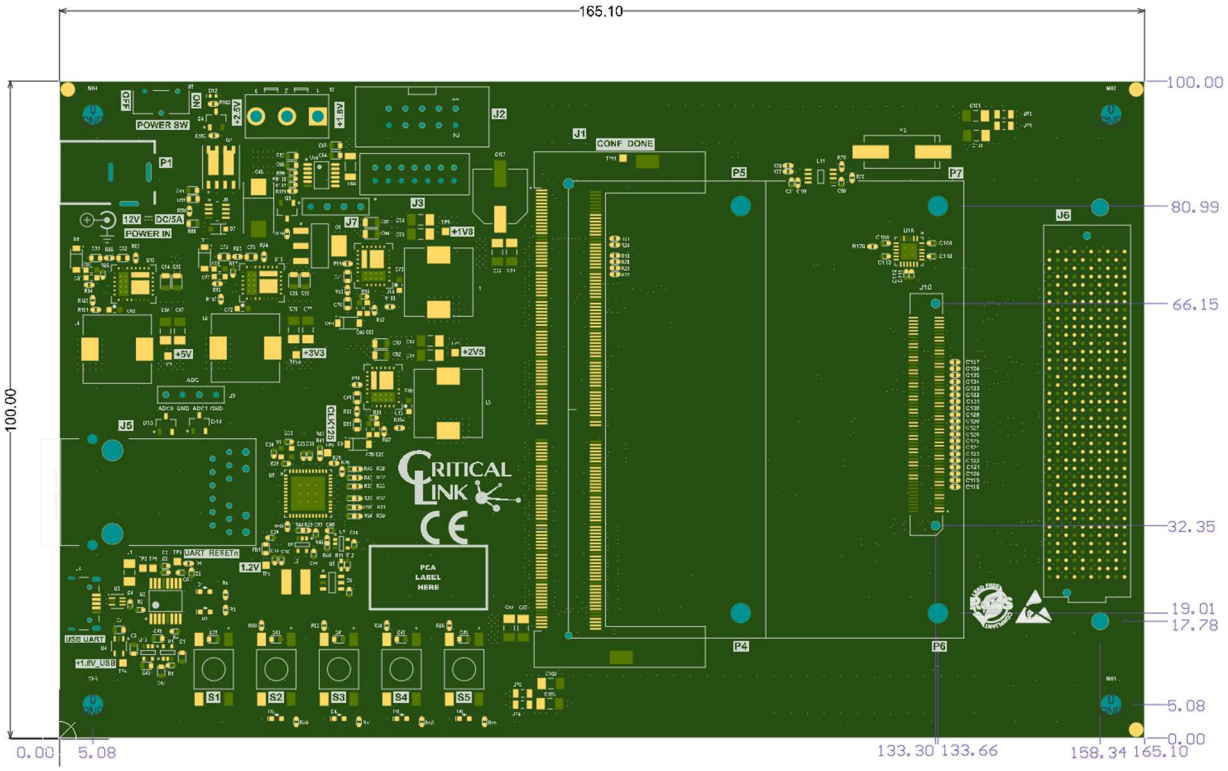

Figure 2 MitySOM-C10G Development Kit Outline, Mounting Hole Locations (Top View, millimeters)

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Figure 3 shows the locations of Pin 1 and the mechanical center of the 2x30 female headers for each of the expansion ports.

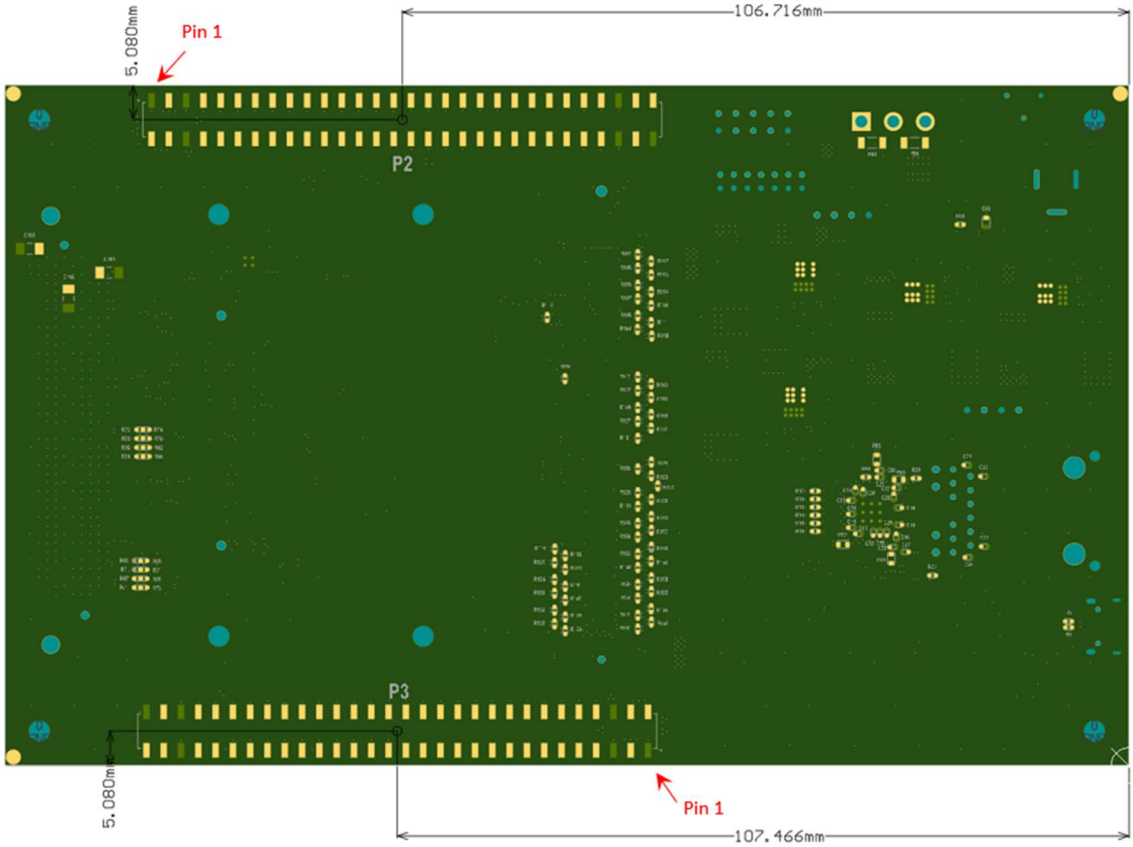

Figure 3 MitySOM-C10G Development Kit Outline, Bottom View / Connector Locations

Figure 4 shows the location of each of the external interfaces on the MitySOM-C10G development kit.

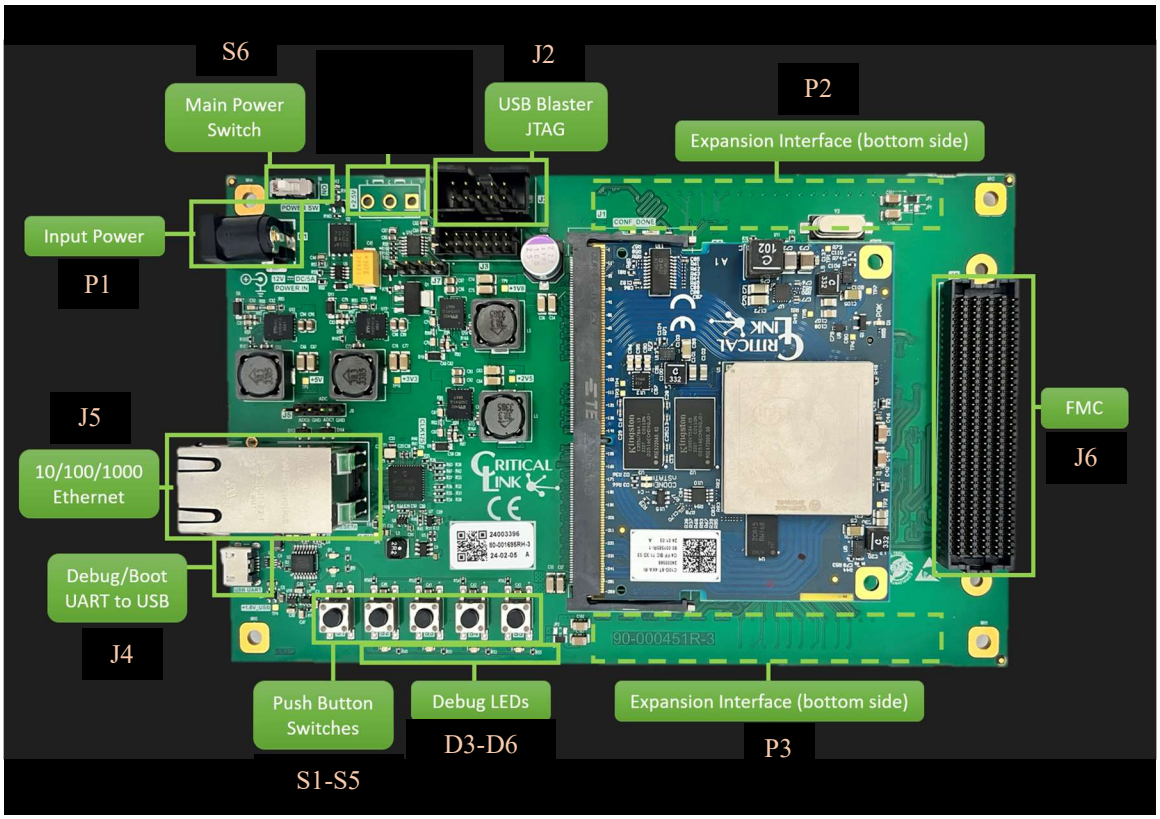

Figure 4 MitySOM-C10G Development Kit, External Interface Locations

P3 (bottom side)

ORDERING INFORMATION

Included Components

Table 14 lists the components that are included with a MitySOM-C10G Development Kit. See Table 15 for specific development kit ordering information.

Figure 4 shows the Development Kit Board, noting some key features.

Table 14: Included Items

Description	Part Number	Interface Port	Qty. Included
MitySOM-C10G Development Kit Board	80-001695	n/a	Qty. 1
MitySOM-C10G Module	See Table 15	J1	Qty. 1
Micro USB Cable for Debug Console		J4	Qty. 1
12V 5A AC to DC Supply		P1	Qty. 1
Ethernet cable		J5	Qty. 1
Development Kit Quick Start Guide		n/a	

Development Kits

The following table lists the standard MitySOM-C10G Development Kit configurations. For shipping status, availability, and lead time of these or other configurations please contact Critical Link at info@criticallink.com.

Table 15: Standard Model Numbers

Development Kit Model	Module Included
80-001738	C10G-6T-4XA-RI

REVISION HISTORY

Date	Revision	Change Description
07/17/2024	A	Initial Release