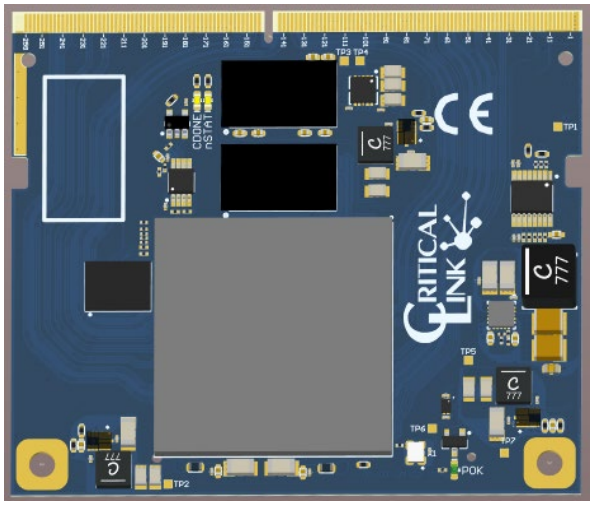
C10G FEATURES

- Intel Cyclone 10 GX – F780 FPGA
  - Up To 220K Logic Elements (LE)
  - Up to 192 DSP Logic Blocks
  - Up to 300Mhz Fabric Clock
  - Up To 11.7Mb Embedded Memory
  - Up To 4 fractional synthesis PLLs
  - Up To 6 IO PLLs
- **Memory**
  - Up To 1GB DDR3L at 7.45 GB/sec
  - Up To 32MB QPSI NOR FLASH
- 4 Banks of FPGA IO
  - 192 Direct Connect FPGA IO pins
  - 70 true LVDS pairs
  - 1.8 LVCMOS, LVDS, SSTL-18, and 1.8V HSTL IO standards supported.
  - 8 Clock Input Pins
- Up to 12 Transceiver Pairs
  - Speeds up to 12.5 Gbps
  - PCIe Gen2 x4 hard IP block
  - 4 Clock Inputs
- Integrated Power Management
  - Single +5V Input for on-board needs
  - Bank IO Voltage Configured for 1.8V
  - Bank IO Reference Voltage at 0.9V
- JTAG Interface Available on Edge Connector
- 2 Channels of ADC input
- **On-Board 100 MHz CLK_USR clock**
- **Configuration Status and General-Purpose Tri-Color LEDs**



- **Mechanical**
  - 260-Pin Card Edge Connector
  - 144-Pin Board to Board Connector (bottom side, not shown in figure)
  - Small 70mm (2.75”) x 60mm (2.4”) size

APPLICATIONS

- Embedded Co-Processor
- Test and Measurement
- Embedded Instrumentation
- Industrial Automation and Control
- Industrial Instrumentation
- System IO expansion
- Embedded Imaging

BENEFITS

- Low Power and Low-Cost FPGA Solution
- Rapid Development / Deployment
- Multiple Connectivity and I/O Options
- Support for NIOS II Softcore
  - 30 to 190 DMIPS
- Support for NIOS V planned

DESCRIPTION

The MitySOM-C10G series of highly configurable, small form-factor System-on-Modules (SoM) features an Intel Cyclone 10 GX field programmable gate array (FPGA) and includes on-board power supplies, NOR FLASH and DDR3L memory subsystem. Using an NIOS II Softcore processor, the MitySOM-C10G provides a complete and flexible CPU infrastructure for a low cost integrated embedded system.

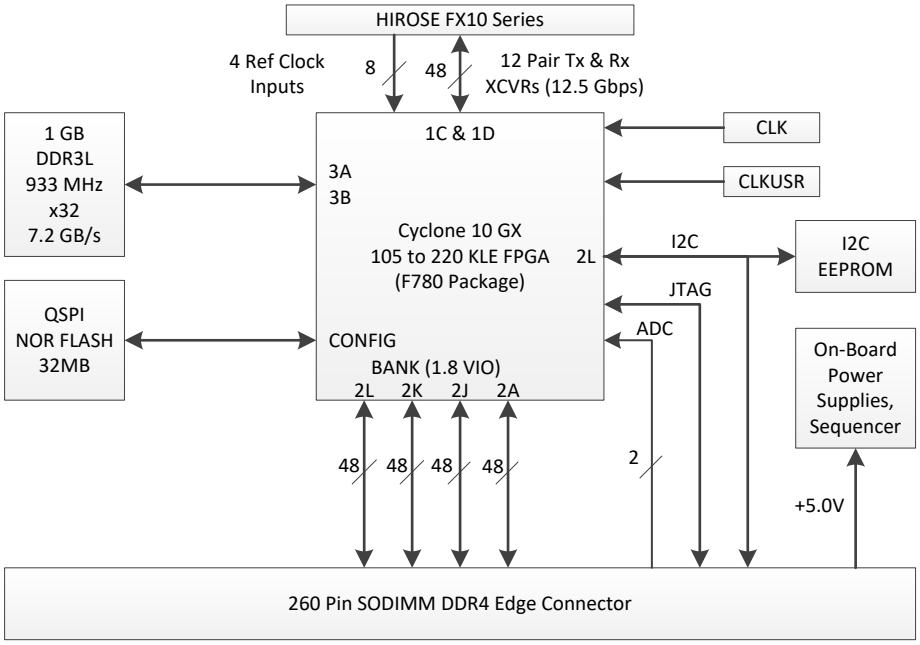


Figure 1 MitySOM-C10G Block Diagram

Figure 1 provides a top-level block diagram of the MitySOM-C10G processor card. As shown in the figure, the interface to the MitySOM-C10G standard bank IO is through a 260-Pin card edge interface. Details of the edge connector interface are included in the Card Edge Interface Description section. In addition, a second board to board connector is provided for access to up to 12 lanes of transceiver IO pins and associated clock inputs.

MitySOM-C10G Onboard Storage

DDR3L Memory

The MitySOM-C10G includes one dedicated 32-bit DDR3L memory interface. A maximum of 1GB of DDR3L is supported by standard MitySOM-C10G modules. The DDR3L interface can be run at up to 933 MHz supporting 7.2 GBs burst transfer rates.

This DDR3L memory may be utilized by the standard FPGA fabric or may be integrated with a NIOS II processor subsystem via Avalon high speed interfaces internal to the Cyclone 10 GX.

See Table 8: Standard Model Numbers for additional details.

NOR FLASH

A maximum of 32MB (1 x 32MB) of on-board quad-SPI NOR FLASH memory is connected to the Cyclone 10 GX via the Active Serial (AS) Configuration serial peripheral interface. This is a reliable flash memory that is used as the primary configuration media for the Cyclone 10 GX. The NOR FLASH memory may also be used at runtime for storing NIOS II executable code and/or user non-volatile data.

I2C EEPROM

An on-board 2 KB I^2C Electrically Erasable Programmable Read-Only Memory (EEPROM) is included on the MitySOM-C10G. The EEPROM includes factory configuration information including assigned serial number, part number, and model number information.

MitySOM-C10G Debug Support

The JTAG interface signals for the Cyclone 10 GX FPGA have been brought out to the SODIMM DDR4 card edge connector. This allows customers to decide whether the interface should be exposed on their custom carrier cards. The on-board MitySOM-C10G SPI NOR FLASH, used to hold the FPGA configuration bitstream, may be programmed via the JTAG interface. In addition, the JTAG interface may be used for in-circuit debugging using standard Intel Quartus Signal Tap logic analyzer and probing tools.

General Status LEDs

There are three light emitting diodes (LEDs) on the MitySOM-C10G module. The LEDs are identified in Figure 2.

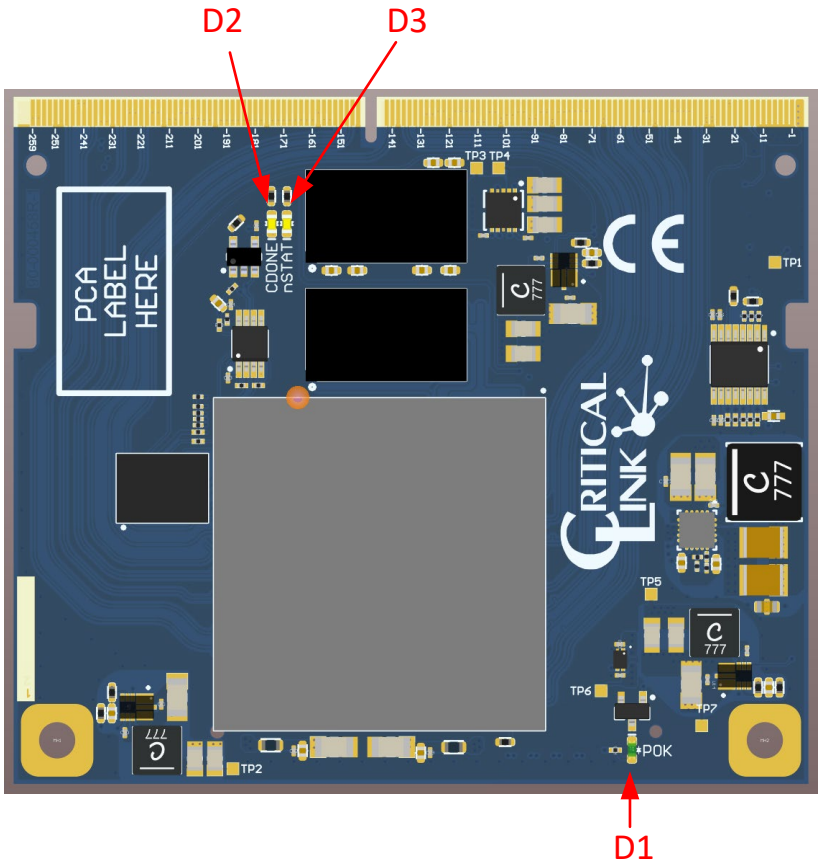


Figure 2 MitySOM-C10G LED positions

Power OK

D1 indicates the MitySOM-C10G on-module power supplies have sequenced on correctly and are currently operating.

Configuration Debug

D2 indicates that FPGA configuration is not complete by lighting a yellow LED. Once the configuration is complete, D2 should turn off.

The cathode of D3 is connected to the nSTATUS signal on the Cyclone 10 GX device and can be used to troubleshoot configuration of the device.

External Interface Connections

GPIO

The MitySOM-C10G routes all 48 pins (192 total) of the Cyclone 10 GX FPGA Bank 2A, 2J, 2K and 2L pins directly to the edge connector interface. All banks are powered with an on-board 1.8V bank voltage and a 0.9V reference voltage. This allows the pins to support both LVDS, 1.8V HSTL, and 1.8V LVCMOS single ended operation.

The MitySOM-C10G FPGA IO mapping has been made with vertical migration in mind. A completed design using the 105 KLE density option will work with the MitySOM-C10G 220 KLE density modules. No adjustments to IO planning should be required.

JTAG

The Cyclone 10 GX JTAG signals (TDI, TDO, TMS, TCK) as well as the 1.8V reference voltage necessary for interfacing to a standard Intel USB Blaster JTAG POD have been routed to the DDR4 edge connector. The TDI and TMS signals are pulled up on board and the TCK signal is pulled down on the SOM in order to support leaving these signals disconnected if desired. The JTAG interface supports programming the Cyclone 10 GX bitstream and may be used to program the on-board SPI NOR FLASH using the FPGA as a proxy controller.

Configuration Status / Control

The MitySOM-C10G exposes the CONFIG_DONE signal from the FPGA on pin 24 of the DDR4 edge connector. The CONFIG_DONE signal is low when the FPGA is not configured and +1.8V when the FPGA is successfully configured. The signal is pulled up to +1.8V with a 10K resistor on the SOM.

Also exposed is the nCONFIG signal input on the FPGA, on pin 23. The nCONFIG signal is pulled high to +1.8V on the MitySOM_C10G. The nCONFIG signal may be pulled and held low for at least 0.5 us to reset the FPGA and reset the configuration sequence.

Application Development Support

Users of the MitySOM-C10G are encouraged to develop applications using the MitySOM-C10G development kit provided by Critical Link LLC.

Growth Options

The MitySOM-C10G has been designed to support several upgrade options. These options include a range of speed grades, DDR3L memory density, quad-SPI NOR FLASH density, and operating temperature specifications including commercial and industrial temperature ranges. The available options are listed in the section below containing ordering information. For additional ordering information and details regarding these options, or to inquire about a particular configuration not listed below, please contact Critical Link via info@criticallink.com.

Absolute Maximum Ratings

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Table 1: Absolute Maximum Ratings

Maximum Supply Voltage (+5VIN)	5.5V
Storage Temperature Range	-55ºC to 150ºC

Operating Conditions

The following are the minimum temperature ratings for the components that are installed on a MitySOM-C10G. For specifications not contained in this table please contact a Critical Link sales representative. Please see the Thermal Management section below concerning ambient/operating temperature recommendations.

Table 2: Module Component Temperature Ratings (minimum)

Temperature Range	Component Ratings
Commercial (-RC)	0ºC to 70ºC
Industrial (-RI)	-40ºC to 85ºC

Thermal Management

The MitySOM-C10G module requires careful consideration of thermal management. Depending on fabric load, thermal management may be required for operation at elevated temperatures.

Thermal management is a system level issue that must be addressed in conjunction with the overall system design. Some systems may have available airflow with limited space for a heat sink; others may have room for a heat sink with or without the possibility for additional airflow. As a result, the approach taken for thermal management is a design consideration that must be addressed by the overall system designers when integrating the MitySOM-C10G into a product.

Every product is different, and it is advisable to perform thorough testing to ensure that the product will meet desired performance and longevity specifications. We recommend that customers utilize Intel's Early Power Estimator (EPE) for the Cyclone 10 GX. This utility will assist in estimating the potential power usage of the processor for a given application. Details can be found on the PowerPlay EPE page at Intel.com.

Card-Edge Interface Description

The primary interface connector for the MitySOM-C10G is the 260-pin card edge interface which contains 4 types of signals:

- Power (**P**) Input to the module
- General purpose I/O pins mapped to the Cyclone 10 GX FPGA pins (**IO**)
- Fixed Function Digital Input Pins **(I)**
- Fixed Function Output pins (**O**)
- Fixed Function Analog Input Pins (AI)

Table 3 contains a summary of the MitySOM-C10G pin-mapping. For pins connected directly to an FPGA ball, the following FPGA information is also included in the table:

- FPGA Ball Number
- FPGA Bank Number
- FPGA IO Voltage Reference Group; this can vary with FPGA density option
- FPGA IO Optional Function; this can vary with FPGA density option
- Matched Length Group; each bank of FPGA pins includes a group of IO that have the trace lengths matched to +/- 5mil to better support high speed bus IO routing. Lengths between groups are not matched.
- LVDS / differential support; FPGA IO pairs routed to the edge connector are indicated. TRUE pairs represent pins on FPGA ROW I/O banks supporting true LVDS standards. EMULATED pairs represent pins on FPGA Bank 2L. See the Cyclone 10 GX Fabric User Guide for additional detail. FPGA IO pairs are routed differentially on the MitySOM-C10G. Each group of bank pins are also length matched.

Card-Edge Mating Connector

The MitySOM-C10G module mates with a connector that contains all the power and standard bank I/O for the module. The mating socket is a 260-pin SODIMM DDR4 style connector. An example connector is a TE Connectivity AMP Connectors 2309411-1, which is available from distributors such as DigiKey and Mouser. There are several height options for these connectors, the height should be selected in order to provide approximately 5mm board to board height, as that is the stacking height used by the Hirose connector interface.

Table 3: MitySOM-C10G Edge Connector Pin-Out

Pin	Net Name	Type	FPGA Ball	FPGA Bank	LVDS?	Optional Function	Notes
1	+5V	P	-				
2	GND	P	-				
3	+5V	P	-				
4	GND	P	-				
5	+5V	P	-				
6	GND	P	-				
7	+5V	P	-				
8	GND	P	-				
9	+5V	P	-				
10	GND	P	-				
11	+5V	P	-				
12	GND	P	-				
13	+5V	P	-				
14	GND	P	-				
15	PROC_RST	I	-				
16	TDI	I	AC10	CSS			10k pullup to +1.8V
17	RESERVED	-	-				
18	TDO	O	W10	CSS			
19	+1.8V_JTAG	P	-				
20	TCK	I	Y9	CSS			1k pulldown
21	PWR_OK	O	-				OD to +5V, 1K pullup (+5V is PWR_OK)
22	TMS	I	AH6	CSS			10k pullup to +1.8V
23	NCONFIG	I	AC8	CSS			10k pullup to +1.8V
24	CONF_DONE	O	AG8	CSS			10k pullup to +1.8V
25	RESERVED	-	-				
26	RESERVED	-	-				
27	RESERVED	-	-				
28	RESERVED	-	-				
29	GND	P	-				

Pin	Net Name	Type	FPGA Ball	FPGA Bank	LVDS?	Optional Function	Notes
30	GND	P	-				
31	GND	P	-				
32	GND	P	-				
33	B2K_LVDS_16_P	IO	A27	2K	YES		
34	B2K_LVDS_18_P	IO	B26	2K	YES		
35	B2K_LVDS_16_N	IO	A26	2K	YES		
36	B2K_LVDS_18_N	IO	B25	2K	YES		
37	B2K_LVDS_15_P	IO	B24	2K	YES	PLL_2K_CLKOUT0p,PLL_2K_CLKOUT0,PLL_2K_FB0	
38	B2L_DIFFIO_15_N	IO	H22	2L	NO	PLL_2L_CLKOUT0n	
39	B2K_LVDS_15_N	IO	B23	2K	YES	PLL_2K_CLKOUT0n	
40	B2L_DIFFIO_15_P	IO	J22	2L	NO	PLL_2L_CLKOUT0p,PLL_2L_CLKOUT0,PLL_2L_FB0	
41	B2K_LVDS_14_N	IO	C21	2K	YES		
42	B2L_DIFFIO_8_N	IO	E23	2L	NO		
43	B2K_LVDS_14_P	IO	B21	2K	YES		
44	B2L_DIFFIO_8_P	IO	D23	2L	NO		
45	B2K_LVDS_13_P	IO	A24	2K	YES	CLK_2K_0p	
46	B2L_DIFFIO_10_P	IO	C23	2L	NO	PLL_2L_CLKOUT1p,PLL_2L_CLKOUT1,PLL_2L_FB1	
47	B2K_LVDS_13_N	IO	A23	2K	YES	CLK_2K_0n	
48	B2L_DIFFIO_10_N	IO	C22	2L	NO	PLL_2L_CLKOUT1n	
49	GND	P	-				
50	GND	P	-				
51	B2K_LVDS_11_N	IO	C20	2K	YES		
52	B2L_DIFFIO_7_P	IO	D22	2L	NO		
53	B2K_LVDS_11_P	IO	B20	2K	YES	RZQ_2K	
54	B2L_DIFFIO_7_N	IO	E21	2L	NO		
55	B2K_LVDS_17_N	IO	A22	2K	YES		
56	B2L_DIFFIO_22_P	IO	D20	2L	NO		
57	B2K_LVDS_17_P	IO	A21	2K	YES		
58	B2L_DIFFIO_22_N	IO	E20	2L	NO		
59	B2K_LVDS_8_P	IO	A19	2K	YES		
60	B2L_DIFFIO_6_P	IO	G20	2L	NO		

Pin	Net Name	Type	FPGA Ball	FPGA Bank	LVDS?	Optional Function	Notes
61	B2K_LVDS_8_N	IO	A18	2K	YES		
62	B2L_DIFFIO_6_N	IO	G19	2L	NO		
63	B2K_LVDS_7_P	IO	A17	2K	YES		
64	B2L_DIFFIO_13_P	IO	J23	2L	NO	CLK_2L_0p	
65	B2K_LVDS_7_N	IO	A16	2K	YES		
66	B2L_DIFFIO_13_N	IO	H23	2L	NO	CLK_2L_0n	
67	GND	P	-				
68	GND	P	-				
69	B2K_LVDS_23_N	IO	A13	2K	YES		
70	B2L_DIFFIO_12_N	IO	G23	2L	NO	CLK_2L_1n	
71	B2K_LVDS_23_P	IO	A12	2K	YES		
72	B2L_DIFFIO_12_P	IO	F23	2L	NO	CLK_2L_1p	
73	B2L_DIFFIO_4_P	IO	F17	2L	NO		
74	B2L_DIFFIO_19_P	IO	D19	2L	NO		
75	B2L_DIFFIO_4_N	IO	F18	2L	NO		
76	B2L_DIFFIO_19_N	IO	D18	2L	NO		
77	B2K_LVDS_9_P	IO	B16	2K	YES		
78	B2L_DIFFIO_20_N	IO	E17	2L	NO		
79	B2K_LVDS_9_N	IO	C15	2K	YES		
80	B2L_DIFFIO_20_P	IO	E16	2L	NO		
81	B2K_LVDS_10_N	IO	B18	2K	YES	PLL_2K_CLKOUT1n	
82	B2K_LVDS_21_N	IO	B15	2K	YES		
83	B2K_LVDS_10_P	IO	B19	2K	YES	PLL_2K_CLKOUT1p, PLL_2K_CLKOUT1, PLL_2K_FB1	
84	B2K_LVDS_21_P	IO	B14	2K	YES		
85	GND	P	-				
86	GND	P	-				
87	B2L_DIFFIO_5_P	IO	G18	2L	NO		
88	B2L_DIFFIO_23_P	IO	C17	2L	NO		
89	B2L_DIFFIO_5_N	IO	H18	2L	NO		
90	B2L_DIFFIO_23_N	IO	C16	2L	NO		

Pin	Net Name	Type	FPGA Ball	FPGA Bank	LVDS?	Optional Function	Notes
91	B2L_DIFFIO_1_P	IO	H17	2L	NO		
92	B2K_LVDS_12_N	IO	E15	2K	YES	CLK_2K_1n	
93	B2L_DIFFIO_1_N	IO	H16	2L	NO		
94	B2K_LVDS_12_P	IO	D15	2K	YES	CLK_2K_1p	
95	B2L_DIFFIO_16_P	IO	H20	2L	NO		
96	B2L_DIFFIO_9_N	IO	F22	2L	NO		
97	B2L_DIFFIO_16_N	IO	H21	2L	NO		
98	B2L_DIFFIO_9_P	IO	E22	2L	NO		
99	B2K_LVDS_22_P	IO	A14	2K	YES		
100	B2L_DIFFIO_11_P	IO	F21	2L	NO	RZQ_2L	
101	B2K_LVDS_22_N	IO	B13	2K	YES		
102	B2L_DIFFIO_11_N	IO	G21	2L	NO		
103	GND	P	-				
104	GND	P	-				
105	B2K_LVDS_6_N	IO	D10	2K	YES		
106	B2L_DIFFIO_24_P	IO	C18	2L	NO		
107	B2K_LVDS_6_P	IO	D9	2K	YES		
108	B2L_DIFFIO_24_N	IO	D17	2L	NO		
109	B2K_LVDS_3_P	IO	C12	2K	YES		
110	B2L_DIFFIO_21_P	IO	E19	2L	NO		
111	B2K_LVDS_3_N	IO	C11	2K	YES		
112	B2L_DIFFIO_21_N	IO	F19	2L	NO		
113	B2K_LVDS_2_P	IO	B10	2K	YES		
114	B2K_LVDS_1_P	IO	B9	2K	YES		
115	B2K_LVDS_2_N	IO	C20	2K	YES		
116	B2K_LVDS_1_N	IO	B8	2K	YES		
117	B2L_DIFFIO_14_N	IO	K21	2L	NO		
118	B2L_DIFFIO_18_P	IO	K23	2L	NO		
119	B2L_DIFFIO_14_P	IO	J20	2L	NO		
120	B2L_DIFFIO_18_N	IO	K22	2L	NO		
121	GND	P	-				

Pin	Net Name	Type	FPGA Ball	FPGA Bank	LVDS?	Optional Function	Notes
122	GND	P	-				
123	B2L_DIFFIO_2_N	IO	J19	2L	NO		
124	B2L_DIFFIO_3_P	IO	J17	2L	NO		
125	B2L_DIFFIO_2_P	IO	J18	2L	NO		
126	B2L_DIFFIO_3_N	IO	K17	2L	NO		
127	B2K_LVDS_5_P	IO	C8	2K	YES		
128	B2L_DIFFIO_17_P	IO	K19	2L	NO		
129	B2K_LVDS_5_N	IO	D8	2K	YES		
130	B2L_DIFFIO_17_N	IO	K20	2L	NO		
131	B2K_LVDS_24_P	IO	A11	2K	YES		
132	B2K_LVDS_20_N	IO	D13	2K	YES		
133	B2K_LVDS_24_N	IO	B11	2K	YES		
134	B2K_LVDS_20_P	IO	C13	2K	YES		
135	B2K_LVDS_4_P	IO	A9	2K	YES		
136	B2K_LVDS_19_P	IO	D14	2K	YES		
137	B2K_LVDS_4_N	IO	A8	2K	YES		
138	B2K_LVDS_19_N	IO	E14	2K	YES		
139	GND	P	-				
140	GND	P	-				
141	B2J_LVDS_4_N	IO	AH10	2J	YES		
142	B2A_LVDS_4_N	IO	AD12	2A	YES		
143	B2J_LVDS_4_P	IO	AH11	2J	YES		
144	B2A_LVDS_4_P	IO	AE12	2A	YES		
145	GND	P	-				
146	GND	P	-				
147	B2J_LVDS_5_N	IO	AG11	2J	YES		
148	B2A_LVDS_6_P	IO	AD13	2A	YES		
149	B2J_LVDS_5_P	IO	AH12	2J	YES		
150	B2A_LVDS_6_N	IO	AD14	2A	YES		
151	B2J_LVDS_6_P	IO	AH13	2J	YES		
152	B2A_LVDS_2_N	IO	AE14	2A	YES		

Pin	Net Name	Type	FPGA Ball	FPGA Bank	LVDS?	Optional Function	Notes
153	B2J_LVDS_6_N	IO	AG13	2J	YES		
154	B2A_LVDS_2_P	IO	AE15	2A	YES		
155	B2A_LVDS_1_N	IO	AE10	2A	YES		
156	B2A_LVDS_23_P	IO	AA12	2A	YES		
157	B2A_LVDS_1_P	IO	AE11	2A	YES		
158	B2A_LVDS_23_N	IO	AA13	2A	YES		
159	GND	P	-				
160	GND	P	-				
161	B2J_LVDS_1_N	IO	AG9	2J	YES		
162	B2A_LVDS_19_N	IO	AA11	2A	YES		
163	B2J_LVDS_1_P	IO	AG10	2J	YES		
164	B2A_LVDS_19_P	IO	AB11	2A	YES		
165	B2A_LVDS_5_N	IO	AF11	2A	YES		
166	B2A_LVDS_13_N	IO	AA16	2A	YES	CLK_2A_0n	
167	B2A_LVDS_5_P	IO	AF12	2A	YES		
168	B2A_LVDS_13_P	IO	AB16	2A	YES	CLK_2A_0p	
169	B2J_LVDS_10_N	IO	Y17	2J	YES	PLL_2J_CLKOUT1n	
170	B2A_LVDS_24_N	IO	AC11	2A	YES		
171	B2J_LVDS_10_P	IO	AA17	2J	YES	PLL_2J_CLKOUT1p, PLL_2J_CLKOUT1, PLL_2J_FB1	
172	B2A_LVDS_24_P	IO	AC12	2A	YES		
173	B2A_LVDS_9_P	IO	AF13	2A	YES		
174	B2A_LVDS_21_N	IO	AB15	2A	YES		
175	B2A_LVDS_9_N	IO	AF14	2A	YES		
176	B2A_LVDS_21_P	IO	AC15	2A	YES		
177	GND	P	-				
178	GND	P	-				
179	B2A_LVDS_12_P	IO	AG14	2A	YES	CLK_2A_1p	
180	B2A_LVDS_3_N	IO	AD15	2A	YES		
181	B2A_LVDS_12_N	IO	AG15	2A	YES	CLK_2A_1n	
182	B2A_LVDS_3_P	IO	AE16	2A	YES		
183	B2A_LVDS_11_N	IO	AF16	2A	YES		

Pin	Net Name	Type	FPGA Ball	FPGA Bank	LVDS?	Optional Function	Notes
184	B2A_LVDS_15_P	IO	AC16	2A	YES	PLL_2A_CLKOUT0p, PLL_2A_CLKOUT0, PLL_2A_FB0	
185	B2A_LVDS_11_P	IO	AG16	2A	YES	RZQ_2A	
186	B2A_LVDS_15_N	IO	AC17	2A	YES	PLL_2A_CLKOUT0n	
187	B2A_LVDS_8_P	IO	AF17	2A	YES		
188	B2J_LVDS_13_N	IO	AB20	2J	YES	CLK_2J_0n	
189	B2A_LVDS_8_N	IO	AF18	2A	YES		
190	B2J_LVDS_13_P	IO	AC20	2J	YES	CLK_2J_0p	
191	B2A_LVDS_7_P	IO	AG18	2A	YES		
192	B2J_LVDS_15_N	IO	AB21	2J	YES	PLL_2J_CLKOUT0n	
193	B2A_LVDS_7_N	IO	AF19	2A	YES		
194	B2J_LVDS_15_P	IO	AC21	2J	YES	PLL_2J_CLKOUT0p, PLL_2J_CLKOUT0, PLL_2J_FB0	
195	GND	P	-				
196	GND	P	-				
197	B2J_LVDS_18_P	IO	AG19	2J	YES		
198	B2J_LVDS_22_P	IO	AC23	2J	YES		
199	B2J_LVDS_18_N	IO	AG20	2J	YES		
200	B2J_LVDS_22_N	IO	AB23	2J	YES		
201	B2J_LVDS_16_N	IO	AE21	2J	YES		
202	B2A_LVDS_17_N	IO	AD17	2A	YES		
203	B2J_LVDS_16_P	IO	AF21	2J	YES		
204	B2A_LVDS_17_P	IO	AE17	2A	YES		
205	B2A_LVDS_20_P	IO	AB14	2A	YES		
206	B2A_LVDS_16_P	IO	AD18	2A	YES		
207	B2A_LVDS_20_N	IO	AA14	2A	YES		
208	B2A_LVDS_16_N	IO	AC18	2A	YES		
209	B2J_LVDS_23_N	IO	AE22	2J	YES		
210	B2J_LVDS_11_N	IO	Y19	2J	YES		
211	B2J_LVDS_23_P	IO	AF22	2J	YES		
212	B2J_LVDS_11_P	IO	Y20	2J	YES	RZQ_2J	
213	GND	P	-				

Pin	Net Name	Type	FPGA Ball	FPGA Bank	LVDS?	Optional Function	Notes
214	GND	P	-				
215	B2J_LVDS_12_P	IO	AA18	2J	YES	CLK_2J_1p	
216	B2A_LVDS_10_P	IO	AE19	2A	YES	PLL_2A_CLKOUT1p, PLL_2A_CLKOUT1, PLL_2A_FB1	
217	B2J_LVDS_12_N	IO	AA19	2J	YES	CLK_2J_1n	
218	B2A_LVDS_10_N	IO	AE20	2A	YES	PLL_2A_CLKOUT1n	
219	B2J_LVDS_3_N	IO	AH15	2J	YES		
220	B2J_LVDS_9_P	IO	AB18	2J	YES		
221	B2J_LVDS_3_P	IO	AH16	2J	YES		
222	B2J_LVDS_9_N	IO	AB19	2J	YES		
223	B2J_LVDS_7_N	IO	Y21	2J	YES		
224	B2A_LVDS_14_N	IO	AD19	2A	YES		
225	B2J_LVDS_7_P	IO	AA21	2J	YES		
226	B2A_LVDS_14_P	IO	AD20	2A	YES		
227	B2J_LVDS_2_N	IO	AH17	2J	YES		
228	B2J_LVDS_21_N	IO	AA22	2J	YES		
229	B2J_LVDS_2_P	IO	AH18	2J	YES		
230	B2J_LVDS_21_P	IO	AA23	2J	YES		
231	GND	P	-				
232	GND	P	-				
233	B2J_LVDS_19_P	IO	AG23	2J	YES		
234	B2A_LVDS_22_P	IO	AC13	2A	YES		
235	B2J_LVDS_19_N	IO	AF23	2J	YES		
236	B2A_LVDS_22_N	IO	AB13	2A	YES		
237	B2J_LVDS_14_N	IO	AH20	2J	YES		
238	B2J_LVDS_24_N	IO	AC22	2J	YES		
239	B2J_LVDS_14_P	IO	AH21	2J	YES		
240	B2J_LVDS_24_P	IO	AD22	2J	YES		
241	B2A_LVDS_18_N	IO	Y15	2A	YES	CLKUSR	Default 100 MHz 1.8V output clock. See Note 1.
242	B2J_LVDS_20_N	IO	AD23	2J	YES		
243	B2A_LVDS_18_P	IO	Y16	2A	YES		

Pin	Net Name	Type	FPGA Ball	FPGA Bank	LVDS?	Optional Function	Notes
244	B2J_LVDS_20_P	IO	AE23	2J	YES		
245	B2J_LVDS_17_N	IO	AG21	2J	YES		
246	B2J_LVDS_8_P	IO	W20	2J	YES		
247	B2J_LVDS_17_P	IO	AH22	2J	YES		
248	B2J_LVDS_8_N	IO	W21	2J	YES		
249	GND	P	-				
250	GND	P	-				
251	GND	P	-				
252	GND	P	-				
253	RESERVED	-	-				
254	RESERVED	-	-				
255	RESERVED	-	-				
256	RESERVED	-	-				
257	SCL_1V8	IO	AH2	3A	N/A		Level Converted, Shared Bus with Factory Configuration EEPROM,1K pullup to +1.8V
258	ADC0	AI	E10	0	N/A		Single ended input.
259	SDA_1V8	IO	AH3	3A	N/A		Level Converted, Shared Bus with Factory Configuration EEPROM,1K pullup to +1.8V
260	ADC1	AI	F11	0	N/A		Single ended input.

Note 1: Pin 241, B2A_LVDS_18_N, is connected to FPGA Ball Y15. This pin is a dual-purpose IO pin as well as the FPGA CLKUSR pin. If the transceiver ports are to be used, the CLKUSR pin must be driven with a reference clock in order to allow the FPGA to calibrate the transceiver subsystem. The MitySOM-C10G, by default after power on, drives a reference 1.8V LVCMOS 100 MHz clock on this pin. This clock may be disabled by driving the X3_ENB, pin AH2 of the FPGA, low via FPGA configuration.

Table 4 lists the connections on the Hirose FX10A-144P-SV connector interface (J2). These pins are direct connections to the transceiver pins and reference clock inputs the Banks 1C and 1D of the Cyclone 10 GX FPGA. The MitySOM-C10G does not include DC blocking capacitors. Users should refer to the Intel Cyclone 10 GX fabric termination reference diagrams and employ proper biasing and termination schemes based on the protocol used for the transceiver pairs.

Table 4 Hirose Board to Board Interface (J2) Pinout

Pin	Net Name	Type	FPGA Ball	FPGA Bank
1	GND	P		
2	GXB_1C_TX0_N	O	AG27	1C
3	GND	P		
4	GXB_1C_TX0_P	O	AG28	1C
5	GXB_1C_RX0_N	I	AF25	1C
6	GND	P		
7	GXB_1C_RX0_P	I	AF26	1C
8	GND	P		
9	GND	P		
10	GXB_1C_TX1_N	O	AE27	1C
11	GND	P		
12	GXB_1C_TX1_P	O	AE28	1C
13	GXB_1C_RX1_N	I	AD25	1C
14	GND	P		
15	GXB_1C_RX1_P	I	AD26	1C
16	GND	P		
17	GND	P		
18	GXB_1C_TX2_N	O	AC27	1C
19	GND	P		
20	GXB_1C_TX2_P	O	AC28	1C
21	GXB_1C_RX2_N	I	AB25	1C
22	GND	P		
23	GXB_1C_RX2_P	I	AB26	1C
24	GND	P		
25	GND	P		
26	GXB_1C_TX3_N	O	AA27	1C
27	GND	P		
28	GXB_1C_TX3_P	O	AA28	1C
29	GXB_1C_RX3_N	I	Y25	1C
30	GND	P		
31	GXB_1C_RX3_P	I	Y26	1C
32	GND	P		
33	GND	P		
34	GXB_1C_TX4_N	O	W27	1C
35	GND	P		
36	GXB_1C_TX4_P	O	W28	1C
37	GXB_1C_RX4_N	I	V25	1C
38	GND	P		
39	GXB_1C_RX4_P	I	V26	1C

Pin	Net Name	Type	FPGA Ball	FPGA Bank
40	GND	P		
41	GND	P		
42	GXB_1C_TX5_N	O	U27	1C
43	GND	P		
44	GXB_1C_TX5_P	O	U28	1C
45	GXB_1C_RX5_N	I	T25	1C
46	GND	P		
47	GXB_1C_RX5_P	I	T26	1C
48	GND	P		
49	GND	P		
50	GXB_1D_TX0_N	O	R27	1D
51	GND	P		
52	GXB_1D_TX0_P	O	R28	1D
53	GXB_1D_RX0_N	I	P25	1D
54	GND	P		
55	GXB_1D_RX0_P	I	P26	1D
56	GND	P		
57	GND	P		
58	GXB_1D_TX1_N	O	N27	1D
59	GND	P		
60	GXB_1D_TX1_P	O	N28	1D
61	GXB_1D_RX1_N	I	M25	1D
62	GND	P		
63	GXB_1D_RX1_P	I	M26	1D
64	GND	P		
65	GND	P		
66	GXB_1D_TX2_N	O	L27	1D
67	GND	P		
68	GXB_1D_TX2_P	O	L28	1D
69	GXB_1D_RX2_N	I	K25	1D
70	GND	P		
71	GXB_1D_RX2_P	I	K26	1D
72	GND	P		
73	GND	P		
74	GXB_1D_TX3_N	O	J27	1D
75	GND	P		
76	GXB_1D_TX3_P	O	J28	1D
77	GXB_1D_RX3_N	I	H25	1D
78	GND	P		
79	GXB_1D_RX3_P	I	H26	1D
80	GND	P		
81	GND	P		
82	GXB_1D_TX4_N	O	G27	1D
83	GND	P		
84	GXB_1D_TX4_P	O	G28	1D
85	GXB_1D_RX4_N	I	F25	1D
86	GND	P		
87	GXB_1D_RX4_P	I	F26	1D
88	GND	P		

Pin	Net Name	Type	FPGA Ball	FPGA Bank
89	GND	P		
90	GXB_1D_TX5_N	O	E27	1D
91	GND	P		
92	GXB_1D_TX5_P	O	E28	1D
93	GXB_1D_RX5_N	I	D25	1D
94	GND	P		
95	GXB_1D_RX5_P	I	D26	1D
96	GND	P		
97	GND	P		
98	REFCLK_1C_BOT_P	I	W24	1C
99	GND	P		
100	REFCLK_1C_BOT_N	I	W23	1C
101	RESERVED	-		
102	GND	P		
103	RESERVED	-		
104	GND	P		
105	GND	P		
106	REFCLK_1C_TOP_P	I	U24	1C
107	GND	P		
108	REFCLK_1C_TOP_N	I	U23	1C
109	RESERVED	-		
110	GND	P		
111	RESERVED	-		
112	GND	P		
113	GND	P		
114	REFCLK_1D_BOT_P	I	R24	1D
115	GND	P		
116	REFCLK_1D_BOT_N	I	R23	1D
117	RESERVED	-		
118	GND	P		
119	RESERVED	-		
120	GND	P		
121	GND	P		
122	REFCLK_1D_TOP_P	I	N24	1D
123	GND	P		
124	REFCLK_1D_TOP_N	I	N23	1D
125	RESERVED	-		
126	GND	P		
127	RESERVED	-		
128	GND	P		
129	GND	P		
130	RESERVED	-		
131	GND	P		
132	RESERVED	-		
133	RESERVED	-		
134	GND	P		
135	RESERVED	-		
136	GND	P		
137	GND	P		

Pin	Net Name	Type	FPGA Ball	FPGA Bank
138	RESERVED	-		
139	GND	P		
140	RESERVED	-		
141	RESERVED	-		
142	RESERVED	-		
143	RESERVED	-		
144	RESERVED	-		

The on-board FPGA connections to the SPI NOR FLASH, the DDR3L RAM, and the I2C EEPROM are listed in Table 5.

Table 5 MitySOM-C10G Internal FPGA functional connections

FPGA Ball	Bank	Connection	IO Voltage	Notes
W4	3A	DDR_DQ1	1.35V	Connected to on-board DDR3.
Y4	3A	DDR_DQ4	1.35V	Connected to on-board DDR3.
W7	3A	DDR_DQ5	1.35V	Connected to on-board DDR3.
Y7	3A	DDR_DQ7	1.35V	Connected to on-board DDR3.
Y6	3A	DDR_DQ3	1.35V	Connected to on-board DDR3.
W5	3A	DDR_DQS0_P	1.35V	Connected to on-board DDR3.
Y5	3A	DDR_DQS0_N	1.35V	Connected to on-board DDR3.
Y1	3A	DDR_DQ0	1.35V	Connected to on-board DDR3.
Y2	3A	DDR_DQ6	1.35V	Connected to on-board DDR3.
AA9	3A	DDR_DQ2	1.35V	Connected to on-board DDR3.
AA8	3A	DDR_DM0	1.35V	Connected to on-board DDR3.
AB4	3A	DDR_DQ24	1.35V	Connected to on-board DDR3.
AB1	3A	DDR_DQ27	1.35V	Connected to on-board DDR3.
AA1	3A	DDR_DQ29	1.35V	Connected to on-board DDR3.
AB6	3A	DDR_DQ28	1.35V	Connected to on-board DDR3.
AB5	3A	DDR_DQ30	1.35V	Connected to on-board DDR3.
AA2	3A	DDR_DQS3_P	1.35V	Connected to on-board DDR3.
AB3	3A	DDR_DQS3_N	1.35V	Connected to on-board DDR3.
AA3	3A	DDR_DQ26	1.35V	Connected to on-board DDR3.
AA5	3A	DDR_DQ31	1.35V	Connected to on-board DDR3.
AG3	3A	DDR_DQ8	1.35V	Connected to on-board DDR3.
AF3	3A	DDR_DQ14	1.35V	Connected to on-board DDR3.
AF1	3A	DDR_DQ12	1.35V	Connected to on-board DDR3.
AE2	3A	DDR_DQS1_P	1.35V	Connected to on-board DDR3.
AD2	3A	DDR_DQS1_N	1.35V	Connected to on-board DDR3.
AC1	3A	DDR_DQ11	1.35V	Connected to on-board DDR3.
AC2	3A	DDR_DQ13	1.35V	Connected to on-board DDR3.
AE1	3A	DDR_DQ9	1.35V	Connected to on-board DDR3.
AF2	3A	DDR_DQ10	1.35V	Connected to on-board DDR3.
AD3	3A	DDR_DQ15	1.35V	Connected to on-board DDR3.
AC3	3A	DDR_DM1	1.35V	Connected to on-board DDR3.

FPGA Ball	Bank	Connection	IO Voltage	Notes
AA6	3A	DDR_DM3	1.35V	Connected to on-board DDR3.
AA7	3A	DDR_DQ25	1.35V	Connected to on-board DDR3.
P3	3B	DDR_DQ21	1.35V	Connected to on-board DDR3.
P4	3B	DDR_DQ23	1.35V	Connected to on-board DDR3.
T8	3B	DDR_DQ22	1.35V	Connected to on-board DDR3.
T9	3B	DDR_DM2	1.35V	Connected to on-board DDR3.
T6	3B	DDR_DQ19	1.35V	Connected to on-board DDR3.
T7	3B	DDR_DQ17	1.35V	Connected to on-board DDR3.
R4	3B	DDR_DQS2_P	1.35V	Connected to on-board DDR3.
R5	3B	DDR_DQS2_N	1.35V	Connected to on-board DDR3.
U5	3B	DDR_DQ20	1.35V	Connected to on-board DDR3.
U8	3B	DDR_DQ18	1.35V	Connected to on-board DDR3.
V8	3B	DDR_DQ16	1.35V	Connected to on-board DDR3.
M3	3B	DDR_BA1	1.35V	Connected to on-board DDR3.
M4	3B	DDR_BA2	1.35V	Connected to on-board DDR3.
K4	3B	DDR_CASN	1.35V	Connected to on-board DDR3.
L4	3B	DDR_BA0	1.35V	Connected to on-board DDR3.
N2	3B	DDR_A15	1.35V	Connected to on-board DDR3.
N3	3B	DDR_RASN	1.35V	Connected to on-board DDR3.
H2	3B	DDR_A13	1.35V	Connected to on-board DDR3.
J3	3B	DDR_A14	1.35V	Connected to on-board DDR3.
J2	3B	DDR_A12	1.35V	Connected to on-board DDR3.
L2	3B	CLK_233_N	1.35V	Connected to on-board DDR3.
L3	3B	CLK_233_P	1.35V	Connected to on-board DDR3.
W3	3B	DDR_WEN	1.35V	Connected to on-board DDR3.
V3	3B	DDR_RESET_N	1.35V	Connected to on-board DDR3.
W2	3B	DDR_CSN	1.35V	Connected to on-board DDR3.
V5	3B	DDR_ODT	1.35V	Connected to on-board DDR3.
U6	3B	DDR_CKE	1.35V	Connected to on-board DDR3.
V1	3B	DDR_CK_P	1.35V	Connected to on-board DDR3.
U1	3B	DDR_CK_N	1.35V	Connected to on-board DDR3.
T1	3B	DDR_A0	1.35V	Connected to on-board DDR3.
R1	3B	DDR_A1	1.35V	Connected to on-board DDR3.
L1	3B	DDR_A2	1.35V	Connected to on-board DDR3.
K1	3B	DDR_A3	1.35V	Connected to on-board DDR3.
T2	3B	DDR_A4	1.35V	Connected to on-board DDR3.
T3	3B	DDR_A5	1.35V	Connected to on-board DDR3.
R2	3B	DDR_A6	1.35V	Connected to on-board DDR3.
P2	3B	DDR_A7	1.35V	Connected to on-board DDR3.
H1	3B	DDR_A8	1.35V	Connected to on-board DDR3.
G1	3B	DDR_A9	1.35V	Connected to on-board DDR3.
N1	3B	DDR_A10	1.35V	Connected to on-board DDR3.
M1	3B	DDR_A11	1.35V	Connected to on-board DDR3.
AD9	CSS	QSPI_CLK	1.8V	Connected to on-board QSPI NOR.
AH5	CSS	QSPI_DQ3	1.8V	Connected to on-board QSPI NOR.

FPGA Ball	Bank	Connection	IO Voltage	Notes
AG5	CSS	QSPI_DQ2	1.8V	Connected to on-board QSPI NOR.
AG6	CSS	QSPI_DQ1	1.8V	Connected to on-board QSPI NOR.
AE9	CSS	QSPI_DQ0	1.8V	Connected to on-board QSPI NOR.
AH8	CSS	QSPI_SS0	1.8V	Includes 10k pullup to 1.8V
AG1	3A	SCL	1.8V	Level Converted to 1.8V
AH3	3A	SDA	1.8V	Level Converted to 1.8V

The Voltage Reference and On-Chip Termination (OCT) calibration are not brought to the DDR4 edge connector and have been connected on the MitySOM-C10G according to Table 6.

Table 6 MitySOM-C10G FPGA Internal Connections for various VREF and OCT Calibration pins

FPGA Ball	Bank	Connection	Pin Function	Notes
K2	3B	240 ohm pull-down to ground.	DDR3 RZQ	Needed for on-chip termination.
AH2	3A	Calibration Clock Enable*	X3_ENB	Used to drive 100 MHz USRCLK on Y15.
AF6	3A	Logic Reset/QSPI Reset Input (active low).	LOGIC_RESETn	Asserted when PROC_RESET is asserted.
U9	3B	0.675 Volts	VREFB3BN0	
W9	3A	0.675 Volts	VREFB3AN0	
K16	2L	0.9 Volts	VREFB2LN0	
E9	2K	0.9 Volts	VREFB2KN0	
W17	2J	0.9 Volts	VREFB2JN0	
W15	2A	0.9 Volts	VREFB2AN0	

ELECTRICAL CHARACTERISTICS

Table 7 lists the Power Supply Input voltage levels and current consumption. The current consumption of the FPGA portion of the SOM is highly dependent on the application. Users are strongly encouraged to examine the Power Estimate provide by the Intel FPGA design suite (Quartus Prime Pro).

Table 7: Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIN	Voltage supply, volt input.		4.8	5.0	5.15	Volts
$I_{5.0}$	Quiescent Current draw	5.0 volt input		TBS		mA
$I_{5.0\text{-}max}$	Max current draw	5.0 volt input		TBS	TBS	mA
	1. Power utilization of the MitySOM-C10G is heavily dependent on end-user application.					

ORDERING INFORMATION

The following table lists the standard module configurations. For shipping status, availability, and lead time of these configurations please contact Critical Link(info@criticallink.com) or visit one of our authorized distributors.

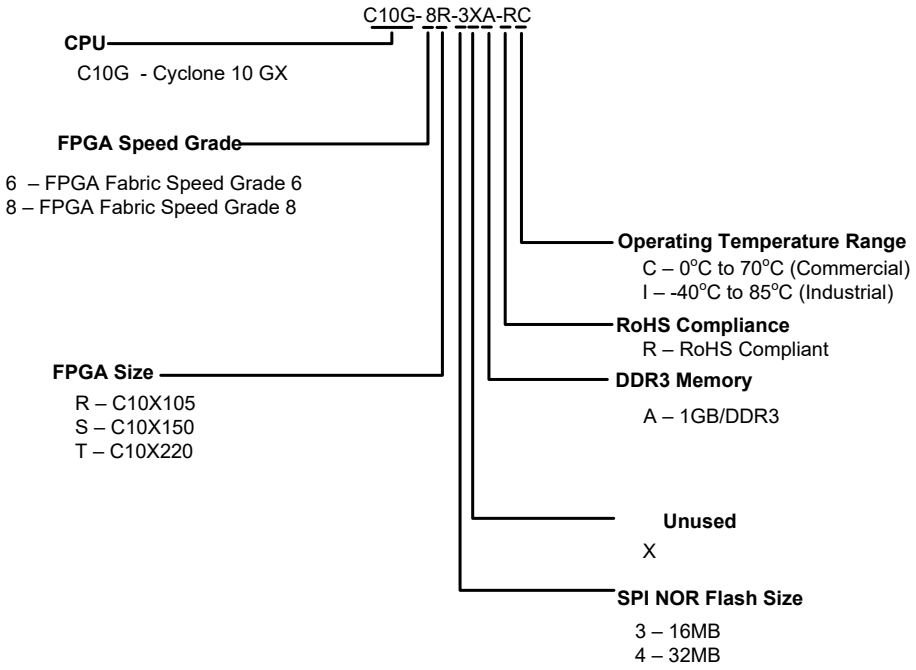
Table 8: Standard Model Numbers

Model	Speed Grade	DDR3L	FPGA KLE	NOR	Temperature Ratings
C10G-8R-4XA-RI	8	1 GB	105	32MB	-40ºC to 85º C
C10G-6T-4XA-RI	6	1 GB	220	32MB	-40ºC to 85º C

MitySOM-C10G Module Family Model Number Guide

If a module suitable for your specific application is not found in Table 8 please reference the following MitySOM-C10G model number decoder for configuring a custom module. Please contact your Critical Link representative to determine pricing, lead-time and availability of a custom module.

Figure 3 MitySOM-C10G Model Number Decoder



MECHANICAL INTERFACE

A top view of the mechanical outline of the MitySOM-C10G is illustrated in Figure 4. The figure provides outer module dimensions and the location of the 2 mounting holes opposite the SODDR4 edge connector interface.

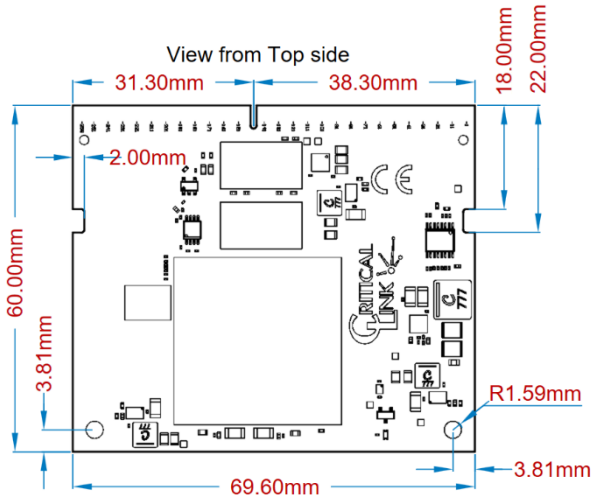


Figure 4 MitySOM-C10G Mechanical Outline, Top Side View

A bottom view of the mechanical outline of the MitySOM-C10G is illustrated in Figure 5. The figure provides the location and orientation (via pin numbers) of J2, the Hirose board to board connector providing access to the transceiver pins. It is important to note that the reference the X (left/right) orientation of J2 is the center of the edge connector alignment slot, and the Y orientation of J2 is referenced to the edge of the board along the edge connector side, as shown.

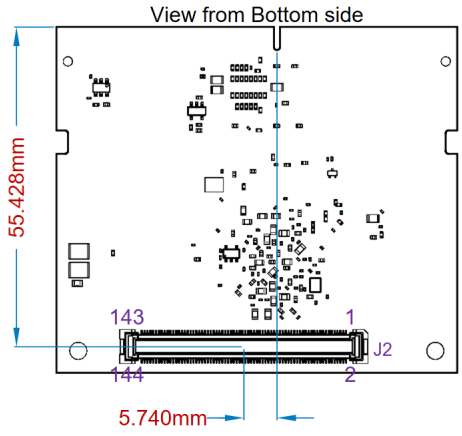


Figure 5 MitySOM-C10G Mechanical Outline, Bottom Side View

Figure 6 illustrates the recommended carrier card layout for the edge connector, Hirose Connector, and (optional) mounting hole positions for mating to the MitySOM-C10G SOM. The dimensions shown are referenced to the centers of the alignment pins of the connectors and center positions of the alignment holes.

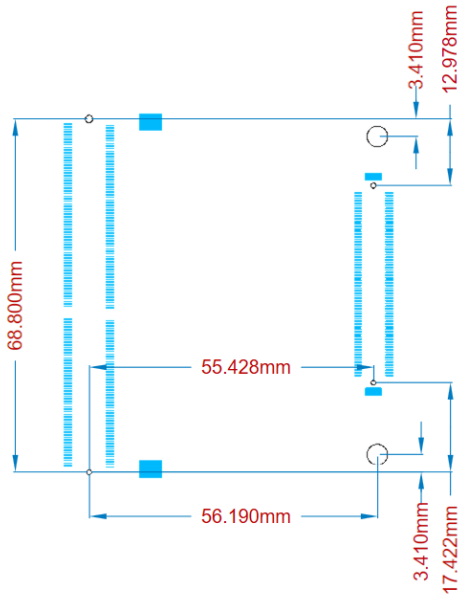


Figure 6 Carrier Card Edge Connector, Hirose Connector, and Mounting Hole Locations

REVISION HISTORY

Date	Revision	Change Description
05-MAY-2023	-	Preliminary revision shared by marketing
14-JULY-2023	1A	Initial release. Corrects pinout tables, multiple revisions following page 2.