MitySOM™ Document

Document: MitySOM-AM62 Carrier Board Design Guide

Revision: 1.0

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1 Overview

1.1 Fast Facts for Getting Started

Facts	MitySOM-AM62
Required socket connector	JEDEC SO-DIMM DDR4 compatible socket connector, 5.2mm height or taller
Voltage required	3.3V, switched 3.3V or 1.8V for IO interfaces
A53 MPU Serial Peripherals*	5x UART, 3x SPI, 3x I2C, 3x McASP, 1x CAN, 2x USB, 2x EMAC (MII or RMII or RGMII)
A53 MPU Display Peripherals*	1x 24-bit parallel video output, 2x 4 lane Open LVDS Display Interface channels
A53 MPU Other Peripherals*	4x Timer, 3x eHRPWM, 3x eQEP, 3x eCAP
MCU Peripherals*	2x CAN, 1x UART, 2x SPI, 1x I2C
PRU Peripherals**	UART, MII/MDIO, eCAP
*Peripherals share pins, see AM62x datasheet and Appendix for specific pin-multiplexing options ** PRU is not always available, see AM62x and MitySOM-AM62 datasheet for details.	

1.2 Introduction

The MitySOM-AM62 family of modules are System on Modules (SOMs) designed to be easy to integrate into an end-user embedded system. The modules integrate many crucial elements of an embedded system and do so with an established design framework utilizing a common set of core libraries. End-user design of the application PCB is also intended to be as simple as possible, allowing the PCB designer to concentrate on the custom I/O interfaces – especially analog & mixed-signal – instead of getting distracted with the learning curve of designing a brand new embedded digital system from scratch.

Developers are encouraged to review the MitySOM-AM62 Development Kit design schematics, available on the Critical Link support site. The Development Kit has been qualified and there is a full software support package already available for the interfaces on the board. Customers interested in the Altium CAD design files for the kit should contact Critical Link for access.

1.4 Links to Important Documents and Information

There are many useful documents and resources available that can be referenced when designing a system with the MitySOM-AM62 module which are listed below. It is recommended that the information on the TI webpages be reviewed often for updates.

MitySOM-AM62 Data Sheet	https://www.criticallink.com/wp-content/uploads/MitySOM-AM62_Datasheet.pdf
MitySOM-AM62 Support Site	https://support.criticallink.com/redmine/projects/mitysom_am62x/wiki
AM62x Data sheet	https://www.ti.com/lit/gpn/am625
AM62x Technical Reference Manual	https://www.ti.com/lit/pdf/spruiv7
AM62x "Home" Page	https://www.ti.com/product/AM625
TPS65219 PMIC Data Sheet	https://www.ti.com/lit/gpn/tps65219
TPS6521903 Technical Reference Manual	https://www.ti.com/lit/pdf/slvucj2?keyMatch=TPS6521903

2 Connectors

The MitySOM-AM62 utilizes a 260 pin, SO-DIMM DDR4 style edge-connector for connectivity with the end user application PCB. This connector was chosen for its high density, compact size, ease of procurement, and low cost. With edge connectors, a physical socket component is only required on one side – the main PCB side. The SO-DIMM standard also allows the MitySOM-AM62 module to lay flat, in parallel with the main PCB as they were intended for use by memory modules in compact equipment, such as laptops. Other connector styles are available that also allow for vertically mounting the MitySOM-AM62.

2.1 Card-edge compatibility

The MitySOM-AM62 is designed to plug into a 260 -pin SO-DIMM DDR4 RAM socket. These sockets are commonly used for memory in PC products. Please note that the MitySOM-AM62 is NOT electrically compatible with the DDR4 socket standard. Intermixing modules/sockets from the two standards would very possibly cause permanent damage to one or both sides.

3 Electrical Requirements

The following sections describe the various electrical requirements for the MitySOM-AM62 module.

3.1 Power Supplies

Figure 2 provides an overview of the MitySOM-AM62 power scheme. The module takes advantage of a TPS65219 power management IC (PMIC), which requires a 3.3V input. The PMIC generates all on-module supplies needed to power the processor, DDR4 memory, and FLASH memories. The PMIC includes a 1.8V buck regulator output that is connected to the SO-DIMM DDR4 edge connector that may be used for 1.8V IO and peripherals on the carrier card. To support Ultra High Speeds (UHS) on the exposed AM62x MMC1 interface, the VDDSHV5 bank and IO pins must be switched from 3.3V to 1.8V during operation. This is accomplished through an exposed control pin, VSEL_SD, and power output pin, VDDSHV_SDIO. The VDDSHV_SDIO output is provided on the SO-DIMM edge connector to support pulling up the MMC1 data and IO lines to the correct runtime voltage based on the selected MMC1 speed.

The MitySOM-AM62 exposes the AM62x processor VDDSHV2, VDDSVH3, VDDSHV6, and VDDSHV_MCU bank supply inputs on the external SO-DIMM DDR4 edge connector. This allows the designer to select either 3.3V or 1.8V for IO pins on these banks. The bank assignment for each IO pin can be determined from Table 1 of the MitySOM-AM62 datasheet and additional information about the VDDSHV Bank voltages can be found in the TI AM62x datasheet.

For secure key programming, a 1.8V supply is required on the VPP pin of the SO-DIMM DDR4 edge connector. This supply should only be provided while the secure keys are actively being programmed. Otherwise, this input should be pulled to ground with a pull-down resistor.

Figure 3 illustrates a typical carrier card power block diagram.

3.1.1 Power Supply Sequencing

The MitySOM-AM62 power inputs should be sequenced when powered on. There are three power groups for sequencing: the main 3.3V input, the VDDSHVXX bank inputs and IO pins to be run at 3.3V, and (optionally) the VDDSHVXX bank inputs and IO pins to be run at 1.8V. The enabling of the 3.3V and 1.8V bank IO voltages can be accomplished using the VDD_3V3_ENABLE (as a control pin to a load switch or MOSFET gate input) and VDD_1V8 SOM output pins as shown in Figure 1.

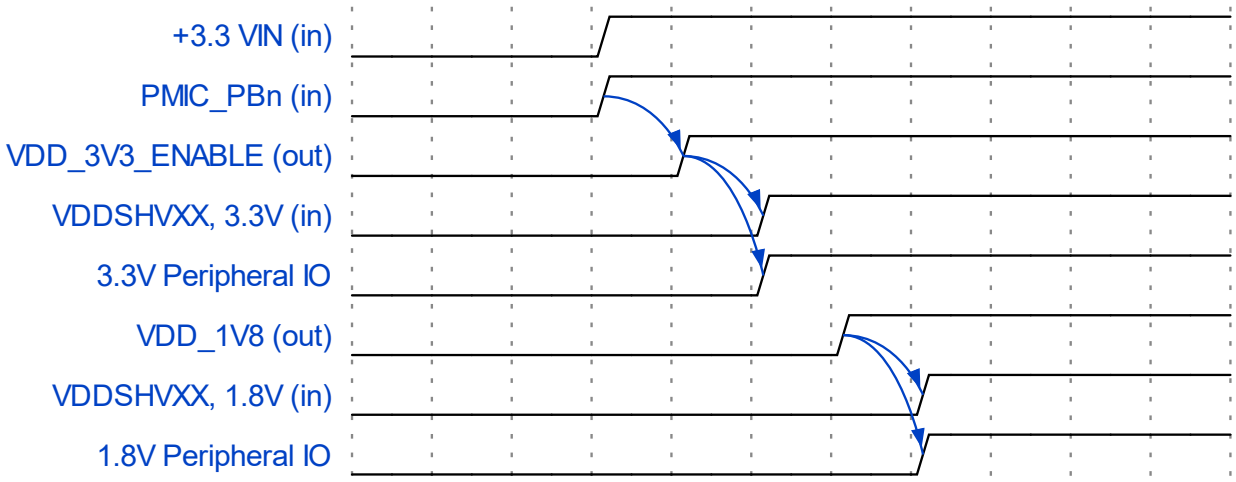

Figure 1: Example MitySOM-AM62 SOM Power Up Sequence Requirements

For switching the +3.3V main input supply onto the relevant VDDSHV Bank pins and powering the peripheral IO, Critical Link chose to use a simple load switch, NCP451AFCT2G, on the development kit. For the 1.8V peripheral IO, the MitySOM-AM62 VDD_1V8 output was used directly as the current requirements matched the supply capability.

Utilizing the VDD_3V3_ENABLE and the VDD_1V8 output from the SOM will allow the processor to initiate a power down sequence that allows the PMIC to shutdown the SOM components (processor, RAM, etc.) as well as the associated peripheral IO on the carrier card in an orderly fashion. By default, the system software will recognize a button press on the PMIC_PBn as a request to power down the system. When off, a a request greater than 600 ms and less than 8 seconds on the PMIC_PBn will cause the TPS65219 to initiate a power on sequence to reboot the processor.

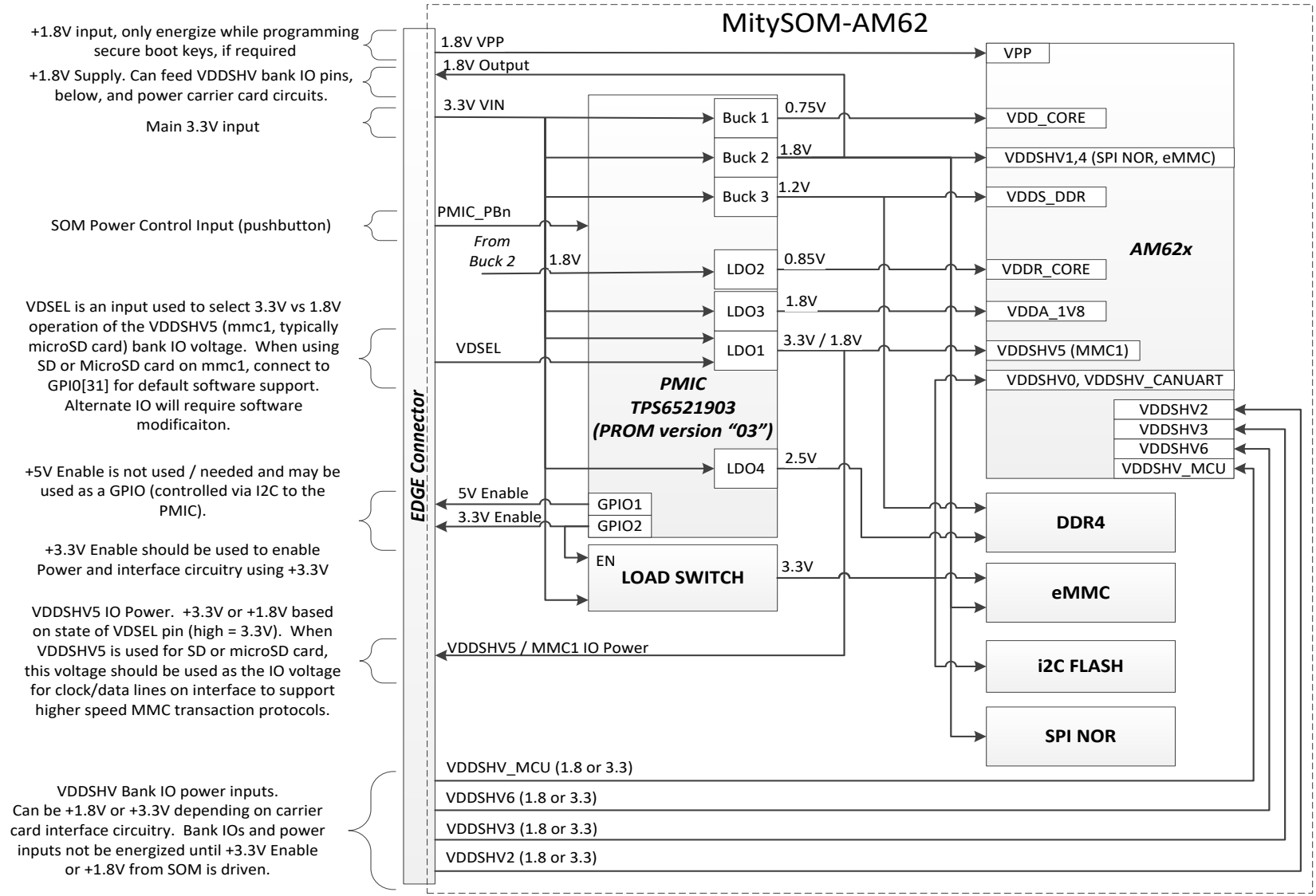

Figure 2 MitySOM-AM62 Power Interface Overview

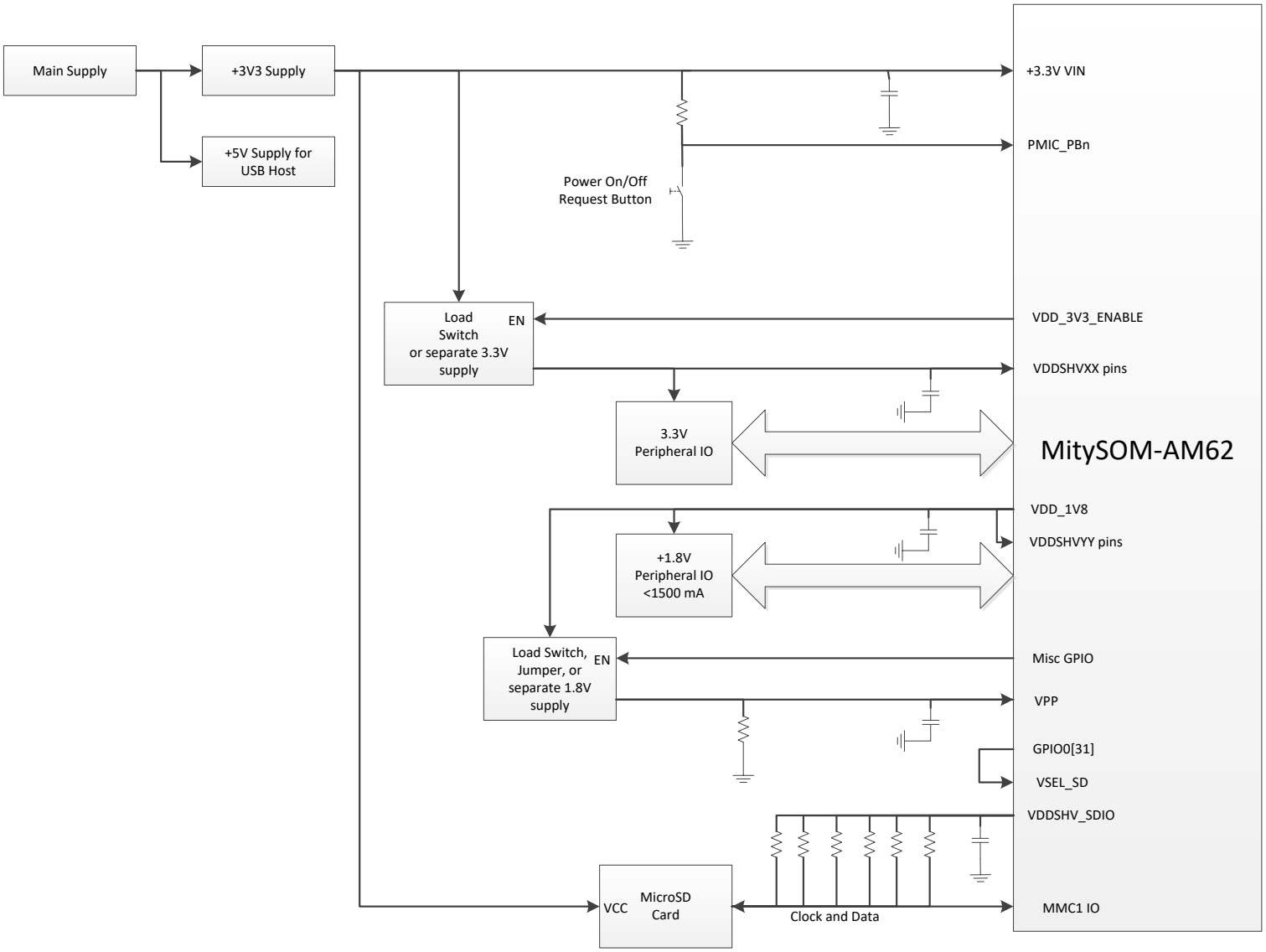

Figure 3 Typical MitySOM-AM62 Carrier Card Power Block Diagram

3.2 Recommended Capacitance

The MitySOM-AM62 module includes some power supply rail bypass capacitors on-board, however additional capacitance is recommended on the carrier board to minimize the ripple effect caused by changing load currents. It is recommended to place at least 20 µF in bulk capacitors nearby the main +3.3V VIN pins in addition to whatever bulk capacitance is recommended for your main 3.3V rail supply design. For each of the VDDSHVXX bank inputs, at least 10 µF in bulk capacitors is recommended. Please note that this is the minimum recommended amount of additional capacitance, and more is typically better.

3.3 I/O Interfaces

The I/O pins directly connected to the AM62x processor can be grouped into the following power domains:

- The USB interfaces – These interfaces utilize low voltage differential signaling input/output in accordance with the USB standard. Data lines should be routed using 90-ohm differential impedance.
- MIPI input interface - These interfaces utilize low voltage differential signaling inputs in accordance with the MIPI D-PHY / CSI standard. Data and clock lines should be routed using 100-ohm differential impedance and be matched in length. Note: MIPI/D-PHY clock and data lanes support data polarity inversion (though not tested/demonstrated on the Development Kit). Data lanes are in fixed order (data lanes may not be shuffled).
- Open LVDS Display Interface(OLDI) – These interfaces utilize low voltage differential signaling outputs and may be used to drive several displays utilizing 3 data (plus 1 clock) to 6 data (plus 2 clock) lanes. Data and clock lines should be routed using 100-ohm differential impedance and be matched in length.
- All AM62x processor I/O pins powered from the VDDSHV2 power domain – These pins can be powered from either 1.8 volts or 3.3 volts as required by the application. For 1.8V operation, the MitySOM-AM62 provides 1.8 volt power on pins VDD_1V8 which can be connected to the VDDSHV2 pins on the connector and to drive the 1.8V peripheral IO pins on the carrier card. For 3.3V operation, the MitySOM-AM62 provides an enable pin, VDD_3V3_ENABLE, which may be used to sequence a 3.3V load switch or separate 3.3V supply on the carrier card to connect to the VDDSHV2 pins and peripheral IO.
- All AM62x processor I/O pins powered from the VDDSHV3 power domain – These pins can be powered from either 1.8 volts or 3.3 volts as required by the application. For 1.8V operation, the MitySOM-AM62 provides 1.8 volt power on pins VDD_1V8 which can be connected to the VDDSHV3 pins on the connector and to drive the 1.8V peripheral IO pins on the carrier card. For 3.3V operation, the MitySOM-AM62 provides an enable pin, VDD_3V3_ENABLE, which may be used to sequence a 3.3V load switch or separate 3.3V supply on the carrier card to connect to the VDDSHV3 pins and peripheral IO.
- All AM62x processor I/O pins powered from the VDDSHV5 power domain – These pins are powered from an LDO connected to the MitySOM-AM62 on-board PMIC, which can be either 1.8 volts or 3.3 volts

depending on the state of the MitySOM-AM62 VSEL_SD pin input. The LDO output is available on the SOM edge interface on the VDDSHV_SDIO pin. The voltage will be 3.3V when VSEL_SD is high and will be 1.8V when VSEL_SD is low. Typically, the pins on this domain are used for interfacing with a MicroSD card and provide the command, clock, and data interface pins. The voltage is changed at runtime to support switching to Ultra High Speed (UHS) clock modes on the MicroSD card device. VSEL_SD is pulled up to a sequenced +3.3V on the SOM, and in general is connected to GPIO0_31 for normal software support.

- All AM62x processor I/O pins powered from the VDDSHV6 power domain – These pins can be powered from either 1.8 volts or 3.3 volts as required by the application. For 1.8V operation, the MitySOM-AM62 provides 1.8 volt power on pins VDD_1V8 which can be connected to the VDDSHV6 pins on the connector and to drive the 1.8V peripheral IO pins on the carrier card. For 3.3V operation, the MitySOM-AM62 provides an enable pin, VDD_3V3_ENABLE, which may be used to sequence a 3.3V load switch or separate 3.3V supply on the carrier card to connect to the VDDSHV6 pins and peripheral IO.

- All AM62x processor I/O pins powered from the VDDSHV_MCU power domain – These pins can be powered from either 1.8 volts or 3.3 volts as required by the application. For 1.8V operation, the MitySOM-AM62 provides 1.8 volt power on pins VDD_1V8 which can be connected to the VDDSHV_MCU pins on the connector and to drive the 1.8V peripheral IO pins on the carrier card. For 3.3V operation, the MitySOM-AM62 provides an enable pin, VDD_3V3_ENABLE, which may be used to sequence a 3.3V load switch or separate 3.3V supply on the carrier card to connect to the VDDSHV_MCU pins and peripheral IO.

3.3.1 I/O Protection

Any I/O interfaces that are external to the MitySOM-AM62 module must be protected to ensure that no out-of-range voltage conditions occur as all I/O pins are directly connected to the AM62x processor. The host board should contain the necessary protection/isolation circuits as required to protect the processor. Please refer to the AM62x Datasheet for details about maximum voltage ranges for both 3.3V and 1.8V I/O domains as the maximum ranges are different.

3.3.2 A53 vs. M4 peripheral access

The AM62x process includes (up to) a Quad Core Arm Cortex-A53 Main Processing Unit (MPU) as well as an Arm Cortex-M4F Microcontroller Unit (MCU). The two processor subsystems are grouped with peripherals in separate domains: the main domain, and the MCU domain. This is done to allow the MCU to be able to perform fixed function, mission critical, or safety critical operations without interference and regardless of the operational state of the MPU subsystem. It is important to understand that, except for the GPIO functions, the assigned MCU peripherals (2x SPI, UART, 2x CAN, I2C) are generally not intended to be used and may not be accessible by the Cortex-A53 complex. In a similar way, the peripherals assigned to the MPU may not be accessible to the M4 complex. This is important to note during carrier board IO planning. Users are strongly

encouraged to review the AM62x datasheet and technical reference manuals for additional detail and should contact Critical Link for any clarification on this topic.

3.4 Module Boot Configuration

The MitySOM-AM62 is capable of booting from several peripherals as defined by the state of the 16 GPMC_AD[15..0] / BOOTMODE[15..0] pins at the time of a reset. The state of the 16 data lines is sampled on the rising edge of the PORz_OUT signal to determine the search order of peripherals for a valid boot image. BOOTMODE[2..0] pins are strapped (via pullup / pulldown resistors) to a logic "011" on the MitySOM-AM62 as they set clock configuration for the AM62x which is fixed by the SOM design.

The carrier card needs to set BOOTMODE[15..3] during power on reset. If the GPMC_AD/BOOTMODE pins are not driven by peripheral IO in the design, then either a 470 ohm pull up to the voltage rail connected to the VDDSHV3 SOM input pins (1.8V or 3.3V, driven by the carrier card) or a 47K pull down resistor may be used to configure the setting.

Care must be taken if the carrier card has peripheral IO that will drive the GPMC_AD[15..0]/BOOTMODE[15..0] pins. The pins must not be in contention with the intended boot configuration during power on reset. A tristate buffer may be used to drive / disable pin states in contention by using the PORz_OUT strobe: when low, assert boot configuration pins and de-assert application pins; when high, de-assert boot configuration pins and assert application pins.

A list of boot peripherals supported by the MitySOM-AM62 is shown below. The AM62x processor does have provisions for a primary boot media and a backup boot media. Users wishing to deviate from boot modes supported on the Development Kit (and documented on the Critical Link Support Site) are strongly encouraged to refer to the AM62x technical reference manual for additional information about boot configuration.

Table 1 Possible Boot Modes, MitySOM-AM62

Boot Mode	Boot Media	AM62x Interface	Can be a backup mode?	Can run on Devkit?	Notes
OSPI	OSPI Flash	OSPI	N	Y	Only MitySOM-AM62 with OSPI option codes / installed supports this boot media.
Ethernet	External Host	RGMII1 / MDIO0	Y	Y	Supports BOOTP, RMII PHY also supported.
UART	External Host	UART0	Y	Y	XMODEM protocol.

Boot Mode	Boot Media	AM62x Interface	Can be a backup mode?	Can run on Devkit?	Notes
MMCSD	SD Card	MMCSD1 (4-bit)	Y	Y	SD card detect (MMC1_SDCD) signal must be 0 for ROM bootloader to operate.
eMMC	eMMC flash	MMCSD0 (8-bit)	Y*	Y	Only MitySOM-AM62 with eMMC option codes / installed supports this boot media. * In backup mode, configuration and data rate is constrained. See Technical Reference Manual
USB – target	External Host	USB0	Y	Y	Uses device firmware upgrade (DFU) protocol.
USB – host	USB mass storage	USB0	Y	Y	Boot from FAT32 filesystem
GPMC	NOR Flash NAND Flash	GCPM0	N	N	Not recommended.

Common boot settings are shown in the table below. This is not an exhaustive list. For additional operations please consult the AM62x Technical Reference Manual or contact Critical Link.

Table 2 Common Boot Mode Settings

BOOTMODE Pins [15..0]*	Primary Boot	Secondary Boot	Notes
0000 0010 0100 0011	MicroSD on MMC1	None	Devkit configuration from factory.
0011 0101 0000 1011	OSPI	MicroSD on MMC1	
0011 0100 1100 1011	eMMC on MMC0	MicroSD on MMC1	Must use SOM with eMMC installed option.
0010 0101 0000 1011	OSPI	USB0 / Mass Storage	

BOOTMODE Pins [15..0]*	Primary Boot	Secondary Boot	Notes
0010 0100 1100 1011	eMMC on MMC0	USB0 / Mass Storage	Must use SOM with eMMC installed option.

*BOOTMODE pins 2..0 are pulled up on the SOM to select 25 MHz main reference clock. Do not drive on the carrier card.

3.5 Debugger Interface

The MitySOM-AM62 JTAG/Debugger interface is available on the I/O connector, and it is strongly recommended that this interface be wired up to a header so a debugger can be attached to the design. The Critical Link devkit uses a Samtec FTR-110-52-L-D-06 header in order to support standard JTAG pods compatible with TI AM62x processors as shown in Figure 4. Note: The MitySOM-AM62 includes 4.7K ohm pullup resistors to VDDSHV_MCU on TCK, TDI, TMS, EMU0, and EMU1 and a 4.7K ohm pulldown resistor on TRSTn such that these pins may be left unconnected on the carrier card if no JTAG interface is desired.

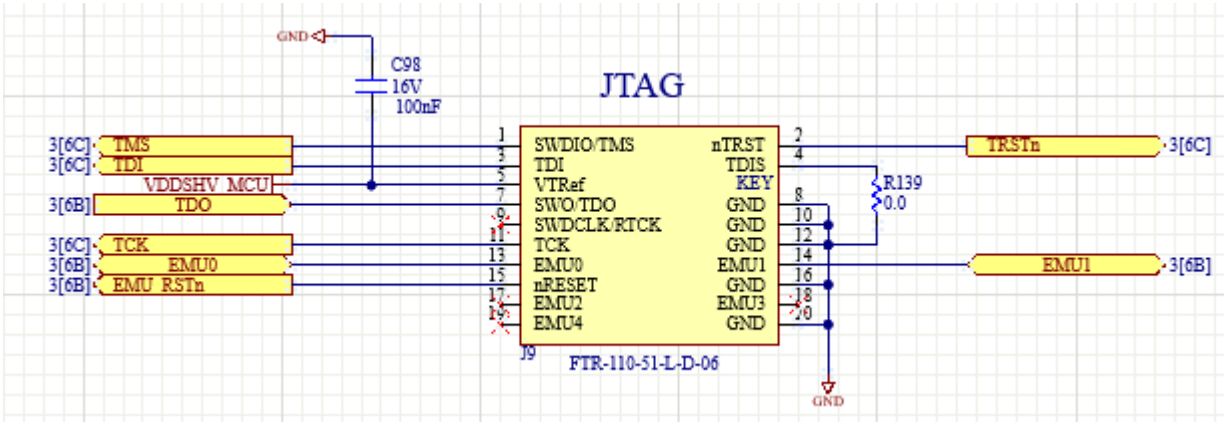

Figure 4: Typical Carrier Card JTAG/Debugger Interface

3.6 RS232 Monitor Interface

It is strongly recommended that UART0 be used as a general-purpose monitor port. All of the u-Boot console and kernel console IO data is routed to UART0 (with no HW flow control) by default in the reference software development images. Using UART0 pins for other functions will require modification of low-level boot software (e.g., U-Boot) and the kernel configuration to disable kernel logging to this port. Modern board designs typically use a USB to UART bridge chip to support standard USB style serial ports (COM ports for windows, ttyUSBX ports for Linux). The Critical Link reference design utilizes a CP2105 dual UART to USB bridge chip to interface both UART0 for the ARM Cortex-A53 console as well as MCU_UART0 to support reading text data from the MCU processor.

3.7 LED Power Return

There are two LEDs on the MitySOM-AM62. One of the LEDs (D2) is hardwired to a voltage source to indicate that the module is powered while the other LED (D1) is connected to a GPIO pin and software controlled. Some applications may require very low power or blackout conditions so the cathode of LED D2 is connected to I/O connector pin LED_RTN. This allows the LED D2 to be disabled in situations where power or visibility is a concern. Typically, the LED_RTN pin would be connected to GND which would enable both LEDs.

3.8 VSYS Monitor

The MitySOM-AM62 provides a connection at the SO-DIMM DDR interface to the AM62x VMON_SYS input pin, which is used to monitor main input supply voltage to detect potential brown-out conditions. This input should be kept within a range of 0-1V (2V absolute maximum) and has a trip point of 0.45 V. The MitySOM-AM62 development kit uses this signal to monitor the +12V main input supply to the board with the circuit shown in Figure 5. Refer to the AM62x datasheet for more information.

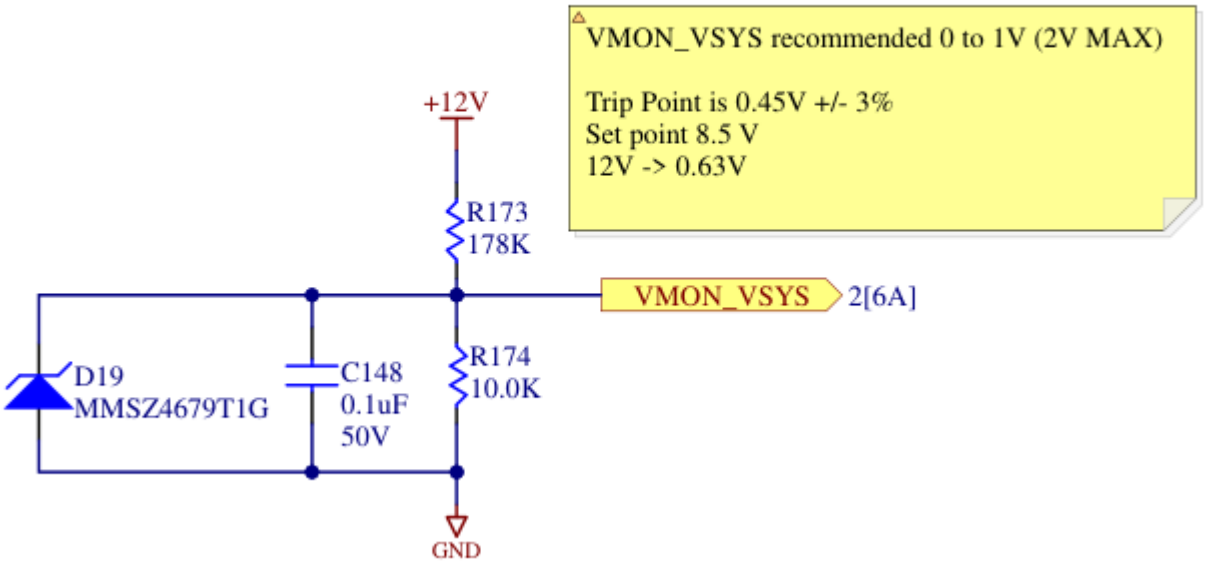

Figure 5 Sample VMON_VSYS input circuit with 12V monitoring

3.9 USB Interface

In addition to USB data lanes (USBn_DP and USBn_DM), carrier card designs intending to support USB operation on either USB0 or USB1 must utilize the signals listed below depending on intended operation. Users are encouraged to review the MitySOM-AM62 development kit as a reference design for Dual Role or Host only operation.

- **Dual Role**: The USB ID pin from the USB receptacle must be connected to an available GPIO pin. The USBn_DRVVBUS must be connected to the enable control of a +5V VBUS power supply for use in Host Mode. The USBn_VBUS must be connected to the USB VBUS voltage through a voltage divider network to limit the input voltage to approximately 1.7V. ***USBn_VBUS is not 5V tolerant***. Please refer to the AM62x datasheet for additional detail.

- **Host Only**: The USBn_DRVVBUS must be connected to the enable control of a +5V VBUS power supply for use in Host Mode. The USBn_VBUS must be connected to the USB VBUS voltage through a voltage divider network to limit the input voltage to approximately 1.7V. ***USBn_VBUS is not 5V tolerant***. Please refer to the AM62x datasheet for additional detail.

- **Device Only**: The USBn_DRVVBUS should be left unconnected. The USBn_VBUS must be connected to the USB VBUS voltage through a voltage divider network to limit the input voltage to approximately 1.7V. ***USBn_VBUS is not 5V tolerant***. Please refer to the AM62x datasheet for additional detail.

Users are cautioned that interfacing to a USB-C or USB-3 interface that includes Power Delivery capability will require additional consideration as the Power Delivery specifications can call for voltages on the VBUS line much higher than the nominal USB 2.0 +5.0V. The AM62x datasheet provides reference circuitry employing a combination of a resistor divider as well as a clamping Zener diode to ensure no damage to the AM62x device will occur.

4 Interface Descriptions

4.1 Module Reset

On the MitySOM-AM62 module, the main power input supply and all on-module generated power supplies are monitored and will trigger a module hard-reset if any of them fails or goes unstable. The main and MCU Power-on-Reset (POR) pin on the AM62x processor, MCU_PORx, is controlled by the TPS65219 PMIC and is not accessible on the SO-DIMM edge connector interface. The status of the power on reset is available on the PORz_OUT pin, accessible on the SO-DIMM edge connector interface. The PORz_OUT pin is pulled to ground on the SOM with a 15K ohm resistor.

There are two reset domains in the AM62x processor, the MCU (Cortex-M4F) reset domain and the MAIN (Cortex-A53) domain. The MCU_PORx pin, mentioned above, will cause both domains to be reset. For the MCU domain, the MitySOM-AM62 exposes the MCU_RESETz and the MCU_RESETSTATz on the SO-DIMM edge connector. These pins are direct connections to the AM62x processor. The MCU_RESETz should be pulled up or driven to VDDSHV_MCU on the carrier card and will act as a WARM RESET pin for the MCU domain, with MCU_RESETSTATz reflecting the MCU reset status. The MCU_RESETz pin, when asserted, will cause both the MCU domain and MAIN domain to be reset.

For the MAIN domain, the MitySOM-AM62 exposes the RESETz_REQ pin (direct connection) and the RESETSTATz (pulled to ground with 15K resistor) on the SO-DIMM edge connector. The RESETz_REQ pin should be pulled up or driven to the sequenced +3.3V IO voltage on the carrier card and will act as a WARM RESET pin for only the MAIN domain. The RESETSTATz tracks the reset status of the MAIN domain.

The reset architecture of the AM62x processor is somewhat complex due to the ability to support asynchronous operation between the MCU domain and the MAIN domain. Users are encouraged to become familiar with the design by referring to the AM62x Technical Reference Manual, section 6.3.

4.2 Emulator/JTAG

The I/O connector on the MitySOM-AM62 has a full set of JTAG/Debugger signals that can be used to connect to an emulator for code downloads and real time debugging.

4.3 McASP Port

The MitySOM-AM62 module can provide up to three Multi-Channel Audio Serial Ports, accessible by the ARM Cortex-A53 processor subsystem. The multichannel audio serial port (McASP) functions as a general-purpose audio serial port optimized for the needs of multichannel audio applications. The McASP is useful for time-division multiplexed (TDM) stream, Inter-Integrated Sound (I2S) protocols, and intercomponent digital audio interface transmission (DIT). The McASP consists of transmit and receive sections that may operate synchronized, or completely independently with separate master clocks, bit clocks, and frame syncs, and using different transmit modes with different bit-stream formats. The McASP module also includes serializers that can be individually enabled for either transmit or receive. For more information, please consult the AM62x device datasheets and Technical Reference Manual. Note that the McASP pins are shared with other peripherals.

4.4 Serial UARTs

The MitySOM-AM62 module can support up to 6 Universal Asynchronous Receive/Transmit (UART) ports that all support IrDA, CIR, and RTS/CTS flow control for the MAIN (Cortex-A53) domain. UART0 should be configured as a UART as that is the factory default console port used to support the boot loader application as well as the console for most higher-level operating systems. The other UARTs may be configured per application needs. For more information, please consult the AM62x device datasheets and Technical Reference Manual. Note that the UART pins are shared with other peripherals.

In addition, the MCU (Cortex-M4F) domain includes 1 UART port and the AM62x WKUP (Single Core R5, used as a device manager) also includes 1 UART port.

Note that the UART pins are shared with other peripherals.

4.5 SPI Ports

The MitySOM-AM62 module can support up to 2 Serial Peripheral Interface (SPI) ports on the MAIN (Cortex-A53) domain with each port having up to 2 chip selects directly controlled by the peripheral. Additional chip selects can be implemented with general GPIO pins if necessary. The module also supports access to both the available SPI ports on the MCU (Cortex-M4F) domain. Note that the SPI pins are shared with other peripherals.

4.6 I2C Ports

The MitySOM-AM62 module can support up to 3 Inter-Integrated Circuit (I2C) ports in the MAIN (Cortex-A53) domain: I2C1, I2C2, and I2C3. I2C0 is connected to an on-board prom (address 1010XXXb) that is used to hold factory configuration data (serial number, MAC address, etc.) in addition to the Power Management IC (TPS65219) which uses address 0110000b. I2C0 is not exposed to the SOM SO-DIMM edge connector interface. In addition, MCU Domain MCU_I2C0 is available and WKUP Domain WKUP_I2C0 are also available at the edge

connector. The I2C bus implementations are true open-drain style interfaces when configured correctly, and proper pull-up resistors must be included on the carrier card to the correct bank voltage pin as listed in the MitySOM-AM62 datasheet. Note that the I2C pins are shared with other peripherals.

4.7 USB

The MitySOM-AM62 provides two Universal Serial Bus (USB) interfaces that are mapped directly to the edge connector of the module. Both USB ports can operate in Dual Role mode and are USB 2.0 compliant. Dual role mode protocols support dynamic switching from host mode (e.g., for controlling USB mass storage devices such as thumb drives) to device mode (e.g., for interfacing to a PC) based on application software. For more information, please consult the AM62x device datasheets and Technical Reference Manual.

4.8 Display Controllers

The MitySOM-AM62 exposes a 24-bit pixel parallel output using either embedded sync or separate sync strobes conforming to the MIPI DPI 2.0 interface as well as two 4-data/1-clk Open LVDS Display Interface (OLDI) output channels. A maximum of two independent display buffers may be presented:

- One display on the 24-bit parallel interface
- One display on the OLDI output interfaces, which may be configured as
    - One 4 channel display interface driving 1 panel in Single Link mode (1 4-data/1-clk LVDS set)
    - One 8 channel display interface driving 1 panel with larger resolution / frame rate in Dual Link mode.
    - Two duplicated displays having the same resolution / timing requirements.

It is not possible to drive 2 independent displays on the 2x 4-channel OLDI output links. Note that the parallel display port interface pins are shared with other peripherals.

4.9 CAN Ports

The MitySOM-AM62 module exposes the 1x Modular Controller Area Network (MCAN) port, supporting CAN and CAN FD, on the MAIN (Cortex-A53) domain connected to the AM62x. The module also exposes the 2x MCAN controllers available on the MCU (Cortex-M4F) domain. CAN ports support bit rates up to 1 Mbps, conform to CAN protocol 2.0 A, B, and ISO 11898-1:2015, and have DMA and interrupt support. For more information, please consult the AM62x device datasheets and Technical Reference Manual. Note that the CAN pins are shared with other peripherals.

4.10 Timers

The MitySOM-AM62 module exposes 12 Timer IO pins, 4 in the MCU domain and 8 in the MAIN domain, that can be individually configured as trigger inputs or PWM outputs. Each timer has a 32-bit register associated with it and supports 3 modes of operation: Timer mode, Capture mode, or Compare mode. Odd number timers can be cascaded to the immediately even number timer (e.g., Timer 1 cascaded to Timer 0) to support up to 64-bit

timing operations. For more information, please consult the AM62x device datasheets and Technical Reference Manual. Note that the Timer pins are shared with other peripherals.

4.11 MultiMediaCard Interfaces

The MitySOM-AM62 module supports interfacing with up to 3 Multi-Media Card (MMC) interfaces that also support Secure Digital (SD) and Secure Digital Input/Output (SDIO) formats: MMC0, MMC1, and MMC2. The MMC ports conform to the MMC5.1, SD4.1, and SDIO 4.0 specifications.

MMC0 is a full 8-bit interface and is (optionally, based on model number) integrated to an onboard eMMC device that may be used as the SOM boot media. The MMC0 interface is not exposed to the SO-DIMM edge connector interface. MMC1 and MMC2 are 4-bit data interfaces and are exposed on the MitySOM-AM62 SO-DIMM edge connector. In general, MMC1 is typically used to interface to a MicroSD card as a boot device and/or external storage. MMC2 may be used for storage, though it is often used to integrate with wireless modules that interface with SDIO host controllers.

For more information, please consult the AM62x device datasheets and Technical Reference Manual. Note that the MMC pins are shared with other peripherals.

4.12 Enhanced Capture

The MitySOM-AM62 module contains three 32-bit Enhanced Capture (eCAP) modules that can be used to perform period and duty cycle measurements of external events. Each eCAP interface can also be configured as a PWM output. For more information, please consult the AM62x device datasheets and Technical Reference Manual. Note that the eCAP pins are shared with other peripherals.

4.13 Enhanced High Resolution PWM

The MitySOM-AM62 module provides three 32-bit Enhanced High-Resolution PWM (eHRPWM) modules that support extending time resolution capability and finer time granularity control or edge positioning. Each interface can be configured as two single ended, two dual-edge symmetric, or two dual-edge asymmetric outputs. For more information, please consult the AM62x device datasheets and Technical Reference Manual. Note that the eHRPWM pins are shared with other peripherals.

4.14 Enhanced Quadrature Encoder Pulse

The MitySOM-AM62 module contains up to three Enhanced Quadrature Encoder Pulse (eQEP) modules that can interface directly to encoder disks like those used on shaft encoders. For more information, please consult the AM62x device datasheets and Technical Reference Manual. Note that the eQEP pins are shared with other peripherals.

4.15 General Purpose Memory Controller

The MitySOM-AM62 module contains a General Purpose Memory Controller (GPMC) that can be used for interfacing to external memory devices including SRAM-like memories, ASIC devices, and NAND Flash. The GPMC supports up to 133 MHz external memory clock performance. For more information, please consult the AM62x device datasheets and Technical Reference Manual. Note that the GPMC pins are shared with other peripherals.

4.16 10/100/1000 Ethernet

The MitySOM-AM62 module contains a 3-port switch (CPSW3G) Gigabit Ethernet Switch subsystem which supports reduced gigabit media independent interfaces (RGMII), and reduced media independent interfaces (RMII), conforming to IEEE 802.3 serial management specifications. For more information, please consult the AM62x device datasheets and Technical Reference Manual. Note that the Ethernet pins are shared with other peripherals.

4.17 GPIO

Most of the pins connected to the AM62x processor can be configured as General Purpose Input/Output (GPIO) pins. The Pin Function Table in the MitySOM-AM62 datasheet identifies which GPIO pins, Power Domain, and register settings correspond to each exposed GPIO capable pin.

5 Mechanical Requirements

The following sections describe some of the mechanical requirements of incorporating a MitySOM-AM62 module into a board design.

5.1 Module Connector

The module has a single connector that contains all of the power and I/O for the module. The mating socket is a standard 260 position SODIMM connector that is commonly used for DDR4 memory modules. Example connectors are the TE Connectivity AMP Connectors 2309409-2 (5.2mm height) and Amphenol Communications Solutions 10141730-004RLF (also 5.2mm height) connectors. Taller options of the right-angle connectors, e.g., the 8mm or 9.2mm height option, are also suitable. There are many variants of this connector that allow the module to be positioned vertically, horizontally, or even stacked. Most of the connectors of this style are rated for approximately 25 insertions.

5.2 Module Clearance – Horizontal Mount

The MitySOM-AM62 module uses a SO-DIMM style main interface connector for electrical and mechanical attachment to the carrier board. This style of connector positions the MitySOM-AM62 module in parallel with the carrier board, and as such there is limited clearance between the module and the carrier board. Therefore, it is not possible to place high-profile carrier board components underneath the MitySOM-AM62 module.

However, it is possible to utilize most of this space for low-profile components. Please refer to the following diagrams and tables for module-specific clearances. Note that this configuration is based on TE Connectivity AMP Connectors 2309409-2 (5.2mm height) connector. Dimensions may have to be adjusted if other connectors are used. As shown a keep-out height of 2.50mm from the top of the module is recommended. On the bottom of the module, two regions are defined, one a 1.2mm with 28mm of the edge connector interface, and a second that is 2.00mm near the floating edge of the connector as there is one part, the EEPROM, on the bottom side that is nominally 1.75mm in that area. The STEP model of the SOM is available from the Critical Link support site, and users are encouraged to verify clearance if making use of the space under the module.

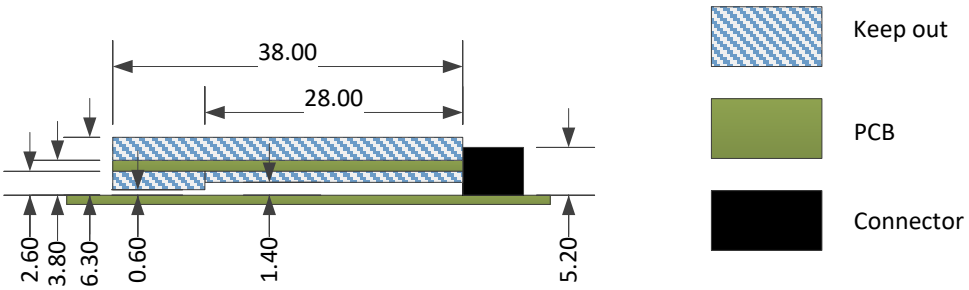

Figure 6: MitySOM-AM62 Module Clearance - Side View, all dimensions in mm

5.3 Mounting Methods

The modules feature an additional optional mechanical attachment method. A hard mechanical attachment by board-to-board standoff and screw hardware may be used to mount the module. The (approximate) center of the free-floating edge of the SOM features a 2.6mm diameter mounting hole that is compatible with M2 size mounting hardware. For details and dimensions of corresponding mounting hole placement on your carrier board please reference Section 6.5 of this document. The mechanical drawing in Figure 7 illustrates the mechanical requirements of this optional attachment method. Note that this configuration is based on the TE Connectivity AMP Connectors 2309409-2 (5.2mm height) connector. Dimensions may have to be adjusted if other connectors are used.

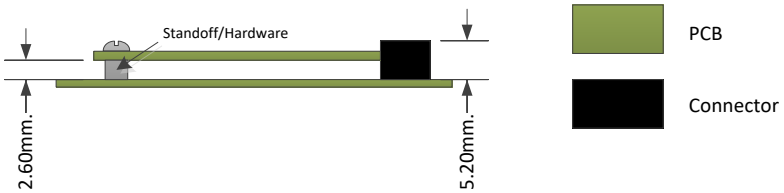

Figure 7: Hard Mounting the MitySOM-AM62

Table 3 shows the hardware and part numbers utilized by the MitySOM-AM62 Development kit. The Development Kit carrier card utilizes a 2mm PEM surface mount standoff. The arrangement requires an additional washer/spacer of approximately 0.5-6mm (0.02”) below the SOM to maintain a roughly 2.6mm board to board spacing.

Table 3: Optional Mounting hardware used in Development Kit

Item	Description	Manufacturer	Part Number
1	Surface Mount Standoff, M2, 2mm	PEM	SMTSO-M2-2ET
2	Polycarbonate Plastic Washer, M2	McMaster Carr	90940A411
3	Zinc-plated M2 Pan head Screw, 4mm	McMaster Carr	94387A512

Shock & Vibration

For customers who are interested in using MitySOM-AM62 modules in rugged environments, the optional mechanical attachment methods discussed in section 5.3 enable MitySOM-AM62 modules to tolerate much greater mechanical shock and vibration forces than without any additional mounting support.

5.4 Thermal Management

The MitySOM-AM62 has no specific requirements regarding thermal management. The modules can be operated without heat sinks or air flow, and inside tight enclosures. However, if a module is intended to be used in hot industrial environments, it is advisable to test the device in the enclosure and environment that the module will be used in. In these cases, it may be necessary to either add thermal management to the enclosure or lower the operating temperature specification of the end product. Results from thermal testing and measured power consumption of the SOM in a fixed configuration are provided on the Critical Link support site.

6 Board Layout Recommendations

The following sections discuss topics for successful board layouts incorporating the MitySOM-AM62 module.

6.1 Placement

Placement of the module site is crucial to a successful carrier board layout. Because the module connector footprint is fine-pitch and dual-row, it is generally best to place the connector fairly centered in the overall board layout. This placement allows traces to be routed out from both sides of the connector, using mainly top-side copper tracks. The use of fewer signal layers, and therefore fewer vias, generally results in a more compact design with better signal integrity than a board using many layers and vias. Of course, ideally central placement is not always possible because of other mechanical constraints.

Mechanically, enough space must be allocated for the full extension of the module. Although it is possible for a module to hang over the edge of its carrier board, this may not be desirable if additional mechanical attachment methods are desired for ruggedness, as discussed in section 5.3. Another thing to keep in mind with placement on the carrier board and in enclosures is the cam-in action of the MitySOM modules into their respective sockets. The modules are generally installed at an angle of about 25° to 30° before swinging down to locked position. Enclosure designs should accommodate this motion.

6.2 Pin-out and Routing

Care must be taken when routing the MitySOM-AM62 high speed interfaces – specifically the USB 2.0 OTG ports, the OLDI/LVDS ports, the MIPI data and clock ports, and the gigabit Ethernet ports. Please refer to the specific device specification for guidance related to these pins.

6.3 Access issues

Given that it is possible and often desirable to make best use of available space by placing components underneath the MitySOM-AM62 module (refer to section 5.2), hardware and software engineers who will be debugging code on the platform could find themselves in a tough situation if the component they need to access is blocked by the installed MitySOM-AM62 module. Because of these situations it is advisable to either not use the space under the MitySOM-AM62 module for active components that might need live probing with the MitySOM-AM62 in-circuit, or only place circuits there that are already tried and tested by engineers on other platforms. If an obscured circuit does need to be probed, it may be necessary to solder temporary wires onto probe points. An even better solution would be to design the board with bottom-side test points, at least in the MitySOM-AM62 region, if this is possible on a given design.

6.4 PCB/PCA Technology

The MitySOM-AM62 module does not have any specific requirements about the PCB technology used for its carrier board. The required socket connectors are available as RoHS compliant and may be used in both leaded and lead-free assembly processes. The only recommendation is to fabricate the carrier board thick enough to rigidly support the MitySOM-AM62 socket connector. In practice, FR-4 with a common finished thickness of 0.062 inches is enough for all types of MitySOM-AM62 modules.

6.5 PCB Footprints

Figure 8, Figure 9, and Figure 10 show the recommended PCB footprint and keep out area for the TE Connectivity 2309409 series connector is shown below. The figures are copied directly from the part drawing and should include all measurements to ensure that a proper footprint for the SO-DIMM module connector is created. Similar figures can be found for other connector manufacturers as the design should be compliant with JEDEC SO-DIMM DDR4 specifications. We recommend that the additional mounting hole be added to this footprint, so they are placed properly on your carrier board. Figure 11 shows the necessary dimensions to properly place the mounting holes for the module. Note the position of the mounting hole is referenced to the mounting pin near pin 260 of the connector (datum Y).

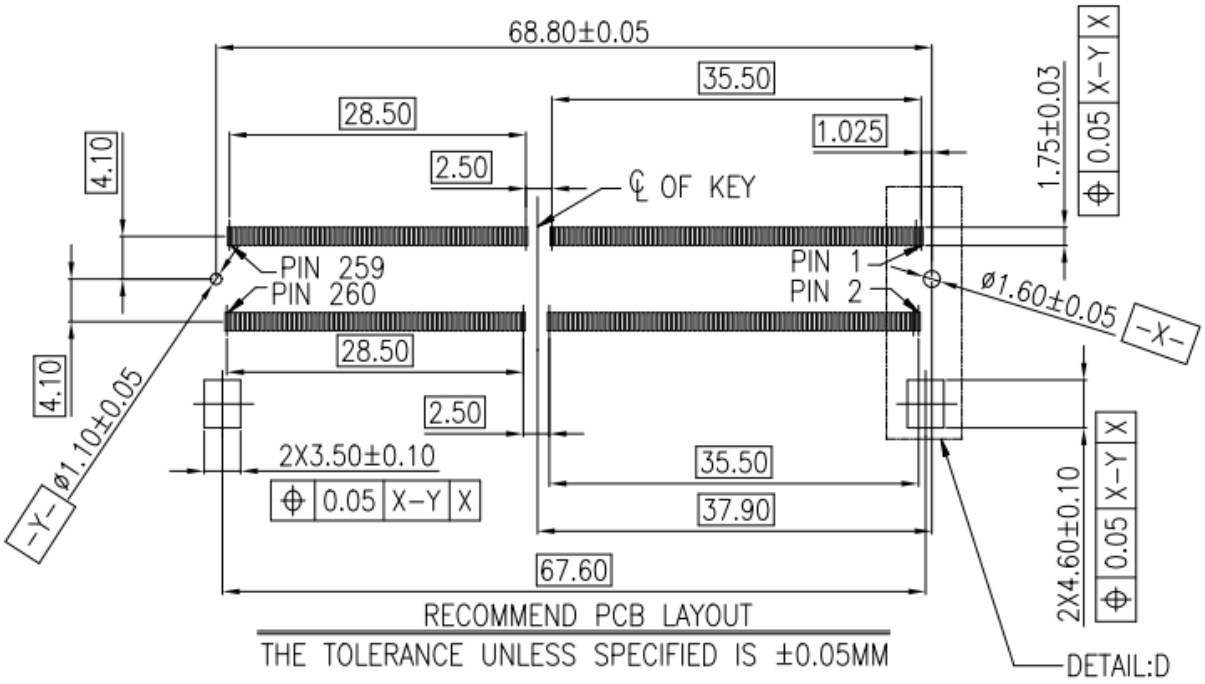

Figure 8: 2309409 Recommended PCB Footprint (as shown on manufacturer datasheet)

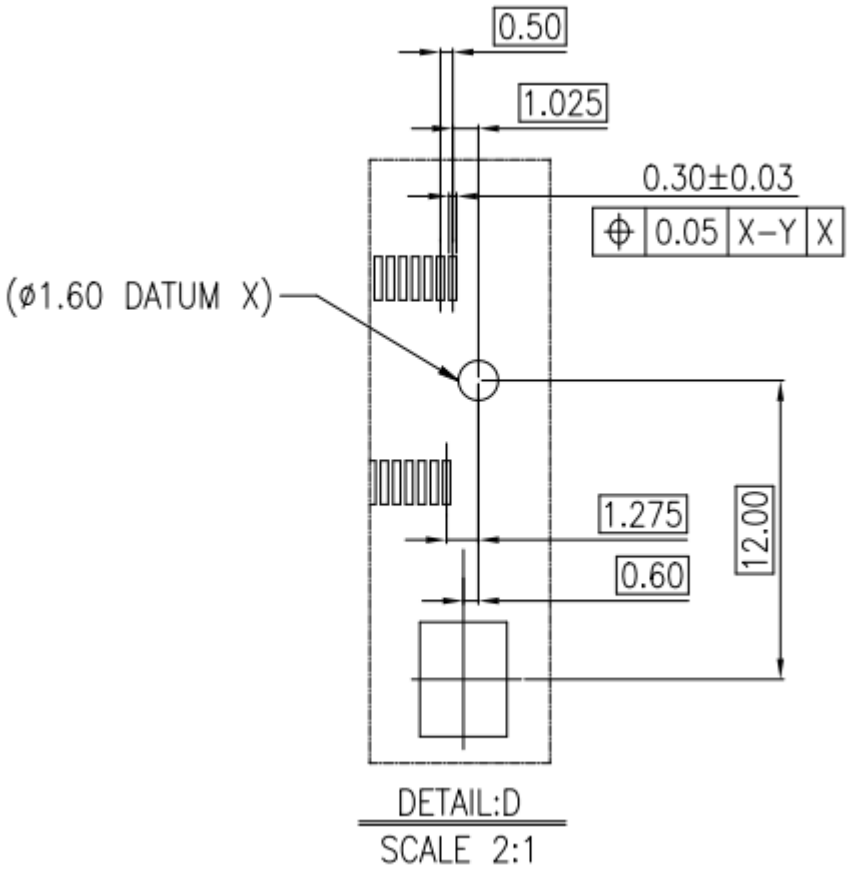

Figure 9 Detail D, recommended pad dimensions for 2309409 (as shown on manufacturer datasheet)

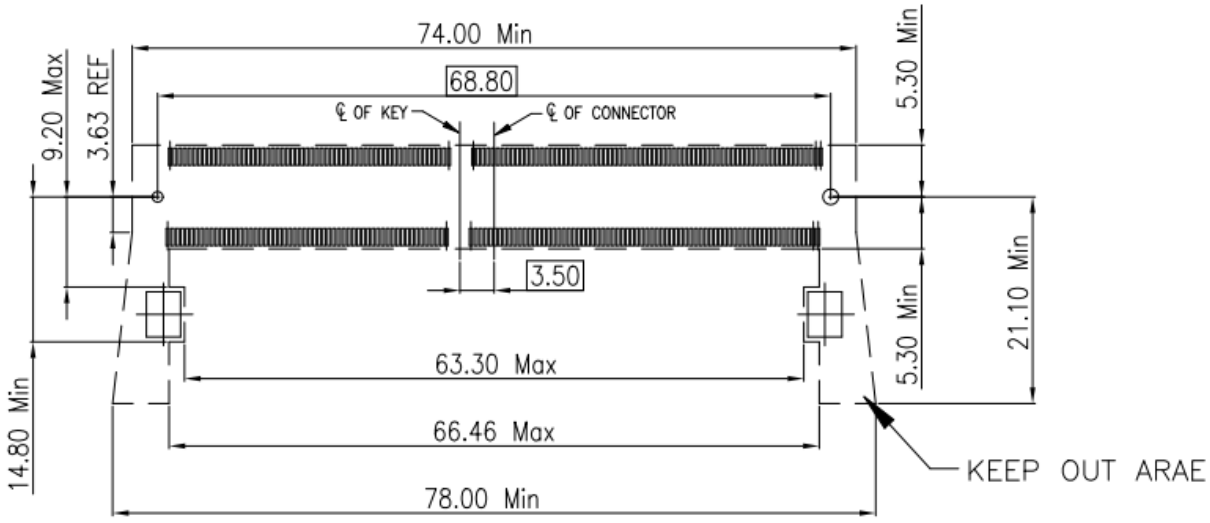

Figure 10 Recommended PCB keep out area for 2309409 (as shown on manufacturer datasheet)

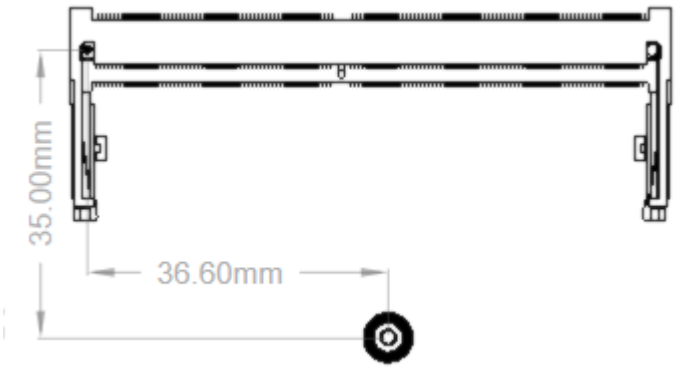

Figure 11: MitySOM-AM62 Mounting Hole Location

Note: These dimensions are in reference to the left side mounting pin (when viewed from above, as shown) of the TE Connectivity 2309409-2 SO-DIMM DDR4 connector.

7 Revision History

Revision	Date	Description of Changes
1.0	27-November-2023	Initial Revision