

FEATURES

MitySOM-AM57(F) Development Board

Supported Critical Link Modules

- MitySOM-AM57
- MitySOM-AM57F

Key Hardware

- TI AM57xx Processor
- Xilinx Artix-7 FPGA (AM57F Only)

Additional Hardware Included:

- Micro USB & Ethernet Cables
- AC to DC 12V 3.34A Adapter

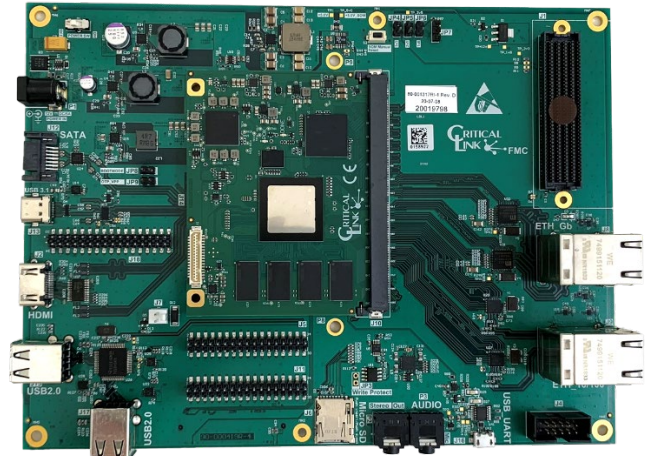
Integrated +1.8V/+2.5V/+3.3V/+5V Power Supplies

Digital Interfaces:

- HDMI (1920x1080p, 60 fps)
- Audio Output and Line Input
- 2 x Gigabit Ethernet
- 2 x 10/100 MBit Ethernet (PRU)
- Board Information EEPROM
- Debug UART to USB Console
- 1 x USB 3.0 DRD Interface (USB-C)
- 4 x USB 2.0 Host (Type-A)
- 1 x SATA 3-Gbps
- Micro SD-Card Socket
- SOM I2C Power and Voltage Monitors

Expansion

- FMC Expansion Header (400-Pin)
- I2C and Artix-7 FPGA IO
- 3 x 34 Pin 0.1" AM57x GPIO Headers
- External I2C Header
- 1.8V and 3.3V levels



Software and Documentation:

- Linux Kernel (Based on TI Processor SDK)
- U-Boot (Based on TI Processor SDK)
- Yocto Filesystem (Based on TI Processor SDK)
- Linux and DSP Cross Development SDK
- Development Board Schematics
- Development Board Gerber Files
- Development Board BOM

APPLICATIONS

- MitySOM-AM57(F) Evaluation
- Process Automation
- Factory Automation
- Industrial Automation
- Embedded Instrumentation
- Rich Displays
- Rapid Prototyping



DESCRIPTION

The MitySOM-AM57(F) Development Kit provides all the hardware and software support for system designers and developers to evaluate the Critical Link MitySOM-AM57(F) System on Module (SOM). The MitySOM-AM57(F) Development Kit comes complete with the MitySOM-AM57(F) module that meets your project's needs.

The MitySOM-AM57(F) Development Kit includes on-board dual 10/100/1000 MBit Ethernet, quad USB-2.0 Host ports, and one USB-C USB 3.0 Dual Role Device (DRD) port. A 400-pin FMC expansion port provides access to IO interfaces on the AM57x modules with an Artix-7 FPGA or additional Multi-Functional IO on AM57 modules. The additional triple 34-pin 0.1-inch headers provide access to GPIO and spare IO from AM57xx processor.

The High-Definition Multimedia Interface (HDMI) supports displays a resolution of up to 1920x1080 at 60Hz through a standard HDMI connector, video only. Multi-Media Card (MMC) interface supporting Micro Secure Digital (Micro SD) cards and an I/O Expansion connector for a WiLink 802.11b/g/n Wireless with Bluetooth module from Texas Instruments or a user-designed custom add-on card. All of these interfaces are powered from a single 12VDC input with onboard +1.8V/+2.5V/+3V/+5V power supplies.

A block diagram of the MitySOM-AM57(F) Development Kit is illustrated in Figure 1. Control of the on-board interface hardware and connected Expansion IO cards require proper configuration of the MitySOM-AM57(F) Module. While not required, it is strongly recommended that the MitySOM software development kit and supplied API be used to manage these interfaces.



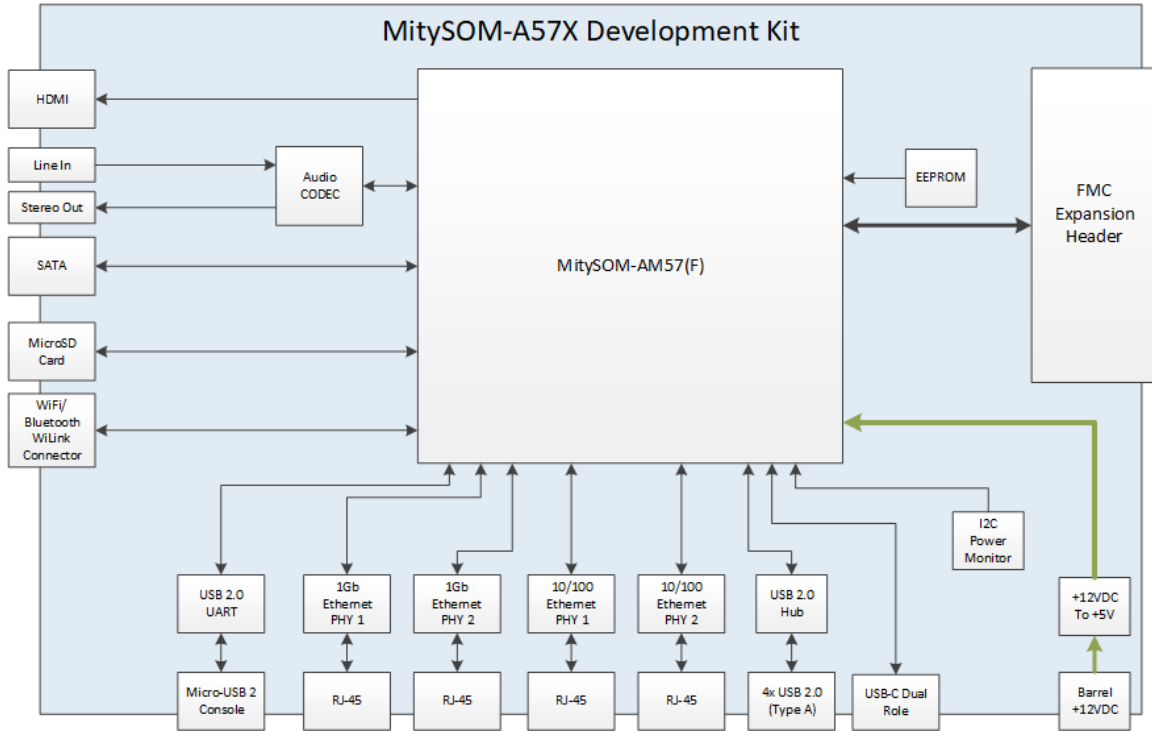


Figure 1: MitySOM-AM57(F) Development Kit Block Diagram

Additional details about the AM57xx, available peripherals, and their features are provided in the datasheet at the TI website (www.ti.com/AM57x).

Additional details about the Artix-7 FPGA are provided in the datasheet at the Xilinx website (<https://www.xilinx.com/products/silicon-devices/fpga/artix-7.html>).

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Feature Descriptions

Debug UART to USB Interface Description

The on-board UART to USB Bridge, FTDI FT230XS-U, provides a serial interface at 115,200 baud 8N1. The USB serial interface, J16 – USB UART, is routed to the primary MitySOM-AM57(F) serial console port, UART3. It allows for general module debugging and console interaction.

When connected to a Windows PC, no drivers are required as Windows Update is used to obtain the drivers.

Audio Input/Output Description

Standard 3.5mm / 1/8th inch audio jacks are provided for both stereo audio output, P2, and line-in audio input, P3, from/to a TLV320AIC3104 32-bit audio CODEC connected to MCASP8 on the AM57xx processor on the MitySOM-AM57(F) module.

Linux Driver and API examples are available to support the audio functionality.

USB 3.0 Interface Description

The USB 3.0 interface using a USB type C connector, J13 – USB 3.0, is configured as a dual role interface. It is connected to the USB1 port of the AM57xx processor of the MitySOM-AM57(F) module and is capable of supporting a maximum data bit rate of 5 Gbps and is also backward compatible with USB 2.0 devices. Linux drivers are available.

4-Port USB 2.0 Interface Description

A 4-port USB 2.0 Hub is connected to the USB2 interface of the AM57xx processor of the MitySOM-AM57(F) module. The interface is through two, J15 and J17, dual USB Type-A connectors configured in host mode. Linux drivers are available.

MultiMedia Card (Micro SD) Interface Description

The onboard Micro MultiMedia Card (MMC) slot uses a Micro Secure Digital (uSD) connector J6 which supports SD Standard v3.01. It is compatible with standard (SD), SDHC (up to 32GB), and SDXC (Up to 2TB) cards. By default, the MitySOM-AM57(F) Development Kit boots from this interface.

U-Boot configuration information and Linux drivers are available.

Dual Gigabit Ethernet Interface Description

Dual Micrel KSZ9031 network PHYs on the Development Board are each capable of running at 10/100/1000Mbit including link auto-negotiation and RGMII/MDIO capability. A dual industry-standard RJ-45 connector, J8 – ETH_Gb, is provided for external connections. These Ethernet interfaces are connected to the AM57xx processor and may be used to perform remote code download via U-Boot and FLASH upgrades on an attached MitySOM-AM57(F) module.

Dual 10/100 Mbit PRU Ethernet Interface Description

The on-board 10/100 Mbit Ethernet interfaces feature Texas Instruments DP83822 network PHYs each capable of running at 10/100 Mbit including link auto-negotiation and MII/MDIO capability. A dual industry-standard RJ-45 connector, J9 – ETH_10/100, is provided for external connection. These Ethernet interfaces are connected to the AM57xx processor's PRU2 on the MitySOM-AM57(F) module.

HDMI (Video Only) Interface Description

A standard HDMI interface for external monitor connection, video only, with a maximum resolution of 1920x1080 is provided. Note that the Texas Instruments AM57x6 devices do not support HDMI.

SATA Interface Description

A standard 7-pin SATA interface, J12 – SATA, is provided for external hard drive connections supporting the SATA standard v2.6. It supports up to SATA Gen 2, 3-Gbps, speeds, and is backward compatible with SATA Gen 1, 1.5-Gbps, devices.

Note that SATA Gen 3, 6-Gbps, devices can be utilized if they can support the slower SATA Gen 2 interface speed.

FMC Expansion Port Interface Description

The FPGA Mezzanine Card (FMC) interface, J1, allows for the use of add-on cards that are designed for the Xilinx Artix-7 on the MitySOM-AM57(F) module. The FMC interface is compatible with Low Pin Count (LPC) FMC expansion cards and provides a subset of High Pin Count (HPC) signals.

It features 2 FPGA Transceiver lanes and 48 FPGA IO pairs (96 IO pins total). FPGA IO signal voltages for the MitySOM-AM57(F) module can be set to either +1.8V, +2.5V, or +3.3V based on the installation of JP4, JP5, or JP6 on the Development Board.

Several “off the shelf” boards/kits are available from third parties that are compatible with this interface.

The MitySOM-AM57 non-FPGA modules routes additional multi-functional IO to the FMC connector from the AM57xx processor in place of the FPGA IO pairs.

3x 34-Pin Expansion Port Interface Descriptions

Accessible on three 0.1-inch dual-row 34-pin headers, J5, J11, and J18, are 67 AM57xx direct IO signals at 1.8V logic levels, 4 Artix-7 FPGA signals, and +1.8V/GND connections. Multi-functional IO replaces the FPGA signals on the MitySOM-AM57(F) modules.

WiFi/Bluetooth Expansion Interface Description

The WiFi/Bluetooth expansion interface, J3, is designed to be directly compatible with the Texas Instruments WL1837MODCOM8I WiFi and Bluetooth expansion card. Linux drivers are available for the TI WL1837 expansion card.

This interface can also be used for a user-designed interface card and features a 4-bit SDIO interface, 2 UART interfaces, a PCM audio interface, and multiple GPIOs.

I2C5 Interface Description

Exposed at the 10-pin connector J4 is the I2C5 interface from the AM57xx processor. Both +1.8V and +3.3V logic level connections for this interface are available on the connector as well as 1.8V and 3.3V power supply and ground connections.

Additionally, the I2C5 interface is connected to the following devices on the Development Kit; USB-C controller, Audio Codec, EEPROM, MitySOM-AM57(F) +5V current/power monitor, and Development Kit voltage monitor.

Baseboard User EEPROM

A 256 Kbit EEPROM, U11, is available for user configuration information on the MitySOM-AM57(F) Development Board. This EEPROM is accessible over the I2C5 interface to the AM57xx processor.

Baseboard Power Supply Monitor

A 4 channel ADC, U10, is installed on the Development Board to enable the monitoring of the +5V, +3.3V, +2.5V, and +1.8V power supplies. This ADC is accessible over the I2C5 interface to the AM57xx processor.



MitySOM-AM57(F) Current/Power Monitor

A power/current monitor, U8, is installed in line with the +5V power to the MitySOM-AM57(F) module. Additionally, this device has a single channel ADC that can monitor the +12V power supply voltage on the Development Board. It is accessible over the I2C5 interface to the AM57xx processor.



Module Configuration Jumpers

Boot Configuration Jumper Description

The MitySOM-AM57(F) Development Board features a 2-pin jumper, JP8, which determines the search order of peripherals from the AM57xx processor for a valid boot image.

By default, the MitySOM-AM57(F) Development Kit boots initially from the SD card.

FPGA IO Voltage Select Jumper

A set of 3 jumpers is provided on the MitySOM-AM57(F) Development Board to select the voltage level of the user-configurable FPGA IO; bank 34 and bank 15. The IO voltages available are +3.3V, +2.5V, and +1.8V. This only applies to the MitySOM-AM57F variants. The IO voltage for the non-FPGA module is +1.8V.

PMIC Power Hold Jumper

The PMIC_POWERHOLD signal from the MitySOM-AM57(F) is exposed on a 3-pin jumper on the MitySOM-AM57(F) Development Board. It controls the module's power state, on/off, from the Development Board.

This signal is designed to be left floating for the default mode of operation. A jumper can be installed for this signal to be pulled up to 1.8V or pulled to GND.

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Maximum Supply Voltage 13.2 V
Storage Temperature Range 0 to 80C

OPERATING CONDITIONS

Ambient Temperature 0 to 70C
Range
Humidity 0 to 95%
Non-condensing

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Typical	Limit	Units (Limits)
I _{Max}	12V Supply (included AC adapter)	Note 1		3.3	A
Maximum Power Supply Output					
I _{Max}	12.0V Supply ² for external components	Note 2		1.0	A
I _{Max}	5.0 V Supply ² for external components	Note 2		3.0	A
I _{Max}	3.3V Supply ² for external components	Note 2		2.5	A
I _{Max}	2.5V Supply ² for external components	Note 2		2.5	A
I _{Max}	1.8V Supply ² for external components	Note 2		1.5	A
Typical Power Usage³					
V _S	Supply Voltage	Note 3	12.0		V
I _S	Supply Current	Note 3	2.3		A

Notes:

1. An alternative higher amperage AC/DC 12V adapter is available upon request. Contact Critical Link for details and ordering information.
2. The maximum current supplied to external components should be limited to the specified maximum for the 12.0V, 3.3V, 2.5V, and 1.8V supplies. Please note that for simultaneous power supply usage a larger 12V external power supply may be needed.
3. No external components attached, 100% ARM utilization, FPGA example loaded, 3.3V selected for FPGA IO, and Ethernet are enabled and active.

ELECTRICAL INTERFACE DESCRIPTIONS

MitySOM-AM57(F) Module Interface Connectors – J10 and J14

Each MitySOM-AM57(F) Development Kit includes a MitySOM-AM57 or MitySOM-AM57F module. The Development Board interfaces with the module through a 314-pin MXM connector, J10, and 100-pin Hirose connector, J14. Please see the MitySOM-AM57(F) Datasheet for complete pinouts of these connectors.

Input Power – P1

The MitySOM-AM57(F) Development Kit power interface, P1, requires a single +12Volt power supply. This input supplies power to the main +5V, +3.3V +2.5V, and +1.8V power supplies on the development board.

Table 1: Input Power Interface Pin Description

Signal	P1 Position
+12V	Center Pin
GND	Outer Ring

Main Power Switch – S1

An input power switch is present on the Development Board, S1, which controls the power input, on or off, from P1.

Debug UART to USB – J16

Table 2: J16 Micro USB Connector Pin Assignments

J16 Pin	J16 Signal	Type	Standard	Notes
1	VBUS	Power	-	
2	D-	I/O	USB 2.0	USB data minus line
3	D+	I/O	USB 2.0	USB data plus line
4	No Connect	-	-	
5	SHIELD	GND	-	

The FTDI FT230XS-U UART to USB controller on the Development Board is connected to the UART 3 interface of the AM57xx processor, as shown below:

Table 3: USB Controller to UART Interface

FTD230XS Signal	SOM Interface Signal	SOM Pin
TXD	DEBUG UART3 RX	J10 – 279
RXD	DEBUG UART3 TX	J10 - 281
RTS#	No Connect – 1.0k to GND resistor	No Connect
CTS#	No Connect – 1.0k to GND resistor	No Connect

I2C5 Devices and Interfaces

The I2C5 interface from the MitySOM-AM57(F) AM57xx processor is used on the Development Board for onboard devices as well as available externally at both the FMC connector, J1, and the I2C5 header J4.

Table 4: I2C5 SOM Pin Connections

Module Pin	Signal Name	Note
J10 - 185	I2C5 SCL	4.7k ohm pull-up on development board
J10 - 207	I2C5 SDA	4.7k ohm pull-up on development board

The list below contains the corresponding devices on the I2C5 bus, device description, and addresses that are used on the Development Board:

Table 5: I2C5 Device and Address Information

Device	Device Description	Address
TLV320AIC3104IRHBR	Audio Input/Output Codec – U29	0x18
AD7995YRJZ-150RL7	Development Board +5V, +3.3V, +2.5V and +1.8V voltage monitor – U10	0x29
HD3SS3220RNHR	USB 3.0 Type-C Controller – U12	0x47
CAT24C256WI-GT3	Baseboard 256Kbit EEPROM – U11	0x50
LTC2945IMS#PBF	MitySOM-AM57(F) +5V current/power monitor – U8	0x6E
FMC Connector	FMC Connector – J1	N/A
I2C5 Connector	I2C5 Connector – J4	N/A

Audio Input/Output – P2 & P3

The MitySOM-AM57(F) Development Board provides both audio input, line-in stereo L/R, and audio output, L/R stereo speaker, connections through audio codec TLV320AIC3104, U29. The codec is connected to the I2C5 bus please reference Table 5 for I2C5 address information.

Two 3.5mm/1/8” jacks, P2 for output and P3 for input, utilize the pinouts shown below:

Table 6: P2 Audio Output Pin Assignments

P2 Pin	P2 Signal	Type	TLV320AIC U29 Pin	Notes
1 - Sleeve	GND	Power	N/A	Audio Ground
2 - Tip	Audio Out Left	O	27	Unbalanced audio output
3 - Ring	Audio Out Right	O	29	Unbalanced audio output
4 – Tip Switch	No Connect	NC	N/A	

Table 7: P3 Audio Input Pin Assignments

P3 Pin	P3 Signal	Type	TLV320AIC U29 Pin	Notes
1 - Sleeve	GND	Power	N/A	Audio Ground
2 - Tip	Line In Left Input	I	14	Line In – no amplification, MIC not supported
3 - Ring	Line In Right Input	I	16	Line In – no amplification, MIC not supported
4 – Tip Switch	No Connect	NC	N/A	

USB 3.0 Type-C – J13

The MitySOM-AM57(F) Development Board features a USB Type-C connector to the USB 3.0 interface of the AM57xx processor, which is also backward compatible with USB 2.0 devices. A HD3SS3220 MUX, U12, allows for connection of the USB Type-C cable in either orientation and detection of the host/peripheral mode required by the connected cable using the USB-C CC pins. The MUX is connected to the I2C5 bus please reference Table 5 for I2C5 address information.

The USB Type-C interface cannot provide power to the MitySOM-AM57(F) Development Board. However, the development board can provide up to 2.8Amps at +5V on the VBUS connections of the USB-C.

The following table lists the interface pin-out for the USB Type-C connector, J13.

Table 8: J13 USB Type-C Pin Out

J13 Pin	J13 Signal	U12 MUX or SOM Pin	J13 Pin	J13 Signal	U12 MUX or SOM Pin
A1	GND	N/A	B12	GND	N/A
A2	TX1 P	U12 – Pin 16	B11	RX1 P	U12 – Pin 14
A3	TX1 N	U12 – Pin 17	B10	RX1 N	U12 – Pin 15
A4	VBUS	U12 – Pin 5	B9	VBUS	U12 – Pin 5
A5	CC1	U12 – Pin 2	B8	No Connect	N/A
A6	USB1 DATA P	J14 – 46	B7	USB1 DATA N	J14 – 44
A7	USB1 DATA N	J14 – 44	B6	USB1 DATA P	J14 – 46
A8	No Connect	N/A	B5	CC2	U12 – Pin 1
A9	VBUS	U12 – Pin 5	B4	VBUS	U12 – Pin 5
A10	RX2 N	U12 – Pin 18	B3	TX2 N	U12 – Pin 20
A11	RX2 P	U12 – Pin 19	B2	TX2 P	U12 – Pin 21
A12	GND	N/A	B1	GND	N/A

4 Port USB 2.0 Type-A – J15 & J17

The MitySOM-AM57(F) Development Board features a 4-port USB hub, TUSB4041IPAPR – U26, which is connected to the USB2 interface from the AM57xx processor. The 4 USB ports are exposed from the Development Board as two dual USB Type-A Host-only connectors, J15 and J17.

This interface is a USB 2.0 interface and supports up to 480Mbps throughput speeds and is backward compatible with Full-speed and Low-speed devices.

Each port is capable of supplying a maximum of 1A of current at +5V and an overcurrent detection circuit is connected to each port individually.

The pinout for both J15 and J17 is included in the following table.

J15 Pin	J15 Signal	J15 Upper or Lower Port	J17 Pin	J17 Signal	J17 Upper or Lower Port
1	VBUS1	Lower	1	VBUS3	Lower
2	USB1 DM		2	USB3 DM	
3	USB1 DP		3	USB3 DP	
4	GND		4	GND	
5	VBUS2	Upper	5	VBUS4	Upper
6	USB2 DM		6	USB4 DM	
7	USB2 DP		7	USB4 DP	
8	GND		8	GND	

MultiMedia Card (Micro SD) – J6

The MitySOM-AM57(F) Development Board provides a MMC v3.01 interface that uses a standard Micro Secure Digital (Micro SD) card slot for the physical interface. This is connected to the MMC1 interface of the AM57xx processor as follows:

Table 9: J6 Micro SD Card Connector

J6 Pin	J6 Signal	SOM Interface Signal	SOM Pin
1	DAT2	MMC1 DAT2	J10 – 171
2	CD/DAT3	MMC1 DAT3	J10 – 169
3	CMD	MMC1 CMD	J10 – 167
4	VDD	+3.3V	N/A
5	CLK	MMC1 CLK	J10 – 165
6	VSS	GND	N/A
7	DAT0	MMC1 DAT0	J10 – 175
8	DAT1	MMC1 DAT1	J10 – 173
9	Switch (B)	MMC1 SD CD	J10 - 163
10	Switch(A)	GND	N/A

The write-protect feature for the Micro SD card can be enabled/disabled, when configured in the host OS, through the use of the jumper JP3 on the MitySOM-AM57(F) Development Board as follows:

Table 10: Micro SD Card Write Protect

Jumper - JP3	Write Protect Status
Installed	Enabled
Removed	Disabled

Dual Gigabit Ethernet – J9A & J9B

The MitySOM-AM57(F) Development Board provides two RJ-45 connections, with link and activity LEDs, for dual Gigabit 10/100/1000 Ethernet from the AM57xx processor. These external connections follow the standard TIA/EIA-568B pin-out as shown in Table 11 below.

Table 11: J9A & J9B Ethernet RJ45 Pin Assignments

Pin	Signal	Type
1	TX RX A P	I/O
2	TX RX A N	I/O
3	TX RX B P	I/O
4	TX RX C P	I/O
5	TX RX C N	I/O
6	TX RX B N	I/O
7	TX RX D P	I/O
8	TX RX D N	I/O

The Ethernet PHY, Micrel KSZ9031, for each interface is located on the Development Board and will auto-negotiate to the speed of the device it is connected to. The Ethernet PHYs are connected to the module through the EMAC0 and EMAC1 interfaces of the AM57xx processor to the pins as shown in Table 12 below.

Table 12: Ethernet PHY to EMAC0 and EMAC1 SOM Interfaces

EMAC0 – J9A (Lower)		EMAC1 – J9B (Upper)	
PHY to SOM Interface Signal	SOM Pin	PHY to SOM Interface Signal	SOM Pin
R EMAC0_RXD0	J10 – 120	R EMAC1_RXD0	J10 – 156
R EMAC0_RXD1	J10 – 118	R EMAC1_RXD1	J10 – 154
R EMAC0_RXD2	J10 – 116	R EMAC1_RXD2	J10 – 152
R EMAC0_RXD3	J10 – 114	R EMAC1_RXD3	J10 – 150
R EMAC0_RX_CLK	J10 – 124	R EMAC1_RX_CLK	J10 – 160
R EMAC0_RX_CTL	J10 – 122	R EMAC1_RX_CTL	J10 – 158
R EMAC0_TXD0	J10 – 100	R EMAC1_TXD0	J10 – 136
R EMAC0_TXD1	J10 – 102	R EMAC1_TXD1	J10 – 138
R EMAC0_TXD2	J10 – 104	R EMAC1_TXD2	J10 – 140
R EMAC0_TXD3	J10 – 106	R EMAC1_TXD3	J10 – 142
R EMAC0_TX_CLK	J10 – 108	R EMAC1_TX_CLK	J10 – 144
R EMAC0_TX_CTL	J10 – 110	R EMAC1_TX_CTL	J10 – 146
MDIO_DATA	J10 – 159	MDIO_DATA	J10 – 159
MDIO_CLK	J10 – 161	MDIO_CLK	J10 – 161
R EMAC0_RESETh	J10 – 157	R EMAC1_RESETh	J10 – 278

Dual 10/100 Mbit PRU Ethernet – J8

The MitySOM-AM57(F) Development Board provides two RJ-45 connections, with link and activity LEDs, for dual 10/100 Megabit Ethernet from the Second Programmable Real-time Unit (PRU2) of the AM57xx processor. These external connections follow the standard TIA/EIA-568B pin-out as shown in Table 11 below.

Table 13: J8A & J8B Ethernet RJ45 Pin Assignments

Pin	Signal	Type
1	TX RX A P	I/O
2	TX RX A N	I/O
3	TX RX B P	I/O
4	No Connect	I/O
5	No Connect	I/O
6	TX RX B N	I/O
7	No Connect	I/O
8	No Connect	I/O

The Ethernet PHY, DP83822, for each interface is located on the Development Board and will auto-negotiate the speed of the device it is connected to. The Ethernet PHYs are connected to the module through the PR2 MII0 and PR2 MII1 interfaces of the AM57xx processor to the pins as shown in Table 12 below.

Table 14: Ethernet PHY to PR2 MII0 and PR2 MII 1 SOM Interfaces

PR2 MII0 – J8A (Lower)		PR2 MII1 – J8B (Upper)	
PHY to SOM Interface Signal	SOM Pin	PHY to SOM Interface Signal	SOM Pin
PR2 MII0 TXD3	J10 – 228	PR2 MII1 TXD3	J10 – 194
PR2 MII0 TXD2	J10 – 226	PR2 MII1 TXD2	J10 – 192
PR2 MII0 TXD1	J10 – 224	PR2 MII1 TXD1	J10 – 190
PR2 MII0 TXD0	J10 – 222	PR2 MII1 TXD0	J10 – 188
PR2 MII0 TXEN	J10 – 220	PR2 MII1 TXEN	J10 – 186
PR2 MII MT0 CLK	J10 – 218	PR2 MII MT1 CLK	J10 – 184
PR2 MII0 RXD3	J10 – 214	PR2 MII1 RXD3	J10 – 180
PR2 MII0 RXD2	J10 – 212	PR2 MII1 RXD2	J10 – 178
PR2 MII0 RXD1	J10 – 210	PR2 MII1 RXD1	J10 – 176
PR2 MII0 RXD0	J10 – 208	PR2 MII1 RXD0	J10 – 174
PR2 MII MR0 CLK	J10 – 198	PR2 MII MR1 CLK	J10 – 164
PR2 MII0 RXER	J10 – 204	PR2 MII1 RXER	J10 – 170
PR2 MII0 RXDV	J10 – 200	PR2 MII1 RXDV	J10 – 166
PR2 MII0 CRS	J10 – 202	PR2 MII1 CRS	J10 – 168
PR2 MII0 RXLINK	J10 – 216	PR2 MII1 RXLINK	J10 – 182
PR2 MII0 COL	J10 – 206	PR2 MII1 COL	J10 – 172
PRU2 MII0 INT*	J10 – 250	PRU2 MII1 INT*	J10 – 237
PRU2 MII0 RESET _n	J10 – 248	PRU2 MII1 RESET _n	J10 – 273
PR2 MDIO MDCLK	J10 – 111	PR2 MDIO MDCLK	J10 – 111
PR2 MDIO DATA	J10 - 113	PR2 MDIO DATA	J10 – 113

HDMI (Video Only) – J2

The MitySOM-AM57(F) Development Board provides a 19-pin standard HDMI connector, J2, supporting video only, which is driven by the AM57xx processor. Supporting HDMI 1.4a, the MitySOM-AM57(F) can output up to a resolution of 1920x1080 pixels at 60Hz.

Table 15: J2 Connector Pin Assignments

J2 Pin	J2 Signal	Type	SOM Interface Signal	SOM Pin
1	TMDS Data2+	O	HDMI_TX2_P	J14 – 4
2	Shield	Power	GND	N/A
3	TMDS Data2-	O	HDMI_TX2_N	J14 – 6
4	TMDS Data1+	O	HDMI_TX1_P	J14 – 10
5	Shield	Power	GND	N/A
6	TMDS Data1-	O	HDMI_TX1_N	J14 – 12
7	TMDS Data0+	O	HDMI_TX0_P	J14 – 16
8	Shield	Power	GND	N/A
9	TMDS Data0-	O	HDMI_TX0_N	J14 – 18
10	TMDS Clock+	O	HDMI_CLK_P	J14 – 22
11	Shield	Power	GND	N/A
12	TMDS Clock-	O	HDMI_CLK_N	J14 – 24
13	CEC	IO	HDMI_CEC_A	J14 – 5
14	Reserved	-	No Connect	N/A
15	SCL	IO	HDMI1_DDC_SCL	J14 – 7
16	SDA	IO	HDMI1_DDC_SDA	J14 – 9
17	GND	Power	GND	N/A
18	+5.0V	Power	+5v0	N/A
19	Hot Plug Detect	O	HDMI_HPD_A	J14 - 3

SATA – J12

Table 16 describes the pin-out of the SATA connector on the MitySOM-AM57(F) Development Board which is connected from the AM57xx processor through a SATA redriver.

Table 16: J12 Pin Assignments

Pin	Signal	SOM Pin	Type	Notes
1	GND	-	POWER	
2	CON SATA_TX_P	J14 – 50	O	
3	CON SATA_TX_N	J14 – 52	O	
4	GND	-	POWER	
5	CON SATA_RX_N	J14 – 56	I	
6	CON SATA_RX_P	J14 - 58	I	
7	GND	-	POWER	

Note: Any SATA device must be powered externally from the development board and care should be taken to ensure proper power supply grounding between devices.

3x 34-Pin Expansion Ports – J5, J11 & J18

The MitySOM-AM57(F) Development Kit provides three 34-pin general expansion connectors, J5, J11 & J18 which utilize standard dual-row 0.1-inch spaced headers. The signals for each connector are listed in the following tables.

Table 17: J5 Connector Pin Assignments

Pin	Signal	SOM Pin	Type	Standard	Notes
1	+1.8V	N/A	Power		See Electrical Characteristics for maximum external current rating of +1.8V supply.
2	GND	N/A	Power		
3	+1.8V	N/A	Power		See Electrical Characteristics for maximum external current rating of +1.8V supply.
4	GND	N/A	Power		
5	GPIO1_29.P5	J10 - 187	AM57xx IO	1.8V	
6	EXT_WAKE	J10 – E4-4	AM57xx	1.8V	10.0k pull-down installed on module. Connected to AM57xx ball AC17.
7	GPIO1_14.G20	J10 - 189	AM57xx IO	1.8V	
8	GPIO2_1.P9	J10 - 183	AM57xx IO	1.8V	
9	GPIO7_23.C26	J10 - 201	AM57xx IO	1.8V	
10	GPIO2_0.N9	J10 - 181	AM57xx IO	1.8V	
11	GPIO7_8.F16	J10 - 199	AM57xx IO	1.8V	
12	GPIO1_30.N7	J10 - 215	AM57xx IO	1.8V	
13	GPIO1_31.R4	J10 - 217	AM57xx IO	1.8V	
14	GPIO5_5.J11	J10 - 213	AM57xx IO	1.8V	
15	GPIO1_28.R5	J10 - 219	AM57xx IO	1.8V	
16	GPIO5_4.G13	J10 - 211	AM57xx IO	1.8V	
17	GPIO4_20.B10	J10 – 267	AM57xx IO	1.8V	
18	GPIO7_15.B22	J10 – 229	AM57xx IO	1.8V	
19	GPIO4_19.D11	J10 – 269	AM57xx IO	1.8V	

20	GPIO4_10.E6	J10 – 261	AM57xx IO	1.8V	
21	GPIO3_28.E1	J10 – 243	AM57xx IO	1.8V	
22	GPIO4_9.F5	J10 – 259	AM57xx IO	1.8V	
23	GPIO4_4.E2	J10 – 245	AM57xx IO	1.8V	
24	GPIO2_9.K7	J10 – 147	AM57xx IO	1.8V	
25	GPIO4_12.F6	J10 – 263	AM57xx IO	1.8V	
26	GPIO2_10.M7	J10 – 149	AM57xx IO	1.8V	
27	GPIO4_0.G6	J10 – 265	AM57xx IO	1.8V	
28	No Connect	N/A	NC		
29	No Connect	N/A	NC		
30	No Connect	N/A	NC		
31	GND	N/A	Power		
32	GND	N/A	Power		
33	GND	N/A	Power		
34	GND	N/A	Power		

Table 18: J11 Connector Pin Assignments

Pin	Signal	SOM Pin	Type	Standard	Notes
1	+1.8V	N/A	Power		See Electrical Characteristics for maximum external current rating of +1.8V supply.
2	GND	N/A	Power		
3	+1.8V	N/A	Power		See Electrical Characteristics for maximum external current rating of +1.8V supply.
4	GND	N/A	Power		
5	GPIO4_23.E11	J10-271	AM57xx IO	1.8V	
6	GPIO7_7.A25	J10-272	AM57xx IO	1.8V	
7	GPIO4_1.F4	J10-241	AM57xx IO	1.8V	
8	GPIO2_2.P4	J10-179	AM57xx IO	1.8V	
9	GPIO1_15.G19	J10-191	AM57xx IO	1.8V	
10	GPIO5_19.Y1	J10-105	AM57xx IO	1.8V	
11	GPIO7_6.T7	J10-205	AM57xx IO	1.8V	
12	GPIO5_18.V2	J10 – 107	AM57xx IO	1.8V	

13	GPIO7_5.T6	J10 – 203	AM57xx IO	1.8V	
14	GPIO7_16.G17	J10 – 195	AM57xx IO	1.8V	
15	GPIO6_16.F21	J10 – 223	AM57xx IO	1.8V	
16	GPIO7_4.T9	J10 – 209	AM57xx IO	1.8V	
17	GPIO7_3.R6	J10 – 221	AM57xx IO	1.8V	
18	GPIO4_2.F3	J10 – 239	AM57xx IO	1.8V	
19	GPIO3_29.G2	J10 – 235	AM57xx IO	1.8V	
20	GPIO7_9.B25	J10 – 274	AM57xx IO	1.8V	
21	GPIO4_3.D1	J10 – 247	AM57xx IO	1.8V	
22	GPIO4_11.D3	J10 – 253	AM57xx IO	1.8V	
23	GPIO2_11.J5	J10 – 151	AM57xx IO	1.8V	
24	GPIO4_7.C1	J10 – 251	AM57xx IO	1.8V	
25	GPIO2_12.K6	J10 – 153	AM57xx IO	1.8V	
26	GPIO4_8.E4	J10 – 255	AM57xx IO	1.8V	
27	No Connect	N/A	NC		
28	GPIO7_14.A26	J10 – 276	AM57xx IO	1.8V	
29	No Connect	N/A	NC		
30	No Connect	N/A	NC		
31	GND	N/A	Power		
32	GND	N/A	Power		
33	GND	N/A	Power		
34	GND	N/A	Power		

Table 19: J18 Connector Pin Assignments

Pin	Signal	SOM Pin	Type	Standard	Notes
1	+1.8V	N/A	Power		See Electrical Characteristics for maximum external current rating of +1.8V supply.
2	GND	N/A	Power		
3	+1.8V	N/A	Power		See Electrical Characteristics for maximum external current rating of +1.8V supply.
4	GND	N/A	Power		

5	PR2_PRU1_GPO4.AA4	J14 – 33	AM57xx IO	1.8V	
6	PR2_PRU1_GPO1.AA3	J14 – 17	AM57xx IO	1.8V	
7	PR2_PRU1_GPO3.AB3	J14 - 35	AM57xx IO	1.8V	
8	PR2_PRU1_GPO2.AB9	J14 - 19	AM57xx IO	1.8V	
9	GPIO7_10.A24	J14 – 11	AM57xx IO	1.8V	
10	GPIO3_16.AF2	J14 – 63	AM57xx IO	1.8V	
11	GPIO2_30.AG8	J14 – 13	AM57xx IO	1.8V	
12	GPIO3_20.AF1	J14 – 65	AM57xx IO	1.8V	
13	GPIO3_17.AF6	J14 – 29	AM57xx IO	1.8V	
14	GPIO3_18.AF3	J14 – 67	AM57xx IO	1.8V	
15	GPIO3_25.AE6	J14 – 31	AM57xx IO	1.8V	
16	GPIO3_24.AE2	J14 – 69	AM57xx IO	1.8V	
17	GPIO3_12.AG4	J14 – 53	AM57xx IO	1.8V	
18	GPIO3_26.AD2	J14 – 71	AM57xx IO	1.8V	
19	GPIO3_11.AH4	J14 – 55	AM57xx IO	1.8V	
20	GPIO3_21.AE3	J14 – 62	AM57xx IO	1.8V	
21	GPIO3_14.AG3	J14 – 57	AM57xx IO	1.8V	
22	GPIO3_19.AF4	J14 – 64	AM57xx IO	1.8V	
23	GPIO3_8.AH3	J14 – 59	AM57xx IO	1.8V	
24	GPIO3_22.AE5	J14 – 66	AM57xx IO	1.8V	
25	GPIO3_13.AG2	J14 – 61	AM57xx IO	1.8V	
26	GPIO3_27.AD3	J14 – 68	AM57xx IO	1.8V	
27	ADC_FPGA_VN_0.L9 ¹	J14 – 97	Artix-7 Input	1.8V	(Negative) XADC 12-Bit 1MSPS ADC from Artix-7 FPGA
28	FPGA_DNX.M9 ¹	J14 – 93	Artix-7 Output		Negative thermocouple diode output from Artix-7 FPGA.

29	ADC_FPGA_VP_0.K10 ²	J14 – 99	Artix-7 Input	1.8V	(Positive) XADC 12-Bit 1MSPS ADC from Artix-7 FPGA
30	FPGA_DXP.M10 ¹	J14 – 95	Artix-7 Output		Positive thermocouple diode output from Artix-7 FPGA.
31	GND	N/A	Power		
32	GND	N/A	Power		
33	GND	N/A	Power		
34	GND	N/A	Power		

1. These signals are not connected to the MitySOM-AM57 non-FPGA variant.
2. These signals are connected to multi-functional IO on the MitySOM-AM57 non-FPGA variant.

WiFi/Bluetooth Expansion Port – J3

The MitySOM-AM57(F) Development Kit incorporates a 100-pin expansion connector, J3, which is directly compatible with the Texas Instruments WL1837MODCOM8I WiFi and Bluetooth expansion card. This connector, MEC6-150-02-L-D-RA1, can also be utilized for a custom expansion card and has the following pinout.

Table 20: J3 Connector Pin Assignments

Pin	Signal	SOM Pin	Pin	Signal	SOM Pin
1	No Connect	N/A	2	GND	N/A
3	GND	N/A	4	WLAN_EN	J14 – 21
5	+3.3V ¹	N/A	6	GND	N/A
7	+3.3V ¹	N/A	8	+1.8V ¹	N/A
9	GND	N/A	10	No Connect	N/A
11	WL_RS232_TX	J10 – 231	12	No Connect	N/A
13	WL_RS232_RX	J10 – 233	14	No Connect	N/A
15	WL_UART_DBG	J10 – 115	16	No Connect	N/A
17	No Connect	N/A	18	GND	N/A
19	GND	N/A	20	WL_SDIO_CLK	J10 – 135
21	No Connect	N/A	22	GND	N/A
23	No Connect	N/A	24	WL_SDIO_CMD	J10 – 137
25	No Connect	N/A	26	WL_SDIO_D0	J10 – 139
27	No Connect	N/A	28	WL_SDIO_D1	J10 – 141
29	No Connect	N/A	30	WL_SDIO_D2	J10 – 143
31	No Connect	N/A	32	WL_SDIO_D3	J10 – 145
33	No Connect	N/A	34	WLAN_IRQ	J14 – 41
35	No Connect	N/A	36	No Connect	N/A
37	GND	N/A	38	No Connect	N/A
39	No Connect	N/A	40	No Connect	N/A
41	No Connect	N/A	42	GND	N/A
43	No Connect	N/A	44	No Connect	N/A
45	No Connect	N/A	46	No Connect	N/A
47	GND	N/A	48	No Connect	N/A
49	No Connect	N/A	50	No Connect	N/A
51	No Connect	N/A	52	BT_PCM_IF_CLK	J10 – 121
53	No Connect	N/A	54	BT_PCM_IF_FSYNC	J10 – 123
55	No Connect	N/A	56	BT_PCM_IF_DIN	J10 – 119

57	No Connect	N/A	58	BT_PCM_IF_DOUT	J10 – 117
59	No Connect	N/A	60	GND	N/A
61	No Connect	N/A	62	No Connect	N/A
63	GND	N/A	64	GND	N/A
65	No Connect	N/A	66	BT_UART_IF_TX	J10 – 227
67	No Connect	N/A	68	BT_UART_IF_RX	J10 – 193
69	No Connect	N/A	70	BT_UART_IF_CTS	J10 – 257
71	No Connect	N/A	72	BT_UART_IF_RTS	J10 – 249
73	No Connect	N/A	74	No Connect	N/A
75	No Connect	N/A	76	BT_UART_DEBUG	J10 – 275
77	GND	N/A	78	WLAN_GPIO9	J14 – 37
79	No Connect	N/A	80	No Connect	N/A
81	No Connect	N/A	82	No Connect	N/A
83	GND	N/A	84	No Connect	N/A
85	No Connect	N/A	86	No Connect	N/A
87	GND	N/A	88	No Connect	N/A
89	WLAN_BT_EN	J14 – 39	90	No Connect	N/A
91	No Connect	N/A	92	GND	N/A
93	No Connect	N/A	94	No Connect	N/A
95	GND	N/A	96	WLAN_GPIO11	J14 – 25
97	GND	N/A	98	WLAN_GPIO12	J14 – 27
99	No Connect	N/A	100	WLAN_GPIO10	J14 – 23

All IO signals are 1.8V logic levels and connected to the AM57xx processor of the MitySOM-AM57(F) module.

1. See Electrical Characteristics for maximum external current rating of +1.8V and +3.3V supplies.

FMC Expansion Port – J1

Table 21.1 to Table 21.10 describes the pin-out of the 400-pin FMC interface, connector part number ASP-134486-01, on the MitySOM-AM57(F) development board.

The Vselect voltage is based upon the Vselect jumper currently installed on the MitySOM-AM57(F) Development Baseboard, see the FPGA IO Voltage Select Jumper – JP4/JP5/JP6 section for further details.

The I/O “type” is in reference to the signal direction from the SOM/development board.

Please see the following VITA documentation concerning the FMC specification (<https://www.vita.com/fmc>).

Table 21.1: J1 FMC Connector Pin A1-A40 Assignments

FMC Pin	FMC Signal	Baseboard/SOM Signal	SOM Pin	Type
A1	GND	GND	-	POWER
A2	DP1 M2C P	FPGA GXB RX1 P ¹	J14 – 98	I
A3	DP1 M2C N	FPGA GXB RX1 N ¹	J14 – 96	I
A4	GND	GND	-	POWER
A5	GND	GND	-	POWER
A6	DP2 M2C P	GND	-	POWER
A7	DP2 M2C N	Vselect	-	POWER
A8	GND	GND	-	POWER
A9	GND	GND	-	POWER
A10	DP3 M2C P	GND	-	POWER
A11	DP3 M2C N	Vselect	-	POWER
A12	GND	GND	-	POWER
A13	GND	GND	-	POWER
A14	DP4 M2C P	Vselect	-	POWER
A15	DP4 M2C N	GND	-	POWER
A16	GND	GND	-	POWER
A17	GND	GND	-	POWER
A18	DP5 M2C P	GND	-	POWER
A19	DP5 M2C N	Vselect	-	POWER
A20	GND	GND	-	POWER
A21	GND	GND	-	POWER
A22	DP1 C2M P	FPGA GXB TX1 P ¹	J14 – 92	O
A23	DP1 C2M N	FPGA GXB TX1 N ¹	J14 – 90	O
A24	GND	GND	-	POWER
A25	GND	GND	-	POWER
A26	DP2 C2M P	GND	-	POWER
A27	DP2 C2M N	Vselect	-	POWER
A28	GND	GND	-	POWER
A29	GND	GND	-	POWER
A30	DP3 C2M P	GND	-	POWER
A31	DP3 C2M N	Vselect	-	POWER
A32	GND	GND	-	POWER
A33	GND	GND	-	POWER
A34	DP4 C2M P	GND	-	POWER
A35	DP4 C2M N	Vselect	-	POWER
A36	GND	GND	-	POWER
A37	GND	GND	-	POWER
A38	DP5 C2M P	GND	-	POWER
A39	DP5 C2M N	Vselect	-	POWER
A40	GND	GND	-	POWER

1. These signals are connected to the AM57xx processor PCIe signals on the MitySOM-AM57x non-FPGA variant.

Table 21.2: J1 FMC Connector Pin B1-B40 Assignments

FMC Pin	FMC Signal	Baseboard/SOM Signal	SOM Pin	Type
B1	CLK DIR	GND ¹	-	-
B2	GND	GND	-	POWER
B3	GND	GND	-	POWER
B4	DP9 M2C P	GND	-	POWER
B5	DP9 M2C N	Vselect	-	POWER
B6	GND	GND	-	POWER
B7	GND	GND	-	POWER
B8	DP8 M2C P	GND	-	POWER
B9	DP8 M2C N	Vselect	-	POWER
B10	GND	GND	-	POWER
B11	GND	GND	-	POWER
B12	DP7 M2C P	GND	-	POWER
B13	DP7 M2C N	Vselect	-	POWER
B14	GND	GND	-	POWER
B15	GND	GND	-	POWER
B16	DP6 M2C P	GND	-	POWER
B17	DP6 M2C N	Vselect	-	POWER
B18	GND	GND	-	POWER
B19	GND	GND	-	POWER
B20	GBTCLK1 M2C P	No Connect ²	-	-
B21	GBTCLK1 M2C N	No Connect ²	-	-
B22	GND	GND	-	POWER
B23	GND	GND	-	POWER
B24	DP9 C2M P	GND	-	POWER
B25	DP9 C2M N	Vselect	-	POWER
B26	GND	GND	-	POWER
B27	GND	GND	-	POWER
B28	DP8 C2M P	GND	-	POWER
B29	DP8 C2M N	Vselect	-	POWER
B30	GND	GND	-	POWER
B31	GND	GND	-	POWER
B32	DP7 C2M P	GND	-	POWER
B33	DP7 C2M N	Vselect	-	POWER
B34	GND	GND	-	POWER
B35	GND	GND	-	POWER
B36	DP6 C2M P	GND	-	POWER
B37	DP6 C2M N	Vselect	-	POWER
B38	GND	GND	-	POWER
B39	GND	GND	-	POWER
B40	RES0	No Connect	-	-

1: 100k ohm resistor to GND

2: R6 and R7 can be installed to connect FPGA_BXB_REF_CLK_P/N respectively

Table 21.3: J1 FMC Connector Pin C1-C40 Assignments

FMC Pin	FMC Signal	Baseboard/SOM Signal	SOM Pin	Type
C1	GND	GND	-	POWER
C2	DP0 C2M P	FPGA GXB TX0 P ³	J14 – 80	O
C3	DP0 C2M N	FPGA GXB TX0 N ³	J14 – 78	O
C4	GND	GND	-	POWER
C5	GND	GND	-	POWER
C6	DP0 M2C P	FPGA GXB RX0 P ³	J14 – 86	I
C7	DP0 M2C N	FPGA GXB RX0 N ³	J14 – 84	I
C8	GND	GND	-	POWER
C9	GND	GND	-	POWER
C10	LA06 P	LA06 P	J10 – 23	IO ²
C11	LA06 N	LA06 N	J10 – 25	IO ²
C12	GND	GND	-	POWER
C13	GND	GND	-	POWER
C14	LA10 P	LA10 P	J10 – 17	IO ²
C15	LA10 N	LA10 N	J10 – 15	IO ²
C16	GND	GND	-	POWER
C17	GND	GND	-	POWER
C18	LA14 P	LA14 P	J10 – 7	IO ²
C19	LA14 N	LA14 N	J10 – 5	IO ²
C20	GND	GND	-	POWER
C21	GND	GND	-	POWER
C22	LA18 P CC	LA18 P	J10 – E3-9	IO ²
C23	LA18 N CC	LA18 N	J10 – E3-10	IO ²
C24	GND	GND	-	POWER
C25	GND	GND	-	POWER
C26	LA27 P	LA27 P	J10 – 63	IO ²
C27	LA27 N	LA27 N	J10 – 65	IO ²
C28	GND	GND	-	POWER
C29	GND	GND	-	POWER
C30	SCL	I2C5 SCL 3v3	J10 – 185	O
C31	SDA	I2C5 SDA 3v3	J10 – 207	IO
C32	GND	GND	-	POWER
C33	GND	GND	-	POWER
C34	GA0	GND	-	POWER
C35	12P0V	+12V FMC ¹	-	POWER
C36	GND	GND	-	POWER
C37	12P0V	+12V FMC ¹	-	POWER
C38	GND	GND	-	POWER
C39	3P3V	+3.3V	-	POWER
C40	GND	GND	-	POWER

1: +12V_FMC is enabled on the MitySOM-AM57(F) Development Board by the RMC_12v_Enable signal which is automatically enabled when the Power Good signal of the +12V to +3.3V power supply on the Development Board is enabled.

2: IO Voltage based upon Vselect jumper currently installed on Development Board

3. These signals are connected to the AM57xx processor PCIe signals on the MitySOM-AM57x non-FPGA variant.

Table 21.4: J1 FMC Connector Pin D1-D40 Assignments

FMC Pin	FMC Signal	Baseboard/SOM Signal	SOM Pin	Type
D1	PG C2M	PG C2M 3V3 ¹		IO
D2	GND	GND	-	POWER
D3	GND	GND	-	POWER
D4	GBTCLK0 M2C P	FPGA GXB REF CLK P ³	J14 – 72	I
D5	GBTCLK0 M2C N	FPGA GXB REF CLK N ³	J14 – 74	I
D6	GND	GND	-	POWER
D7	GND	GND	-	POWER
D8	LA01 P CC	LA01 P	J10 – 47	IO ²
D9	LA01 N CC	LA01 N	J10 – 45	IO ²
D10	GND	GND	-	POWER
D11	LA05 P	LA05 P	J10 – 39	IO ²
D12	LA05 N	LA05 N	J10 – 37	IO ²
D13	GND	GND	-	POWER
D14	LA09 P	LA09 P	J10 – 29	IO ²
D15	LA09 N	LA09 N	J10 – 27	IO ²
D16	GND	GND	-	POWER
D17	LA13 P	LA13 P	J10 – 19	IO ²
D18	LA13 N	LA13 N	J10 – 21	IO ²
D19	GND	GND	-	POWER
D20	LA17 P CC	LA17 P	J10 – 11	IO ²
D21	LA17 N CC	LA17 N	J10 – 9	IO ²
D22	GND	GND	-	POWER
D23	LA23 P	LA23 P	J10 – 3	IO ²
D24	LA23 N	LA23 N	J10 – 1	IO ²
D25	GND	GND	-	POWER
D26	LA26 P	LA26 P	J10 – 55	IO ²
D27	LA26 N	LA26 N	J10 – 57	IO ²
D28	GND	GND	-	POWER
D29	TCK	No Connect	-	NC
D30	TDI	No Connect	-	NC
D31	TDO	No Connect	-	NC
D32	3P3VAUX	+3.3V	-	POWER
D33	TMS	No Connect	-	NC
D34	TRST L	No Connect	-	NC
D35	GA1	GND	-	POWER
D36	3P3V	+3.3V	-	POWER
D37	GND	GND	-	POWER
D38	3P3V	+3.3V	-	POWER
D39	GND	GND	-	POWER
D40	3P3V	+3.3V	-	POWER

1: The PG_C2M_3V3 net has a 10.0k pull up to +3.3V installed, R1.

2: IO Voltage based upon Vselect jumper currently installed on Development Board

3. These signals are connected to the AM57xx processor ref clock PCIe signals on the MitySOM-AM57x non-FPGA variant.

Table 21.5: J1 FMC Connector Pin E1-E40 Assignments

FMC Pin	FMC Signal	Baseboard/SOM Signal	SOM Pin	Type
E1	GND	GND	-	POWER
E2	HA01 P CC	HA01 P	J10 – 99	IO ¹
E3	HA01 N CC	HA01 N	J10 – 101	IO ¹
E4	GND	GND	-	POWER
E5	GND	GND	-	POWER
E6	HA05 P	HA05 P	J10 – 72	IO ¹
E7	HA05 N	HA05 N	J10 – 74	IO ¹
E8	GND	GND	-	POWER
E9	HA09 P	HA09 P	J10 – 58	IO ¹
E10	HA09 N	HA09 N	J10 – 60	IO ¹
E11	GND	GND	-	POWER
E12	HA13 P	HA13 P	J10 – 50	IO ¹
E13	HA13 N	HA13 N	J10 – 52	IO ¹
E14	GND	GND	-	POWER
E15	HA16 P	No Connect	-	NC
E16	HA16 N	No Connect	-	NC
E17	GND	GND	-	POWER
E18	HA20 P	No Connect	-	NC
E19	HA20 N	No Connect	-	NC
E20	GND	GND	-	POWER
E21	HB03 P	No Connect	-	NC
E22	HB03 N	No Connect	-	NC
E23	GND	GND	-	POWER
E24	HB05 P	No Connect	-	NC
E25	HB05 N	No Connect	-	NC
E26	GND	GND	-	POWER
E27	HB09 P	No Connect	-	NC
E28	HB09 N	No Connect	-	NC
E29	GND	GND	-	POWER
E30	HB13 P	No Connect	-	NC
E31	HB13 N	No Connect	-	NC
E32	GND	GND	-	POWER
E33	HB19 P	GND	-	POWER
E34	HB19 N	GND	-	POWER
E35	GND	GND	-	POWER
E36	HB21 P	GND	-	POWER
E37	HB21 N	GND	-	POWER
E38	GND	GND	-	POWER
E39	VADJ	Vselect	-	POWER
E40	GND	GND	-	POWER

1: IO Voltage based upon Vselect jumper currently installed on Development Board

Table 21.6: J1 FMC Connector Pin F1-F40 Assignments

FMC Pin	FMC Signal	Baseboard/SOM Signal	SOM Pin	Type
F1	PG M2C	PG M2C ¹	-	PULL-UP ¹
F2	GND	GND	-	POWER
F3	GND	GND	-	POWER
F4	HA00 P CC	HA00 P	J10 – 97	IO ²
F5	HA00 N CC	HA00 N	J10 – 95	IO ²
F6	GND	GND	-	POWER
F7	HA04 P	HA04 P	J10 – 68	IO ²
F8	HA04 N	HA04 N	J10 – 70	IO ²
F9	GND	GND	-	POWER
F10	HA08 P	HA08 P	J10 – 56	IO ²
F11	HA08 N	HA08 N	J10 – 54	IO ²
F12	GND	GND	-	POWER
F13	HA12 P	HA12 P	J10 – 46	IO ²
F14	HA12 N	HA12 N	J10 – 48	IO ²
F15	GND	GND	-	POWER
F16	HA15 P	No Connect	-	NC
F17	HA15 N	No Connect	-	NC
F18	GND	GND	-	POWER
F19	HA19 P	No Connect	-	NC
F20	HA19 N	No Connect	-	NC
F21	GND	GND	-	POWER
F22	HB02 P	No Connect	-	NC
F23	HB02 N	No Connect	-	NC
F24	GND	GND	-	POWER
F25	HB04 P	No Connect	-	NC
F26	HB04 N	No Connect	-	NC
F27	GND	GND	-	POWER
F28	HB08 P	No Connect	-	NC
F29	HB08 N	No Connect	-	NC
F30	GND	GND	-	POWER
F31	HB12 P	No Connect	-	NC
F32	HB12 N	No Connect	-	NC
F33	GND	GND	-	POWER
F34	HB16 P	GND	-	POWER
F35	HB16 N	GND	-	POWER
F36	GND	GND	-	POWER
F37	HB20 P	GND	-	POWER
F38	HB20 N	GND	-	POWER
F39	GND	GND	-	POWER
F40	VADJ	Vselect	-	POWER

1: The PG_M2C net has a 10.0k pull up to +3.3V installed, R2.

2: IO Voltage based upon Vselect jumper currently installed on Development Board

Table 21.7: J1 FMC Connector Pin G1-G40 Assignments

FMC Pin	FMC Signal	Baseboard/SOM Signal	SOM Pin	Type
G1	GND	GND	-	POWER
G2	CLK1 M2C P	No Connect	-	NC
G3	CLK1 M2C N	No Connect	-	NC
G4	GND	GND	-	POWER
G5	GND	GND	-	POWER
G6	LA00 P CC	LA00 P	J10 – 43	IO ¹
G7	LA00 N CC	LA00 N	J10 – 41	IO ¹
G8	GND	GND	-	POWER
G9	LA03 P	LA03 P	J10 – 42	IO ¹
G10	LA03 N	LA03 N	J10 – 40	IO ¹
G11	GND	GND	-	POWER
G12	LA08 P	LA08 P	J10 – 34	IO ¹
G13	LA08 N	LA08 N	J10 – 32	IO ¹
G14	GND	GND	-	POWER
G15	LA12 P	LA12 P	J10 – 24	IO ¹
G16	LA12 N	LA12 N	J10 – 22	IO ¹
G17	GND	GND	-	POWER
G18	LA16 P	LA16 P	J10 – 16	IO ¹
G19	LA16 N	LA16 N	J10 – 14	IO ¹
G20	GND	GND	-	POWER
G21	LA20 P	LA20 P	J10 – 6	IO ¹
G22	LA20 N	LA20 N	J10 – 4	IO ¹
G23	GND	GND	-	POWER
G24	LA22 P	LA22 P	J10 – E4-9	IO ¹
G25	LA22 N	LA22 N	J10 – E4-8	IO ¹
G26	GND	GND	-	POWER
G27	LA25 P	LA25 P	J10 – 73	IO ¹
G28	LA25 N	LA25 N	J10 – 75	IO ¹
G29	GND	GND	-	POWER
G30	LA29 P	LA29 P	J10 – 93	IO ¹
G31	LA29 N	LA29 N	J10 – 91	IO ¹
G32	GND	GND	-	POWER
G33	LA31 P	LA31 P	J10 – 59	IO ¹
G34	LA31 N	LA31 N	J10 – 61	IO ¹
G35	GND	GND	-	POWER
G36	LA33 P	LA33 P	J10 – 77	IO ¹
G37	LA33 N	LA33 N	J10 – 79	IO ¹
G38	GND	GND	-	POWER
G39	VADJ	Vselect	-	POWER
G40	GND	GND	-	POWER

1: IO Voltage based upon Vselect jumper currently installed on Development Board

Table 21.8: J1 FMC Connector Pin H1-H40 Assignments

FMC Pin	FMC Signal	Baseboard/SOM Signal	SOM Pin	Type
H1	VREF A M2C ¹	No Connect	-	NC
H2	PRSNT M2C L	D3 – LED ²	-	LED
H3	GND	GND	-	POWER
H4	CLK0 M2C P	No Connect	-	NC
H5	CLK0 M2C N	No Connect	-	NC
H6	GND	GND	-	POWER
H7	LA02 P	LA02 P	J10 – 35	IO ³
H8	LA02 N	LA02 N	J10 – 33	IO ³
H9	GND	GND	-	POWER
H10	LA04 P	LA04 P	J10 – 38	IO ³
H11	LA04 N	LA04 N	J10 – 36	IO ³
H12	GND	GND	-	POWER
H13	LA07 P	LA07 P	J10 – 30	IO ³
H14	LA07 N	LA07 N	J10 – 28	IO ³
H15	GND	GND	-	POWER
H16	LA11 P	LA11 P	J10 – 20	IO ³
H17	LA11 N	LA11 N	J10 – 18	IO ³
H18	GND	GND	-	POWER
H19	LA15 P	LA15 P	J10 – 12	IO ³
H20	LA15 N	LA15 N	J10 – 10	IO ³
H21	GND	GND	-	POWER
H22	LA19 P	LA19 P	J10 – E4-10	IO ³
H23	LA19 N	LA19 N	J10 – 2	IO ³
H24	GND	GND	-	POWER
H25	LA21 P	LA21 P	J10 – E4-7	IO ³
H26	LA21 N	LA21 N	J10 – E4-6	IO ³
H27	GND	GND	-	POWER
H28	LA24 P	LA24 P	J10 – 83	IO ³
H29	LA24 N	LA24 N	J10 – 81	IO ³
H30	GND	GND	-	POWER
H31	LA28 P	LA28 P	J10 – 53	IO ³
H32	LA28 N	LA28 N	J10 – 51	IO ³
H33	GND	GND	-	POWER
H34	LA30 P	LA30 P	J10 – 71	IO ³
H35	LA30 N	LA30 N	J10 – 69	IO ³
H36	GND	GND	-	POWER
H37	LA32 P	LA32 P	J10 – 89	IO ³
H38	LA32 N	LA32 N	J10 – 87	IO ³
H39	GND	GND	-	POWER
H40	VADJ	Vselect	-	POWER

1: Vref already set to 0.9V on MitySOM-AM57(F)

2: When PRSNT_M2C_L is low (GND), LED D3, will illuminate

3: IO Voltage based upon Vselect jumper currently installed on Development Board

Table 21.9: J1 FMC Connector Pin J1-J40 Assignments

FMC Pin	FMC Signal	Baseboard/SOM Signal	SOM Pin	Type
J1	GND	GND	-	POWER
J2	CLK3 BIDIR P	No Connect	-	NC
J3	CLK3 BIDIR N	No Connect	-	NC
J4	GND	GND	-	POWER
J5	GND	GND	-	POWER
J6	HA03 P	HA03 P	J10 – 90	IO ¹
J7	HA03 N	HA03 N	J10 – 92	IO ¹
J8	GND	GND	-	POWER
J9	HA07 P	HA07 P	J10 – 66	IO ¹
J10	HA07 N	HA07 N	J10 – 64	IO ¹
J11	GND	GND	-	POWER
J12	HA11 P	HA11 P	J10 – 76	IO ¹
J13	HA11 N	HA11 N	J10 – 78	IO ¹
J14	GND	GND	-	POWER
J15	HA14 P	No Connect	-	NC
J16	HA14 N	No Connect	-	NC
J17	GND	GND	-	POWER
J18	HA18 P	No Connect	-	NC
J19	HA18 N	No Connect	-	NC
J20	GND	GND	-	POWER
J21	HA22 P	No Connect	-	NC
J22	HA22 N	No Connect	-	NC
J23	GND	GND	-	POWER
J24	HB01 P	No Connect	-	NC
J25	HB01 N	No Connect	-	NC
J26	GND	GND	-	POWER
J27	HB07 P	No Connect	-	NC
J28	HB07 N	No Connect	-	NC
J29	GND	GND	-	POWER
J30	HB11 P	No Connect	-	NC
J31	HB11 N	No Connect	-	NC
J32	GND	GND	-	POWER
J33	HB15 P	GND	-	POWER
J34	HB15 N	GND	-	POWER
J35	GND	GND	-	POWER
J36	HB18 P	GND	-	POWER
J37	HB18 N	GND	-	POWER
J38	GND	GND	-	POWER
J39	VIO_B M2C	No Connect	-	NC
J40	GND	GND	-	POWER

1: IO Voltage based upon Vselect jumper currently installed on Development Board

Table 21.10: J1 FMC Connector Pin K1-K40 Assignments

FMC Pin	FMC Signal	Baseboard/SOM Signal	SOM Pin	Type
K1	VREF_B_M2C ¹	-	-	NC
K2	GND	GND	-	POWER
K3	GND	GND	-	POWER
K4	CLK2_BIDIR_P	No Connect	-	NC
K5	CLK2_BIDIR_N	No Connect	-	NC
K6	GND	GND	-	POWER
K7	HA02_P	HA02_P	J10 – 88	IO ³
K8	HA02_N	HA02_N	J10 – 86	IO ³
K9	GND	GND	-	POWER
K10	HA06_P	HA06_P	J10 – 94	IO ³
K11	HA06_N	HA06_N	J10 – 96	IO ³
K12	GND	GND	-	POWER
K13	HA10_P	HA10_P	J10 – 82	IO ³
K14	HA10_N	HA10_N	J10 – 84	IO ³
K15	GND	GND	-	POWER
K16	HA17_P_CC	No Connect	-	NC
K17	HA17_N_CC	No Connect	-	NC
K18	GND	GND	-	POWER
K19	HA21_P	No Connect	-	NC
K20	HA21_N	No Connect	-	NC
K21	GND	GND	-	POWER
K22	HA23_P	No Connect	-	NC
K23	HA23_N	No Connect	-	NC
K24	GND	GND	-	POWER
K25	HB00_P_CC	No Connect	-	NC
K26	HB00_N_CC	No Connect	-	NC
K27	GND	GND	-	POWER
K28	HB06_P_CC	No Connect	-	NC
K29	HB06_N_CC	No Connect	-	NC
K30	GND	GND	-	POWER
K31	HB10_P	No Connect	-	NC
K32	HB10_N	No Connect	-	NC
K33	GND	GND	-	POWER
K34	HB14_P	No Connect	-	NC
K35	HB14_N	No Connect	-	NC
K36	GND	GND	-	POWER
K37	HB17_P_CC	GND	-	POWER
K38	HB17_N_CC	GND	-	POWER
K39	GND	GND	-	POWER
K40	VIO_B_M2C ²	No Connect	-	NC

1: Vref already set to 0.9V on MitySOM-AM57(F)

2: VIO_B already set to +1.8V on MitySOM-AM57(F)

3: IO Voltage based upon Vselect jumper currently installed on Development Board

I2C5 Expansion Port – J4

The 10-pin connector J4 allows external connections to the I2C5 interface from the AM57xx processor. Both +1.8V and +3.3V logic level connections for this interface are available on the connector as well as 1.8V and 3.3V power supply and ground connections. Please reference Table 5 for I2C5 address information. The pinout for this connector is shown below.

Table 22: J4 Connector Pin Assignments

Pin	Signal	SOM Pin	Type	Standard	Notes
1	I2C5_SCL_1v8	J10 - 185	I/O	1.8V	4.7k pull-up to 1.8V on Development Baseboard, R37.
2	I2C5_SCL_3v3	J10 - 185	I/O	3.3V	4.7k pull-up to 3.3V on Development Baseboard, R53.
3	I2C5_SDA_1v8	J10 - 207	I/O	1.8V	4.7k pull-up to 1.8V on Development Baseboard, R39.
4	I2C5_SDA_3v3	J10 - 207	I/O	3.3V	4.7k pull-up to 3.3V on Development Baseboard, R54.
5	+1.8V		Power		See Electrical Characteristics for maximum external current rating of +1.8V supply.
6	+3.3V		Power		See Electrical Characteristics for maximum external current rating of +3.3V supply.
7	No Connect		NC		
8	No Connect		NC		
9	GND		Power		
10	GND		Power		

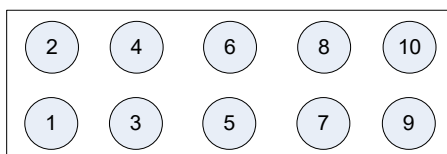


Figure 2: J4 Pin-out (Top View)

5V DC Fan Connector – J7

The 5V fan connector, J7, is a Molex 22-23-2021. The interface is designed to mate with a +5V DC cooling fan and is controlled, enabled by default, by the PMIC on the MitySOM-AM57(F) module. The connector pinout is described below:

Table 23: J7 Pin Out

J7 Pin	Signal	Note	SOM Pin
1	+5V	N/A	N/A
2	GND	Enabled by AUXFAN_EN	J10 – E3-4

Baseboard 256Kbit EEPROM – U11

The MitySOM-AM57(F) Development Board features a user-accessible CAT24C256WI-GT3 I2C accessible 256 Kbit EEPROM. Please reference Table 5 for I2C5 address information. The hardware write-protect feature on this EEPROM is not available.

MitySOM-AM57(F) +5V current/power monitor – U8

The MitySOM-AM57(F) Development Board features a LTC2945IMS I2C accessible power/current monitor and single-channel ADC. Please reference Table 5 for I2C5 address information.

The single ADC channel monitors the +12V power supply on the Development Board through a resistor divider with a ratio of ~0.0826/volt. With this divider, a value of 0.99V is expected for a 12.0V supply voltage.

The ALERT# output, Pin 10, from the power monitor, U8, is connected to MitySOM-AM57(F) Pin J10 – 246.

Development Board +5V, +3.3V, +2.5V and +1.8V voltage monitor – U10

The MitySOM-AM57(F) Development Board features an AD7995YRJZ I2C accessible 4 channel ADC which is used to measure/monitor the +5V, +3.3V, +2.5V, and +1.8V supplies generated on the Development Board. Please reference Table 5 for I2C5 address information.

The table below lists each channel, the voltage that it measures, and any resistor divider ratio used.

Table 24: U10 Pinout

U10 Pin	ADC Channel	Voltage Monitored	Ratio	Expected Value at Stated Voltage
3	0	+5.0V	0.5/volt	2.50V
4	1	+3.3V	0.5/volt	1.65V
5	2	+1.8V	1.0/volt	1.8V
6	3	+2.5V	1.0/volt	2.5V

Module Configuration Jumpers

Boot Configuration Jumper – JP8

The MitySOM-AM57(F) can be configured to boot using 2 different boot sequences according to the BOOTMODE jumper on the development board, JP8. The pin is pulled up to +1.8V on the SOM and results in the default boot mode being the “high” mode shown below. If the “low” mode is desired a jumper should be installed across JP8 which will cause the BOOTMODE pin of the MitySOM-AM57(F) (J10 – Pin 74) to be pulled to GND.

JP8 Removed (Default) “high”

1. SD card (MMC1)
2. eMMC (MMC2)
3. HS USB2.0 (USB1)

JP8 Installed “low”

1. On SOM Quad SPI NOR (QSPI1)
2. SD card (MMC1)
3. HS USB2.0 (USB1)

Please see the “AM57xx Boot Media Mode” section in the MitySOM-AM57(F) Datasheet for additional details.

FPGA IO Voltage Select Jumper – JP4/JP5/JP6

The Artix-7 FPGA user-controlled banks on the MitySOM-AM57(F) feature user-selectable IO voltages. On the MitySOM-AM57x Development Board VCCO_34 and VCCO_15 are powered by the same voltage, Vselect. This voltage level, either +3.3V, +2.5V, or +1.8V is selected by which jumper is installed on either JP4, JP5, or JP6. The table below lists the jumper settings.

Table 25: JP4, JP5, and JP6 Jumper Settings

JP4 (+3.3V)	JP5 (+2.5V)	JP6 (+1.8V)	VCCO 34 Voltage	VCCO 15 Voltage
Installed	Not Installed	Not Installed	+3.3V	+3.3V
Not Installed	Installed	Not Installed	+2.5V	+2.5V
Not Installed	Not Installed	Installed	+1.8V	+1.8V

Note that only one jumper should be installed at a given time.

PMIC Power Hold Jumper – JP7

The MitySOM-AM57(F) Development Board features a 3-pin jumper header to control the state of the PMIC_POWERHOLD signal to the module, J10 – Pin E3-7. By default, no jumper is installed on this header. The jumper settings are documented in the following table.

Table 26: J7 Settings

JP7 Setting	Module Power State
Pin 1 & 2 Shorted	Pulled High (+1.8V) Module is always on
Pin 2 & 3 Shorted Or All Pins Floating	(Default) Software control of module power through the PMIC on the MitySOM-AM57(F) module

Please see the MitySOM-AM57(F) Datasheet for additional details about the PMIC_POWERHOLD feature.

SOM Manual Reset Switch – S2

When switch S2 is pressed it connects the PB_RESETh signal to GND which causes the AM57xx processor on the MitySOM-AM57(F) to reset.

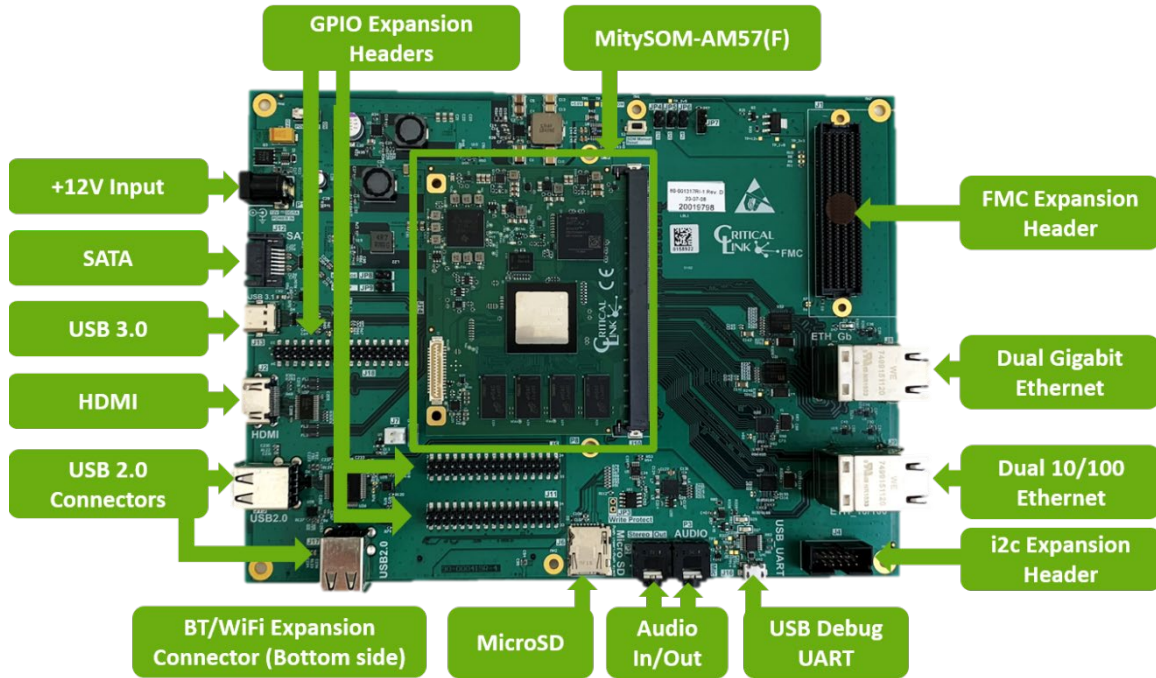
INCLUDED COMPONENTS

The following table lists the components that are included with a MitySOM-AM57(F) Development Kit. See Table 28 for specific development kit ordering information.

Table 27: Included Items

Description	Interface Port	Qty. Included
MitySOM-AM57(F) Development Kit Board	n/a	Qty. 1
MitySOM-AM57 or AM57F Module	n/a	Qty. 1
Micro USB Cable	J16	Qty. 1
12V 3.34A AC to DC Supply	P1	Qty. 1
Ethernet cable	J8 & J9	Qty. 1
Development Kit Schematic Files	n/a	
Development Kit Gerber Drawings	n/a	
Development Kit Bill Of Materials	n/a	

MitySOM-AM57(F) Development Kit Board with MitySOM-AM57(F) Module



ORDERING INFORMATION

Development Kits

The following table lists the standard MitySOM-AM57(F) Development Kit configurations. For shipping status, availability, and lead time of these or other configurations please contact your Critical Link representative.

Table 28: Standard Model Numbers

Development Kit Model	Module Included	Operating Temp
80-001428	5728-PJ-4AA-RC	0°C to 70°C
80-001429	5748-PJ-4AA-RI	-40°C to 85°C
80-001430	5749-PM-4AA-RI	-40°C to 85°C
80-001527	5729-PX-4AA-RC	0°C to 70°C
80-001528	5749-PX-4AA-RC	0°C to 70°C

MECHANICAL INTERFACE DESCRIPTION

Main Board Interface / Mounting

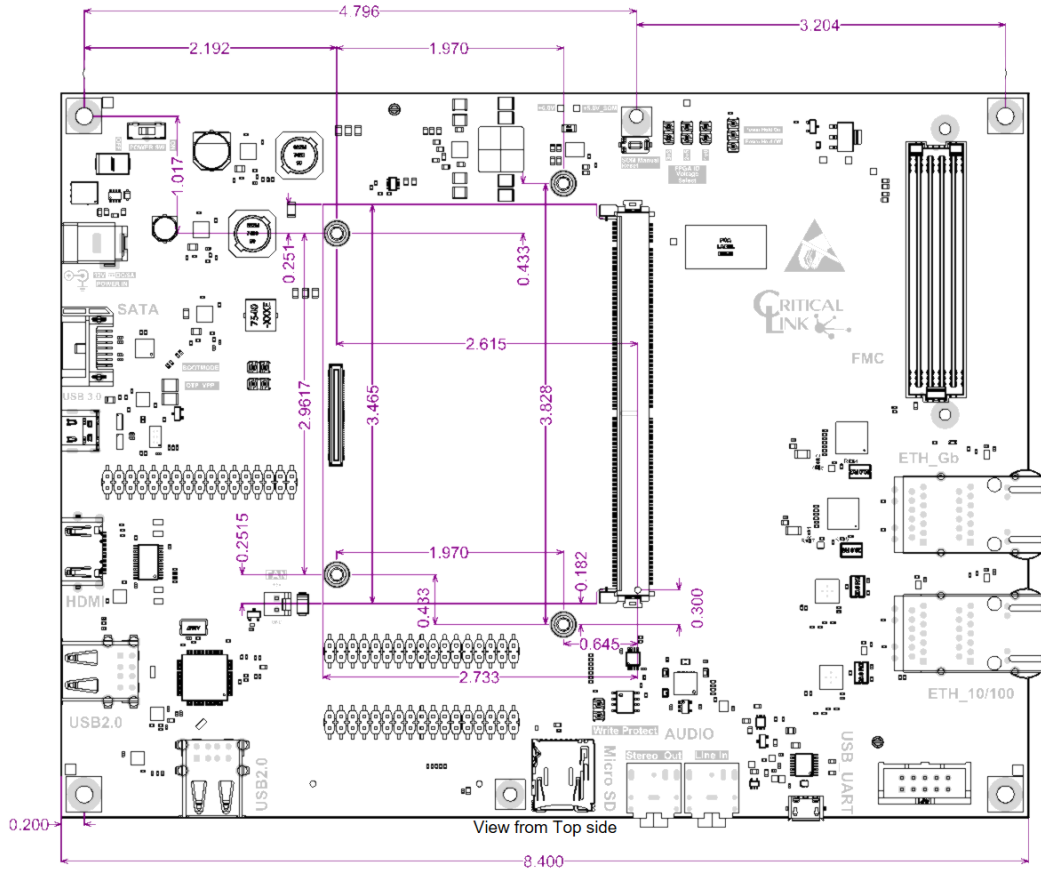


Figure 3: MitySOM-AM57(F) Development Kit Outline and Mounting Hole Locations (Top View, inches)

REVISION HISTORY

Date	Rev	Change Description
24-Sept-21	A	Initial Release
07-Jun-23	B	Update Table 28, available part numbers Update Table 21.1, correct Pins A14 and A15 Update Figure 3, MitySOM-AM57x mounting hole locations adjusted. Improved wording and formatting.