MitySOM™ Document

Document: MitySOM-AM57F Carrier Board Design Guide

Revision: 1.2

Date: November 6, 2024

1 Overview

1.1 MitySOM-AM57F Fast Facts for Getting Started

Facts	MitySOM-AM5728F, MitySOM-AM5748F, MitySOM-AM5749F
Required connectors placed on carrier board	JAE MM70-314B1-2-R300: card edge receptacle HiRose DF40HC(3.0)-100DS-0.4V(58) : fine-pitch hi-speed header
Input Voltages supplied from carrier board	+5V (to SOM on-board power supply / power management IC), +1.8 to +3.3V (FPGA bank I/O)
Supported I/O standards	LVTTL, LVCMOS33, LVCMOS25*, LVDS25*, LVCMOS18*
Total number of FPGA I/O's	96
Number of LVDS capable I/O's	48 pairs
SOC Cores, speeds	• 2x ARM Cortex-A15 @ 1500 MHz max. • 2x 66x floating point DSP cores @ 750 MHz max. • 2x ARM Cortex-M4 Image Processing Unit (IPU) @ 212.8 MHz max.
SOC Peripherals**	Video Processing: • LCD Display / HDMI support, Image Video Accelerator (IVA) • 3D Graphics Processing Unit (GPU), Video Processing Engine (VPE) • Embedded Video Engine (EVE): AM5749 only Program / Data Storage: • 2.5 MB on-chip shared RAM • General purpose memory controller (GPMC) • Dual DDR3 memory controller, dynamic memory manager (DMM) Interface Support: • Dual Controller Area Network (CAN) • Dual Ethernet (MII, RMII or RGMII interface support) • Up to 199x SOC General Purpose I/O (GPIO) • Up to 5x I2C, up to 8x Multichannel Audio Serial Port (McASP) • Multi Media Card, Secure Digital I/O (MMC, SD, SDIO): up to 4x • PCI Express 3.0, Serial Advanced Technology Attachment (SATA) • up to 4x Multi-channel Serial Peripheral Interface (McSPI) • Quad Serial Peripheral Interface (QSPI) • up to 10x Universal Asynchronous Receiver/Transmitter (UART) • USB 3.0 with SuperSpeed, dual role device support • USB 2.0: with high speed, dual role device support
*Requires external bank voltage supply according to standard **Peripherals share pins, see AM57x datasheets and PINMUX utility for valid pin multiplexing configurations	

1.2 Introduction

The MitySOM-AM5728F, MitySOM-AM5748F and MitySOM-AM5749F modules (collectively referred to as MitySOM-AM57F) are System-On-Modules (SOMs) designed to be easy to integrate into an end-user embedded system. The modules integrate many crucial elements of an embedded system and do so with an established design framework utilizing a common set of core libraries. End-user design of the application PCB is also intended to be as simple as possible, allowing the PCB designer to concentrate on the custom I/O interfaces – especially analog & mixed-signal – instead of getting distracted with the learning curve of designing a brand new embedded digital system from scratch.

Developers are encouraged to review the MitySOM-AM57x Development Kit design schematics, available on the Critical Link support site. The Development Kit has been qualified with a full software support package available for the interfaces and devices on the board. Customers may contact Critical Link for access to Altium CAD design files for the development kit and for design reviews, email support@criticallink.com

A schematic design checklist is available from the Critical Link support Wiki for customer carrier boards designed around AM57x SOM series. The checklist is a baseline for Critical Link reviews of customer designs. Please see "Reference Documents and Links" section of this document for a link.

1.3 MitySOM-AM57F Family Modules

The MitySOM-AM57F family of modules represents a 5th generation SOM in the MityDSP/MitySOM product line. These modules are based on Texas Instruments AM57x System-On-Chip (SOC) Sitara processors. Each of these SOC devices are footprint-compatible devices using a 760-PBGA package with summary features described in section 1.1 (Fast Facts) above.

Each MitySOM-AM57F SOM includes a power supply & management subsystem, DDR3 SDRAM, NOR FLASH memory, and interfaces to a carrier board with a 314-pin low-profile MXM card-edge receptable and a 100-position, fine-pitch, low-profile connector set. AM57F SOMs also integrate a Xilinx/AMD Artix-7 FPGA for end-user customizable logic and I/O interfaces beyond the capability of the SOC device. Carrier board design for the "F" type of MitySOM (with FPGA) is the main focus of this document.

MitySOM-AM57F products are available with options for AM57x SOC device variant, RAM and FLASH memory depth, FPGA size and operating temperature range. Please visit the "MITYSOM-AM57F" product page or contact Critical Link for the current list of orderable MitySOM-AM57x part numbers.

1.4 MitySOM-AM57 Family Modules (No FPGA)

Available alternates to the MitySOM-AM57F family have no Artix-7 FPGA installed. This "AM57" (no "F") SOM type is less expensive and requires less power than a comparable AM57F SOM with FPGA. IO pins reserved for the FPGA on the AM57F SOM are routed to additional peripheral interfaces on the SOC processor. See separate SOM datasheets and carrier board design guide for the MitySOM-AM57 module types.

1.5 SOM Dimensions

The dimensions of the MitySOM-AM57F are 88.00mm (~3.46in) x 69.42mm (~2.73in) and features two mounting holes at the end of the SOM where the 100-pin connector, J3, is located. See Figure 1 for top view.

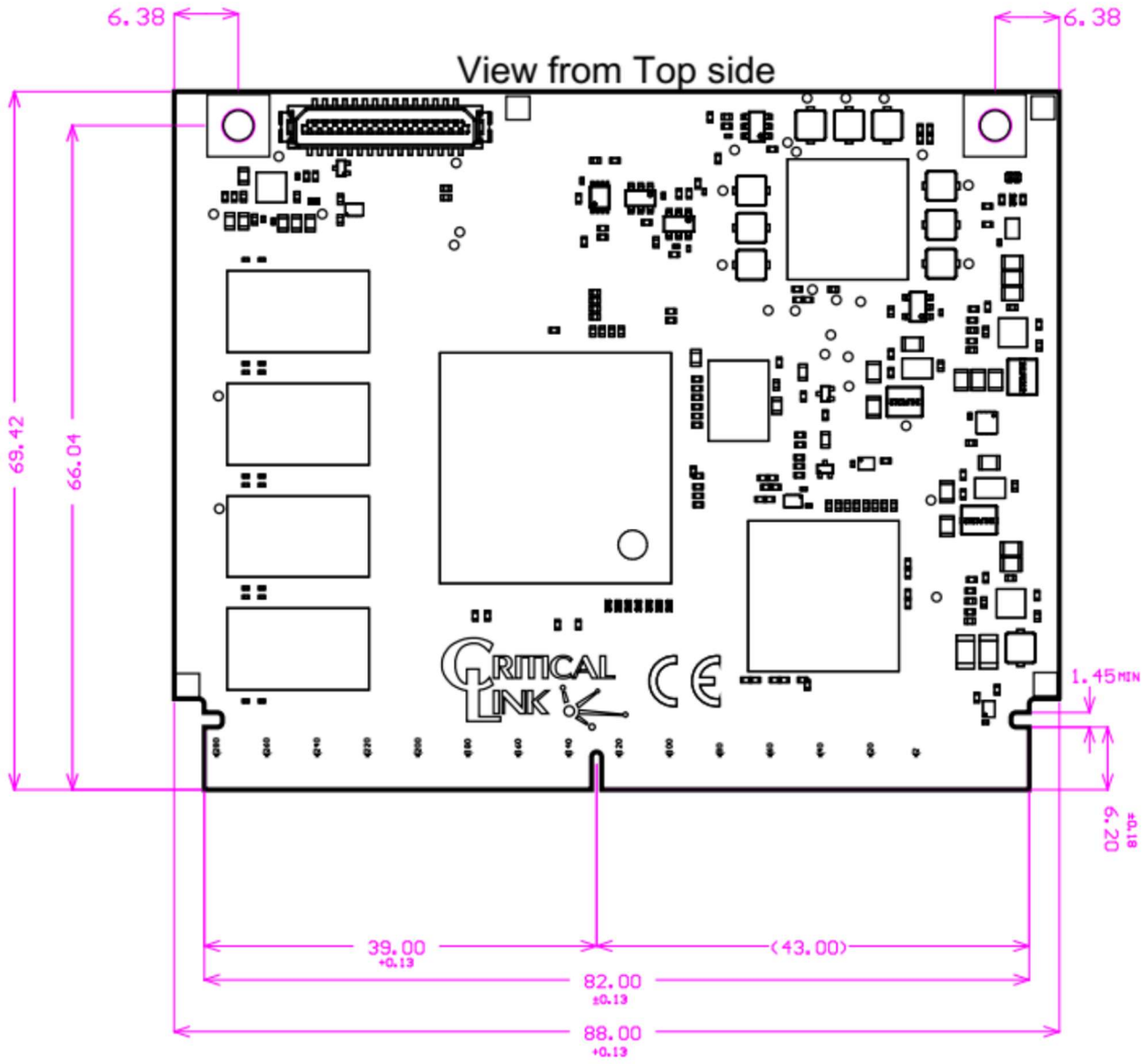


Figure 1: MitySOM-AM57F Mechanical Drawing

The mechanical outline of the MitySOM-AM57F is illustrated in Figure 2 and shows the location of the bottom side-mounted 100-pin fine-pitch plug-type connector (J3). The center of this 100-pin connector is the reference point for its placement.

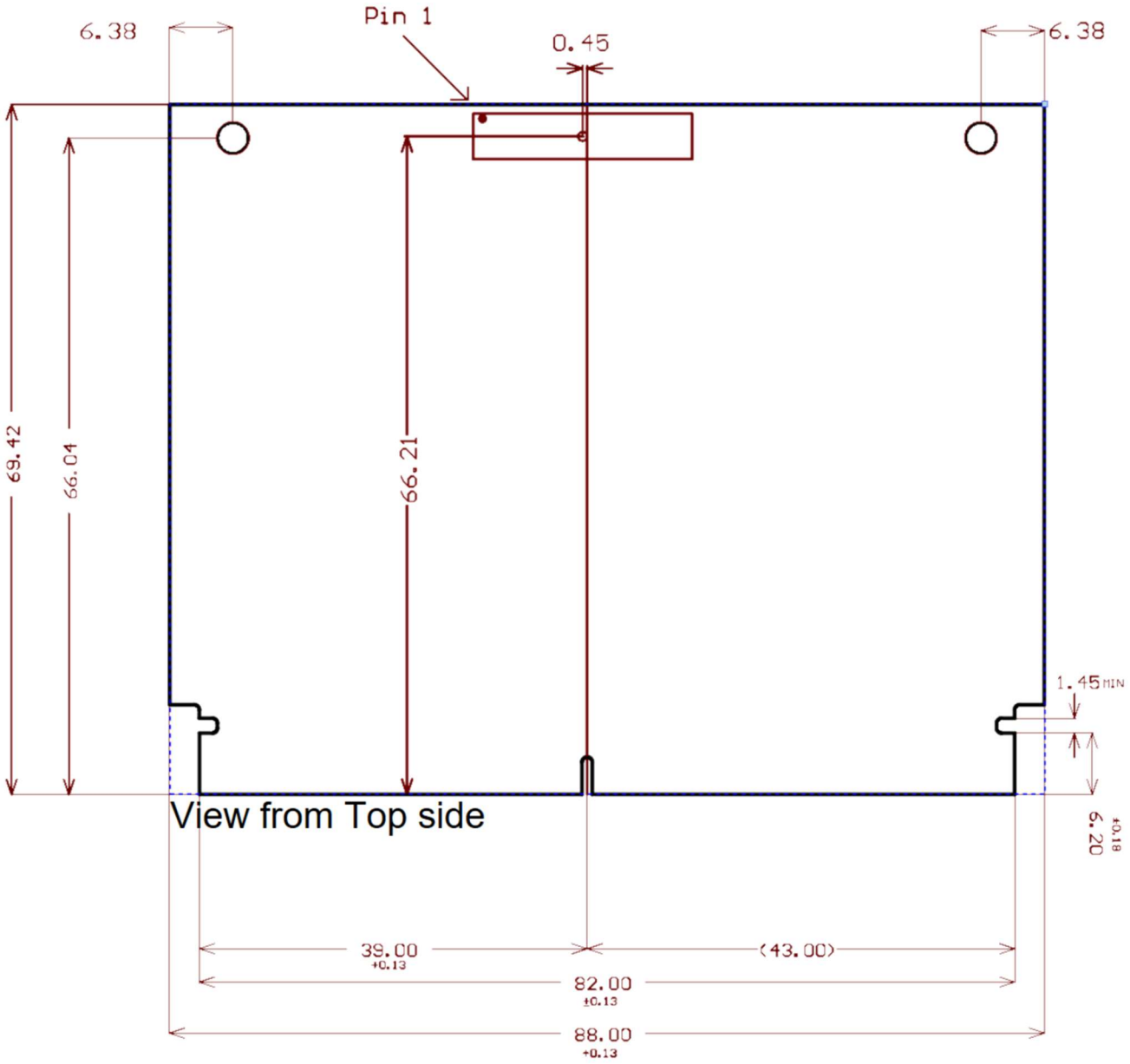


Figure 2: MitySOM-AM57F 100-pin bottom side connector location (J3)

1.6 Carrier Board: SOM Outline

Figure 3 specifies the recommended carrier board outline for placement of the mating 100-position receptacle and mounting holes for fasteners. Dimensions are referenced from the left alignment pin position of the MXM connector; this point is analogous to the SOM lower left inset corner shown in Figure 2. As in Figure 2, the center of the 100-position receptacle connector is the reference point for its placement.

Note that the vertical spacing between the reference (MXM alignment pin) and the center of the 100-position receptacle connector on the carrier board is slightly longer (by 0.3 mm) than the distance from SOM card edge to J3 connector shown in Figure 2. This accounts for tolerances in the MXM connector insertion depth to allow for proper alignment of when mating the 100-position connector set.

Fastener mounting holes on the carrier board should be sized for installation of 3 mm high threaded spacers or stand-offs. Recommended spacer part number: Penn Engineering SMTSOB-M3-3ET or equivalent. The 3 mm spacer height matches the board-to-board distance between the carrier board and SOM when the SOM is fully seated into the recommended JAE 314-pin MXM card edge connector and the HiRose 100-position connector set.

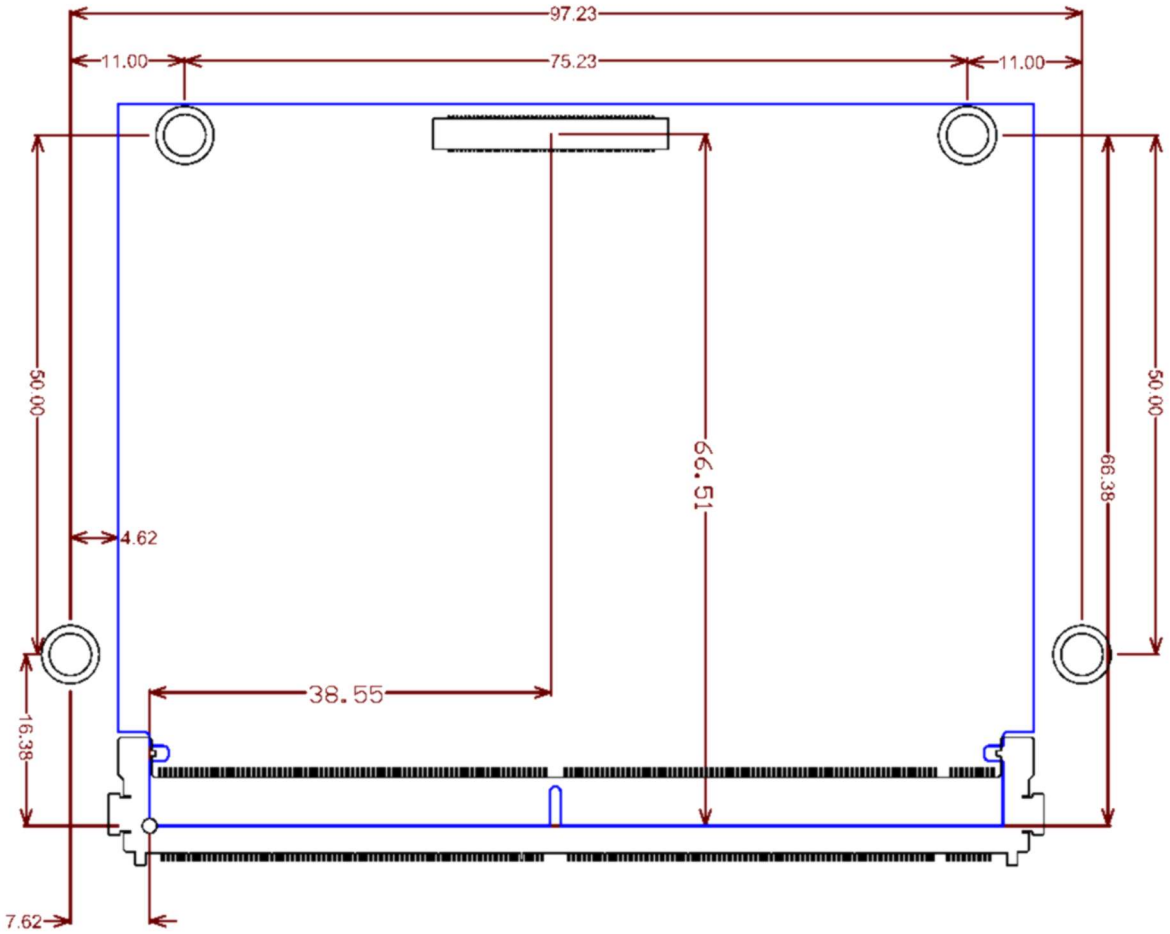


Figure 3: Recommended MitySOM-AM57F Carrier Card Outline with heat spreader mounting holes

If a heat spreader / heat sink solution is required, Critical Link recommends placing two additional mounting holes outside of the SOM outline area at the end near the MXM connector as shown. See Figures 4 and 5 for top and bottom renderings of Critical Link heat spreader 94-900813-3, designed for use with MitySOM-AM57F. Design files for this heat spreader are available from Critical Link on request.

See Section 5 of this document for additional Carrier Board Mechanical requirements.

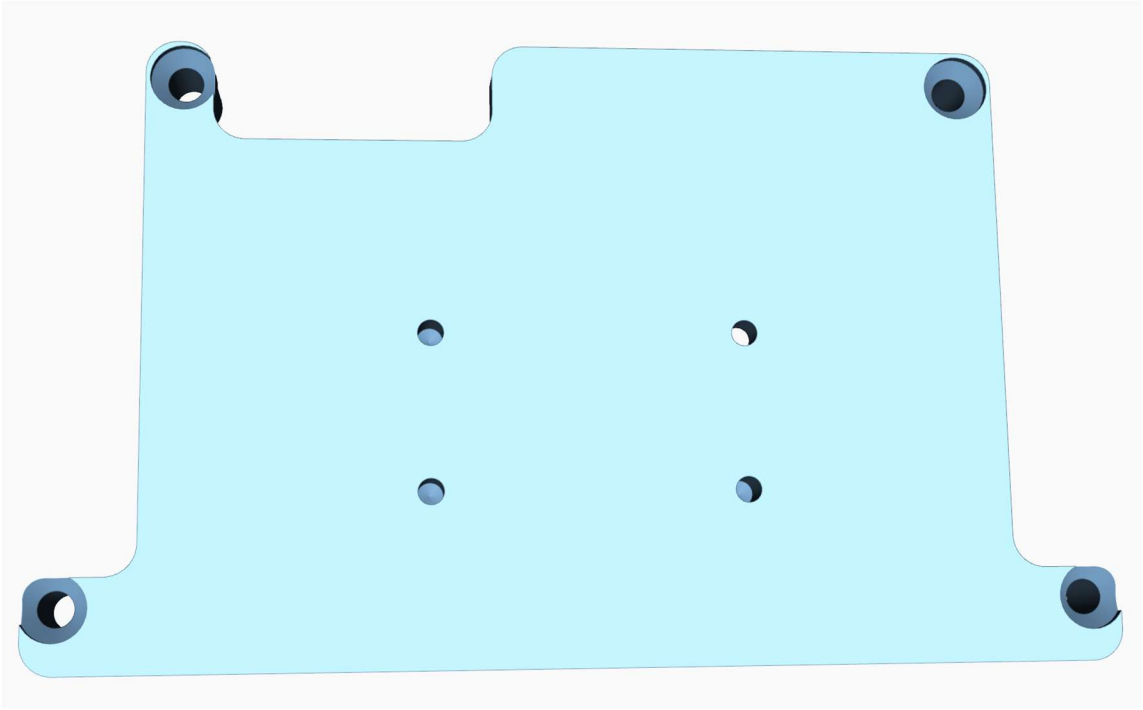


Figure 4: Heat Spreader 94-800913-3 Top Side View (faces away from SOM)

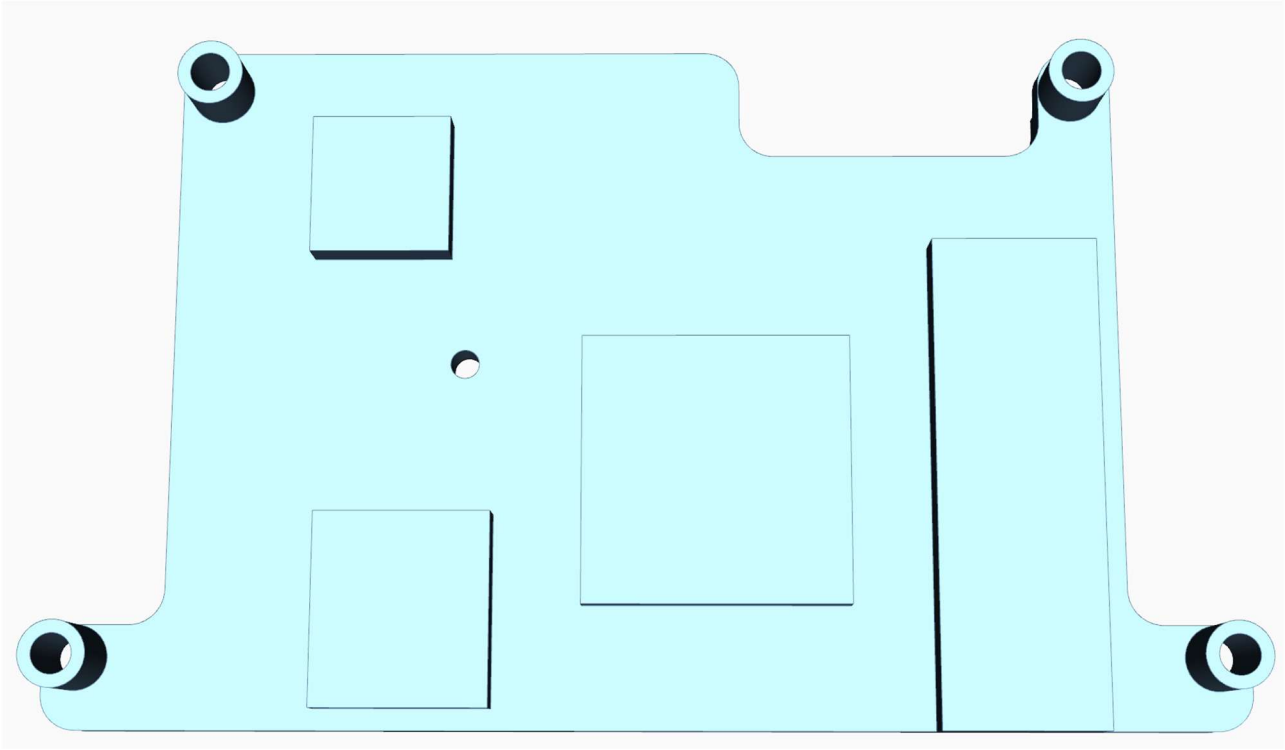


Figure 5: Heat Spreader 94-800913-3 Bottom Side View (faces SOM)

1.7 Reference Documents and Links

From Critical Link LLC:

MitySOM-AM57F Product Page:
https://www.criticallink.com/wp-content/uploads/MitySOM-AM57F-Data-Sheet.pdf

MitySOM-AM57x Support (Wiki):
https://support.criticallink.com/redmine/projects/mitysom_am57x/wiki

MitySOM-AM57F Data Sheet:
https://www.criticallink.com/wp-content/uploads/MitySOM-AM57F-Data-Sheet.pdf

MitySOM-AM57(F) Family Development Kit Product Page:
https://www.criticallink.com/product/mitysom-am57f-development-kit/

MitySOM-AM57x Carrier Schematic Checklist:
https://www.criticallink.com/wp-content/uploads/MitySOM-AM57x-Carrier-Schematic-Checklist.pdf

From Texas Instruments:

AM57x Sitara Processor Data Sheet:
TI document: SPRS953 rev. G revised Nov. 2019
https://www.ti.com/lit/gpn/am5728

AM57x Sitara Processor Technical Reference Manual:
TI document: SPRUHZ6 rev. L revised Aug. 2019
https://www.ti.com/lit/pdf/spruhz6

TPS659039 PMIC Product Page:
https://www.ti.com/product/TPS659039-Q1

From Xilinx/AMD:

Artix 7 FPGA Product Page:
https://www.xilinx.com/products/silicon-devices/fpga/artix-7.html

2 Connectors

The MitySOM-AM57 utilizes a dual connector set to physically interface with the end user's application board ("SOM Carrier" or "Carrier" board). Recommended sources for carrier board connectors are listed below in bold type.

- 314 position, MXM-style card edge connector provides primary access to SOM I/O:
  - SOM board: 'gold finger' pads spaced at 0.5 mm pitch on top and bottom sides along board edge, with pad gap for 'key' notch, no physical connector
  - **Carrier board card edge receptacle: JAE MM70-314B1-2-R300**
- 100-position (dual row, 50 positions per row), 0.4 mm pitch, 3.0 mm mating height, high speed-capable connector set provides access to additional SOM I/O:
  - SOM board plug-type connector: HiRose DF40C-100DP-0.4V(51)
  - **Carrier board receptacle-type connector: HiRose DF40HC(3.0)-100DS-0.4V(58)**

This connector set was chosen for its high density, compact size, ease of procurement, and low cost. With the MXM card edge connector, a physical socket component is only required on the carrier board. The connector set allows the MitySOM-AM57F module to lay flat, parallel to the carrier board surface with a 3.0 mm board-to-board distance. The mounting method is similar to installation of expansion memory and interface cards into compact equipment like laptop computers.

2.1 MXM Card-edge Compatibility

The MXM interface, consisting of a set of card edge-placed "gold finger" pads on top and bottom sides of a plug-in board, and a mating receptacle connector on a host or carrier board, was developed for PCI Express (PCIe) graphic adapter cards which install onto PC motherboards -- similar to memory expansion cards using an SO-DIMM card edge connector. **Please note that the MitySOM-AM57F is NOT electrically compatible with the PCIe socket standard**, and intermixing modules/sockets from the two standards would very likely cause permanent damage to one or both sides of the interface.

The MitySOM-AM57F shall only be installed into a board which is designed for compatibility with the SOM's pin-out and electrical characteristics.

Standard MXM connector footprints have the following characteristics which are not compatible with the MitySOM-AM57F pin-out and must be designed out of a Carrier Board PCB footprint:

Common PCB pad is shared for these pin groups:

- E1[1:9], E2[1:9], E3[2:10], E4[2:10],
- Pins [1, 3, 5, 7, 9]; pins [11, 13, 15, 17]; pins [279, 281]

PCB pads are not provided for these pin positions:

- E1-10, E2-10, E3-1 and E4-1 (from legacy 310-position connector design);

Total PCB pad calculation: 281 numbered pins **minus** 7 "key" deletions **plus** 40 E-pins **equals** 314 pads.

The carrier board footprint for the MXM-style card edge receptacle compatible with the MitySOM-AM57F must provide individual PCB pads for all 314 available connector pins. Developers of carrier board designs may request SOM and MXM connector footprints from Critical Link which are compatible with Altium Designer.

For backward compatibility with legacy 310-pin connectors, Critical Link recommends defining pins E1-10, E2-10, E3-1 and E4-1 as "no connects" in the carrier board design. These pins have no connections on the MitySOM-AM57F module.

2.2 MitySOM-AM57F Pin-out

Error! Reference source not found. and 2 contains a summary of the MitySOM-AM57F connector pin mapping which includes:

- Connector pin assignment
- Voltage domains
  - B15 and B34 indicate Artix 7 FPGA Bank 15 and 34 voltages; these are sourced from the Carrier board side of MXM card edge connector. Voltage range: +1.8 to +3.3 V.
- FPGA or AM57XX ball location for signals which directly connect with Carrier board
- Signal Types for each pin. Notes:
  - 'FPGA' signal types: the signal option name is of the form IO_<BANK>_<LVDSPAIR>_<N/P>
  - 'MFIO' (multi-function I/O) signal types: pin multiplexing (PINMUX) utility, sourced from Texas Instruments, must be utilized to configure valid combinations of peripheral devices. Not all combinations are supported. Except for MMC pins (+3.3 V), MFIO signals are +1.8 V logic.
  - 'PWR' and 'GND' types are reserved for power and ground
  - 'FF' (fixed function) and 'PMIO' (power management I/O) signal types have dedicated SOM functions and shall not be re-assigned. Most signals in these groups have interface-specific voltage characteristics.
  - Table 1 (card edge connector): Red shaded rows: reserved for other SOM functions; do not reassign
  - Table 2 (100-pin connector set): see legend for colored row restrictions
  - 'NC' and 'KEY' pin types have no connection on AM57F SOM.
- Signal Options for each pin: Refer to manufacturer documentation for descriptions of the various peripheral choices, pin functions and valid pin multiplex (PINMUX) settings. This documentation includes:
  - AM57x device datasheet
  - AM57x Technical Reference Manual
  - PINMUX utility

Table 1: MitySOM-AM57F Card-edge (J1) Pin-out

Pin	Type	FPGA Bank or Voltage Domain	FPGA ball	57xx ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10	Signal Option 11	Signal Option 12	Signal Option 13
1	FPGA	B15	B17	-	IO_15_L16_N												
2	FPGA	B15	C18	-	IO_15_L18_N												
3	FPGA	B15	C16	-	IO_15_L16_P												
4	FPGA	B15	D18	-	IO_15_L17_N												
5	FPGA	B15	D16	-	IO_15_L14_N		SRCC_N										
6	FPGA	B15	E17	-	IO_15_L17_P												
7	FPGA	B15	E16	-	IO_15_L14_P		SRCC_P										
8	GND	-	-	-	GND												
9	FPGA	B15	F15	-	IO_15_L21_N												
10	FPGA	B15	E18	-	IO_15_L24_N												
11	FPGA	B15	G15	-	IO_15_L21_P												
12	FPGA	B15	F17	-	IO_15_L24_P												
13	GND	-	-	-	GND												
14	FPGA	B15	F18	-	IO_15_L19_N												
15	FPGA	B15	G16	-	IO_15_L20_N												
16	FPGA	B15	G17	-	IO_15_L19_P												
17	FPGA	B15	H16	-	IO_15_L20_P												
18	FPGA	B15	H18	-	IO_15_L23_N												
19	FPGA	B15	C11	-	IO_15_L4_P												
20	FPGA	B15	H17	-	IO_15_L23_P												
21	FPGA	B15	B11	-	IO_15_L4_N												
22	FPGA	B15	C8	-	IO_15_L1_N	AD0N											
23	FPGA	B15	A13	-	IO_15_L8_P	AD10P											
24	FPGA	B15	D8	-	IO_15_L1_P	AD0P											
25	FPGA	B15	A14	-	IO_15_L8_N	AD10N											
26	GND	-	-	-	GND												

Pin	Type	FPGA Bank or Voltage Domain	FPGA ball	57xx ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10	Signal Option 11	Signal Option 12	Signal Option 13
27	FPGA	B15	A15	-	IO_15_L10_N	AD11N											
28	FPGA	B15	A12	-	IO_15_L7_N	AD2N											
29	FPGA	B15	B14	-	IO_15_L10_P	AD11P											
30	FPGA	B15	B12	-	IO_15_L7_P	AD2P											
31	GND	-	-	-	GND												
32	FPGA	B15	B15	-	IO_15_L9_N	AD3N											
33	FPGA	B15	C13	-	IO_15_L11_N		SRCC_N										
34	FPGA	B15	C14	-	IO_15_L9_P	AD3P											
35	FPGA	B15	D13	-	IO_15_L11_P		SRCC_P										
36	FPGA	B15	D14	-	IO_15_L12_N		MRCC_N										
37	FPGA	B15	C12	-	IO_15_L6_N												
38	FPGA	B15	E13	-	IO_15_L12_P		MRCC_P										
39	FPGA	B15	D11	-	IO_15_L6_P												
40	FPGA	B15	F14	-	IO_15_L22_N												
41	FPGA	B15	C9	-	IO_15_L2_N	AD8N											
42	FPGA	B15	G14	-	IO_15_L22_P												
43	FPGA	B15	D9	-	IO_15_L2_P	AD8P											
44	GND	-	-	-	GND												
45	FPGA	B15	D15	-	IO_15_L13_N		MRCC_N										
46	FPGA	B34	V8	-	IO_34_L24_P												
47	FPGA	B15	E15	-	IO_15_L13_P		MRCC_P										
48	FPGA	B34	V7	-	IO_34_L24_N												
49	GND	-	-	-	GND												
50	FPGA	B34	U7	-	IO_34_L23_P												
51	FPGA	B34	R3	-	IO_34_L14_P		SRCC_P										
52	FPGA	B34	V6	-	IO_34_L23_N												
53	FPGA	B34	T2	-	IO_34_L14_N		SRCC_N										
54	FPGA	B34	M6	-	IO_34_L8_P												

Pin	Type	FPGA Bank or Voltage Domain	FPGA ball	57xx ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10	Signal Option 11	Signal Option 12	Signal Option 13
55	FPGA	B34	R2	-	IO_34_L13_P		MRCC_P										
56	FPGA	B34	N6	-	IO_34_L8_N												
57	FPGA	B34	R1	-	IO_34_L13_N		MRCC_N										
58	FPGA	B34	P6	-	IO_34_L19_P												
59	FPGA	B34	J5	-	IO_34_L2_P												
60	FPGA	B34	P5	-	IO_34_L19_N												
61	FPGA	B34	J4	-	IO_34_L2_N												
62	GND	-	-	-	GND												
63	FPGA	B34	P1	-	IO_34_L9_N												
64	FPGA	B34	T7	-	IO_34_L22_N												
65	FPGA	B34	N1	-	IO_34_L9_P												
66	FPGA	B34	R7	-	IO_34_L22_P												
67	GND	-	-	-	GND												
68	FPGA	B34	T5	-	IO_34_L21_N												
69	FPGA	B34	K6	-	IO_34_L1_N												
70	FPGA	B34	R5	-	IO_34_L21_P												
71	FPGA	B34	K5	-	IO_34_L1_P												
72	FPGA	B34	U6	-	IO_34_L20_P												
73	FPGA	B34	L5	-	IO_34_L6_P												
74	FPGA	B34	U5	-	IO_34_L20_N												
75	FPGA	B34	M5	-	IO_34_L6_N												
76	FPGA	B34	V4	-	IO_34_L18_N												
77	FPGA	B34	M4	-	IO_34_L10_P												
78	FPGA	B34	U4	-	IO_34_L18_P												
79	FPGA	B34	N4	-	IO_34_L10_N												
80	GND	-	-	-	GND												
81	FPGA	B34	L4	-	IO_34_L5_P												
82	FPGA	B34	T4	-	IO_34_L17_P												

Pin	Type	FPGA Bank or Voltage Domain	FPGA ball	57xx ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10	Signal Option 11	Signal Option 12	Signal Option 13
83	FPGA	B34	L3	-	IO_34_L5_N												
84	FPGA	B34	T3	-	IO_34_L17_N												
85	GND	-	-	-	GND												
86	FPGA	B34	N3	-	IO_34_L11_P		SRCC_P										
87	FPGA	B34	M2	-	IO_34_L7_P												
88	FPGA	B34	N2	-	IO_34_L11_N		SRCC_N										
89	FPGA	B34	M1	-	IO_34_L7_N												
90	FPGA	B34	V3	-	IO_34_L16_P												
91	FPGA	B34	P4	-	IO_34_L12_P		MRCC_P										
92	FPGA	B34	V2	-	IO_34_L16_N												
93	FPGA	B34	P3	-	IO_34_L12_N		MRCC_N										
94	FPGA	B34	U2	-	IO_34_L15_P												
95	FPGA	B34	K2	-	IO_34_L3_P												
96	FPGA	B34	U1	-	IO_34_L15_N												
97	FPGA	B34	K1	-	IO_34_L3_N												
98	GND	-	-	-	GND												
99	FPGA	B34	K3	-	IO_34_L4_P												
100	MFIO	1.8	-	U6	RGMII0_TXD0	RMII0_RXD0	MII0_RXD0	VIN2A_D10	SPI4_CS0	UART4_RTSN	PR1_MII0_RXD0	PR2_PRU1_GPI10	PR2_PRU1_GPO10	GPIO5_25			
101	FPGA	B34	L2	-	IO_34_L4_N												
102	MFIO	1.8	-	V6	RGMII0_TXD1	RMII0_RXD1	MII0_RXD1	VIN2A_VSYNC0	VIN4B_VSYNC1	SPI4_D0	UART4_CTSN	PR1_MII0_RXD1	PR2_PRU1_GPI9	PR2_PRU1_GPO9	GPIO5_24		
103	GND		-	-	GND												
104	MFIO	1.8	-	U7	RGMII0_TXD2	RMII0_RXER	MII0_RXER	VIN2A_HSYNC0	VIN4B_HSYNC1	SPI4_D1	UART4_TXD	PR1_MII0_RXER	PR2_PRU1_GPI8	PR2_PRU1_GPO8	GPIO5_23		
105	MFIO	1.8	-	Y1	SPI3_D1	UART3_TXD	RMII1_RXER	MII0_RXCLK	VIN2A_D2	VIN4B_D2	SPI4_CS1	PR1_MII_MR0_CLK	PR2_PRU1_GPI4	PR2_PRU1_GPO4	GPIO5_19		
106	MFIO	1.8	-	V7	RGMII0_TXD3	RMII0_CRS	MII0_CRS	VIN2A_DE0	VIN4B_DE1	SPI4_SCLK	UART4_RXD	PR1_MII0_CRS	PR2_PRU1_GPI7	PR2_PRU1_GPO7	GPIO5_22		
107	MFIO	1.8	-	V2	SPI3_SCLK	UART3_RXD	RMII1_CRS	MII0_RXDV	VIN2A_D1	VIN4B_D1	PR1_MII0_RXDV	PR2_PRU1_GPI3	PR2_PRU1_GPO3	GPIO5_18			
108	MFIO	1.8	-	W9	RGMII0_TXC	UART3_CTSN	RMII1_RXD1	MII0_RXD3	VIN2A_D3	VIN4B_D3	SPI3_D0	SPI4_CS2	PR1_MII0_RXD3	PR2_PRU1_GPI5	PR2_PRU1_GPO5	GPIO5_20	
109	MFIO	3.3	-	Y9	MMC1_SDWP	UART6_TXD	I2C4_SCL	GPIO6_28									
110	MFIO	1.8	-	V9	RGMII0_TXCTL	UART3_RTSN	RMII1_RXD0	MII0_RXD2	VIN2A_D4	VIN4B_D4	SPI3_CS0	SPI4_CS3	PR1_MII0_RXD2	PR2_PRU1_GPI6	PR2_PRU1_GPO6	GPIO5_21	

Pin	Type	FPGA Bank or Voltage Domain	FPGA ball	57xx ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10	Signal Option 11	Signal Option 12	Signal Option 13
111	MFIO	1.8	-	C14	PR2_MDIO_MDCLK	MCASP1_ACLKX	VIN6A_FLD0	I2C3_SDA	PR2_PRU1_GPI7	PR2_PRU1_GPO7	GPIO7_31						
112	GND	-	-	-	GND												
113	MFIO	1.8	-	D14	PR2_MDIO_DATA	MCASP1_FSX	VIN6A_DE0	I2C3_SCL	GPIO7_30								
114	MFIO	1.8	-	V4	RGMII0_RXD3	RMII1_TXD0	MII0_TXD2	VIN2A_D7	VIN4B_D7	PR1_MII0_TXD2	PR2_PRU1_GPI13	PR2_PRU1_GPO13	GPIO5_28				
115	MFIO	1.8	-	G16	UART4_RXD	MCASP4_AXR0	SPI3_D0	UART8_CTSN	VOUT2_D18	VIN4A_D18	VIN5A_D13						
116	MFIO	1.8	-	V3	RGMII0_RXD2	RMII0_TXEN	MII0_TXEN	VIN2A_D8	PR1_MII0_TXEN	PR2_PRU1_GPI14	PR2_PRU1_GPO14	GPIO5_29					
117	MFIO	1.8	-	E12	MCASP4_AXR2	MCASP1_AXR4	VOUT2_D4	VIN4A_D4	GPIO5_6								
118	MFIO	1.8	-	Y2	RGMII0_RXD1	RMII0_TXD1	MII0_TXD1	VIN2A_D9	PR1_MII0_TXD1	PR2_PRU1_GPI15	PR2_PRU1_GPO15	GPIO5_30					
119	MFIO	1.8	-	D17	MCASP4_AXR1	SPI3_CS0	UART8_RTSN	UART4_TXD	VOUT2_D19	VIN4A_D19	VIN5A_D12	PR2_PRU1_GPI0	PR2_PRU1_GPO0				
120	MFIO	1.8	-	W2	RGMII0_RXD0	RMII0_TXD0	MII0_TXD0	VIN2A_FLD0	VIN4B_FLD1	PR1_MII0_TXD0	PR2_PRU1_GPI16	PR2_PRU1_GPO16	GPIO5_31				
121	MFIO	1.8	-	C18	MCASP4_ACLKX	MCASP4_ACLKR	SPI3_SCLK	UART8_RXD	I2C4_SDA	VOUT2_D16	VIN4A_D16	VIN5A_D15					
122	MFIO	1.8	-	V5	RGMII0_RXCTL	RMII1_TXD1	MII0_TXD3	VIN2A_D6	VIN4B_D6	PR1_MII0_TXD3	PR2_PRU1_GPI12	PR2_PRU1_GPO12	GPIO5_27				
123	MFIO	1.8	-	A21	MCASP4_FSX	MCASP4_FSR	SPI3_D1	UART8_TXD	I2C4_SCL	VOUT2_D17	VIN4A_D17	VIN5A_D14					
124	MFIO	1.8	-	U5	RGMII0_RXC	RMII1_TXEN	MII0_TXCLK	VIN2A_D5	VIN4B_D5	PR1_MII_MT0_CLK	PR2_PRU1_GPI11	PR2_PRU1_GPO11	GPIO5_26				
125	FPGA	1.8	F12	-	FPGA_DONE												
126	KEY	-	-	-													
127	KEY	-	-	-													
128	KEY	-	-	-													
129	KEY	-	-	-													
130	KEY	-	-	-													
131	KEY	-	-	-													
132	KEY	-	-	-													
133	GND	-	-	-	GND												
134	GND	-	-	-	GND												
135	MFIO	1.8	-	J7	MMC2_CLK	GPMC_A23	GPMC_A17	VIN4A_FLD0	VIN3B_D4	GPIO2_13							
136	MFIO	1.8	-	D6	RGMII1_TXD0	VIN2A_D17	VIN2B_D6	VOUT2_D6	VIN3A_D9	MII1_TXD2	EHRPWM3A	PR1_MII1_RXD2	PR1_PRU1_GPI14	PR1_PRU1_GPO14	GPIO4_25		
137	MFIO	1.8	-	H6	MMC2_CMD	GPMC_CS1	GPMC_A22	VIN4A_DE0	VIN3B_VSYNC1	GPIO2_18							
138	MFIO	1.8	-	B2	RGMII1_TXD1	VIN2A_D16	VIN2B_D7	VOUT2_D7	VIN3A_D8	MII1_TXD1	EQEP3_STROBE	PR1_MII1_RXD3	PR1_PRU1_GPI13	PR1_PRU1_GPO13	GPIO4_24		

Pin	Type	FPGA Bank or Voltage Domain	FPGA ball	57xx ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10	Signal Option 11	Signal Option 12	Signal Option 13
139	MFIO	1.8	-	J4	MMC2_DAT0	GPMC_A24	GPMC_A18	VIN3B_D5	GPIO2_14								
140	MFIO	1.8	-	C4	RGMII1_TXD2	VIN2A_D15	VOUT2_D8	MII1_TXD0	EQEP3_INDEX	PR1_MII1_RXDV	PR1_PRU1_GPI12	PR1_PRU1_GPO12	GPIO4_16				
141	MFIO	1.8	-	J6	MMC2_DAT1	GPMC_A25	GPMC_A19	VIN3B_D6	GPIO2_15								
142	MFIO	1.8	-	C3	RGMII1_TXD3	VIN2A_D14	VOUT2_D9	MII1_TXCLK	EQEP3B_IN	PR1_MII_MR1_CLK	PR1_PRU1_GPI11	PR1_PRU1_GPO11	GPIO4_15				
143	MFIO	1.8	-	H4	MMC2_DAT2	GPMC_A26	GPMC_A20	VIN3B_D7	GPIO2_16								
144	MFIO	1.8	-	D5	RGMII1_TXC	VIN2A_D12	VOUT2_D11	MII1_RXCLK	KBD_COL8	ECAP2_IN_PWM2_OUT	PR1_MII1_TXD1	PR1_PRU1_GPI9	PR1_PRU1_GPO9	GPIO4_13			
145	MFIO	1.8	-	H5	MMC2_DAT3	GPMC_A27	GPMC_A21	VIN3B_HSYNC1	GPIO2_17								
146	MFIO	1.8	-	C2	RGMII1_TXCTL	VIN2A_D13	VOUT2_D10	MII1_RXDV	KBD_ROW8	EQEP3A_IN	PR1_MII1_TXD0	PR1_PRU1_GPI10	PR1_PRU1_GPO10	GPIO4_14			
147	MFIO	1.8	-	K7	GPMC_A19	MMC2_DAT4	GPMC_A13	VIN4A_D12	VIN3B_D0	GPIO2_9							
148	GND	-	-	-	GND												
149	MFIO	1.8	-	M7	GPMC_A20	MMC2_DAT5	GPMC_A14	VIN4A_D13	VIN3B_D1	GPIO2_10							
150	MFIO	1.8	-	B3	RGMII1_RXD3	VIN2A_D20	VIN2B_D3	VOUT2_D3	VIN3A_DE0	VIN3A_D12	MII1_RXER	ECAP3_IN_PWM3_OUT	PR1_MII1_RXER	PR1_PRU1_GPI17	PR1_PRU1_GPO17	GPIO4_28	
151	MFIO	1.8	-	J5	GPMC_A21	MMC2_DAT6	GPMC_A15	VIN4A_D14	VIN3B_D2	GPIO2_11							
152	MFIO	1.8	-	B4	RGMII1_RXD2	VIN2A_D21	VIN2B_D2	VOUT2_D2	VIN3A_FLD0	VIN3A_D13	MII1_COL	PR1_MII1_RXLINK	PR1_PRU1_GPI18	PR1_PRU1_GPO18	GPIO4_29		
153	MFIO	1.8	-	K6	GPMC_A22	MMC2_DAT7	GPMC_A16	VIN4A_D15	VIN3B_D3	GPIO2_12							
154	MFIO	1.8	-	B5	RGMII1_RXD1	VIN2A_D22	VIN2B_D1	VOUT2_D1	VIN3A_HSYNC0	VIN3A_D14	MII1_CRS	PR1_MII1_COL	PR1_PRU1_GPI19	PR1_PRU1_GPO19	GPIO4_30		
155	GND	-	-	-	GND												
156	MFIO	1.8	-	A4	RGMII1_RXD0	VIN2A_D23	VIN2B_D0	VOUT2_D0	VIN3A_VSYNC0	VIN3A_D15	MII1_TXEN	PR1_MII1_CRS	PR1_PRU1_GPI20	PR1_PRU1_GPO20	GPIO4_31		
157	MFIO	1.8	-	U3	GPIO5_17	RMII_MHZ_50_CLK	VIN2A_D11	PR2_PRU1_GPI2	PR2_PRU1_GPO2								
158	MFIO	1.8	-	A3	RGMII1_RXCTL	VIN2A_D19	VIN2B_D4	VOUT2_D4	VIN3A_D11	MII1_TXER	EHRPWM3_TRIPZ_IN	PR1_MII1_RXD0	PR1_PRU1_GPI16	PR1_PRU1_GPO16	GPIO4_27		
159	MFIO	1.8	-	U4	MDIO_D	UART3_CTSN	MII0_TXER	VIN2A_D0	VIN4B_D0	PR1_MII0_RXLINK	PR2_PRU1_GPI1	PR2_PRU1_GPO1	GPIO5_16				
160	MFIO	1.8	-	C5	RGMII1_RXC	VIN2A_D18	VIN2B_D5	VOUT2_D5	VIN3A_D10	MII1_TXD3	EHRPWM3B	PR1_MII1_RXD1	PR1_PRU1_GPI15	PR1_PRU1_GPO15	GPIO4_26		
161	MFIO	1.8	-	V1	MDIO_MCLK	UART3_RTSN	MII0_COL	VIN2A_CLK0	VIN4B_CLK1	PR1_MII0_COL	PR2_PRU1_GPI0	PR2_PRU1_GPO0	GPIO5_15				
162	GND	-	-	-	GND												
163	MFIO	3.3	-	W7	MMC1_SDCD	UART6_RXD	I2C4_SDA	GPIO6_27									
164	MFIO	1.8	-	AC9	PR2_MII_MR1_CLK	MMC3_DAT2	SPI3_CS0	UART5_CTSN	VIN2B_D3	VIN5A_D3	EQEP3_INDEX	PR2_PRU0_GPI6	PR2_PRU0_GPO6	GPIO7_1			
165	MFIO	3.3	-	W6	MMC1_CLK	GPIO6_21											

Pin	Type	FPGA Bank or Voltage Domain	FPGA ball	57xx ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10	Signal Option 11	Signal Option 12	Signal Option 13
166	MFIO	1.8	-	AC3	PR2_MII1_RXDV	MMC3_DAT3	SPI3_CS1	UART5_RTSN	VIN2B_D2	VIN5A_D2	EQEP3_STROBE	PR2_PRU0_GPI7	PR2_PRU0_GPO7	GPIO7_2			
167	MFIO	3.3	-	Y6	MMC1_CMD	GPIO6_22											
168	MFIO	1.8	-	E17	PR2_MII1_CRS	XREF_CLK1	MCASP2_AXR9	MCASP1_AXR5	MCASP2_AHCLKX	MCASP6_AHCLKX	VIN6A_CLK0	TIMER14	PR2_PRU1_GPI6	PR2_PRU1_GPO6	GPIO6_18		
169	MFIO	3.3	-	Y3	MMC1_DAT3	GPIO6_26											
170	MFIO	1.8	-	B19	PR2_MII1_RXER	MCASP3_AXR0	MCASP2_AXR14	UART7_CTSN	UART5_RXD	VIN6A_D1	PR2_PRU0_GPI14	PR2_PRU0_GPO14					
171	MFIO	3.3	-	AA5	MMC1_DAT2	GPIO6_25											
172	MFIO	1.8	-	D18	PR2_MII1_COL	XREF_CLK0	MCASP2_AXR8	MCASP1_AXR4	MCASP1_AHCLKX	MCASP5_AHCLKX	VIN6A_D0	HDQ0	CLKOUT2	TIMER13	PR2_PRU1_GPI5	PR2_PRU1_GPO5	GPIO6_17
173	MFIO	3.3	-	Y4	MMC1_DAT1	GPIO6_24											
174	MFIO	1.8	-	AB5	PR2_MII1_RXD0	MMC3_DAT7	SPI4_CS0	UART10_RTSN	VIN2B_CLK1	VIN5A_VSYNC0	ECAP3_IN_PWM3_OUT	PR2_PRU0_GPI11	PR2_PRU0_GPO11	GPIO1_25			
175	MFIO	3.3	-	AA6	MMC1_DAT0	GPIO6_23											
176	MFIO	1.8	-	AB8	PR2_MII1_RXD1	MMC3_DAT6	SPI4_D0	UART10_CTSN	VIN2B_DE1	VIN5A_HSYNC0	EHRPWM3_TRIPZ_IN	PR2_PRU0_GPI10	PR2_PRU0_GPO10	GPIO1_24			
177	GND	-	-	-	GND												
178	MFIO	1.8	-	AD6	PR2_MII1_RXD2	MMC3_DAT5	SPI4_D1	UART10_TXD	VIN2B_D0	VIN5A_D0	EHRPWM3B	PR2_PRU0_GPI9	PR2_PRU0_GPO9	GPIO1_23			
179	MFIO	1.8	-	P4	GPMC_A12	VIN4A_CLK0	GPMC_A0	VIN4B_FLD1	TIMER8	SPI4_CS1	DMA_EVT1	GPIO2_2					
180	MFIO	1.8	-	AC8	PR2_MII1_RXD3	MMC3_DAT4	SPI4_SCLK	UART10_RXD	VIN2B_D1	VIN5A_D1	EHRPWM3A	PR2_PRU0_GPI8	PR2_PRU0_GPO8	GPIO1_22			
181	MFIO	1.8	-	N9	GPMC_A10	VIN3A_DE0	VOUT3_DE	VIN4B_CLK1	TIMER10	SPI4_D0	GPIO2_0						
182	MFIO	1.8	-	C17	PR2_MII1_RXLINK	MCASP3_AXR1	MCASP2_AXR15	UART7_RTSN	UART5_TXD	VIN6A_D0	VIN5A_FLD0	PR2_PRU0_GPI15	PR2_PRU0_GPO15				
183	MFIO	1.8	-	P9	GPMC_A11	VIN3A_FLD0	VOUT3_FLD	VIN4A_FLD0	VIN4B_DE1	TIMER9	SPI4_CS0	GPIO2_1					
184	MFIO	1.8	-	AC5	PR2_MII_MT1_CLK	GPIO6_10	MDIO_MCLK	I2C3_SDA	VIN2B_HSYNC1	VIN5A_CLK0	EHRPWM2A	PR2_PRU0_GPI0	PR2_PRU0_GPO0	GPIO6_10			
185	MFIO	1.8	-	P6	I2C5_SCL	GPMC_A4	QSPI1_CS3	VIN3A_D20	VOUT3_D20	VIN4A_D4	VIN4B_D4	UART6_RXD	GPIO1_26				
186	MFIO	1.8	-	AB4	PR2_MII1_TXEN	GPIO6_11	MDIO_D	I2C3_SCL	VIN2B_VSYNC1	VIN5A_DE0	EHRPWM2B	PR2_PRU0_GPI1	PR2_PRU0_GPO1	GPIO6_11			
187	MFIO	1.8	-	P5	GPMC_A7	VIN3A_D23	VOUT3_D23	VIN4A_D7	VIN4B_D7	UART8_TXD	UART6_RTSN	GPIO1_29					
188	MFIO	1.8	-	AC6	PR2_MII1_TXD0	MMC3_DAT1	SPI3_D0	UART5_TXD	VIN2B_D4	VIN5A_D4	EQEP3B_IN	PR2_PRU0_GPI5	PR2_PRU0_GPO5	GPIO7_0			
189	MFIO	1.8	-	G20	DCAN1_TX	UART8_RXD	MMC2_SDCD	HDMI1_HPD	GPIO1_14								
190	MFIO	1.8	-	AC7	PR2_MII1_TXD1	MMC3_DAT0	SPI3_D1	UART5_RXD	VIN2B_D5	VIN5A_D5	EQEP3A_IN	PR2_PRU0_GPI4	PR2_PRU0_GPO4	GPIO6_31			
191	MFIO	1.8	-	G19	DCAN1_RX	UART8_TXD	MMC2_SDWP	SATA1_LED	HDMI1_CEC	GPIO1_15							
192	MFIO	1.8	-	AC4	PR2_MII1_TXD2	MMC3_CMD	SPI3_SCLK	VIN2B_D6	VIN5A_D6	ECAP2_IN_PWM2_OUT	PR2_PRU0_GPI3	PR2_PRU0_GPO3	GPIO6_30				

Pin	Type	FPGA Bank or Voltage Domain	FPGA ball	57xx ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10	Signal Option 11	Signal Option 12	Signal Option 13
193	MFIO	1.8	-	F20	UART10_TXD	GPIO6_15	MCASP1_AXR9	DCAN2_RX	VOUT2_VSYNC	VIN4A_VSYNC0	I2C3_SCL	TIMER2	GPIO6_15				
194	MFIO	1.8	-	AD4	PR2_MII1_TXD3	MMC3_CLK	VIN2B_D7	VIN5A_D7	EHRPWM2_TRIPZ_IN	PR2_PRU0_GPI2	PR2_PRU0_GPO2	GPIO6_29					
195	MFIO	1.8	-	G17	SPI2_D0	UART3_CTSN	UART5_RXD	GPIO7_16									
196	GND	-	-	-	GND												
197	MFIO	1.8	-	E15	MCASP2_ACLKR	MCASP8_AXR2	VOUT2_D8	VIN4A_D8									
198	MFIO	1.8	-	A13	PR2_MII_MR0_CLK	MCASP1_AXR13	MCASP7_AXR1	VIN6A_D10	TIMER10	PR2_PRU1_GPI15	PR2_PRU1_GPO15	GPIO6_4					
199	MFIO	1.8	-	F16	SPI1_D1	GPIO7_8											
200	MFIO	1.8	-	G14	PR2_MII0_RXDV	MCASP1_AXR14	MCASP7_ACLKX	MCASP7_ACLKR	VIN6A_D9	TIMER11	PR2_PRU1_GPI16	PR2_PRU1_GPO16	GPIO6_5				
201	MFIO	1.8	-	C26	UART1_TXD	MMC4_SDWP	GPIO7_23										
202	MFIO	1.8	-	B18	PR2_MII0_CRS	MCASP3_ACLKX	MCASP3_ACLKR	MCASP2_AXR12	UART7_RXD	VIN6A_D3	PR2_PRU0_GPI12	PR2_PRU0_GPO12	GPIO5_13				
203	MFIO	1.8	-	T6	GPMC_A2	VIN3A_D18	VOUT3_D18	VIN4A_D2	VIN4B_D2	UART7_RXD	UART5_CTSN	GPIO7_5					
204	MFIO	1.8	-	G12	PR2_MII0_RXER	MCASP1_AXR0	UART6_RXD	VIN6A_VSYNC0	I2C5_SDA	PR2_PRU1_GPI8	PR2_PRU1_GPO8	GPIO5_2					
205	MFIO	1.8	-	T7	GPMC_A3	QSPI1_CS2	VIN3A_D19	VOUT3_D19	VIN4A_D3	VIN4B_D3	UART7_TXD	UART5_RTSN	GPIO7_6				
206	MFIO	1.8	-	F15	PR2_MII0_COL	MCASP3_FSX	MCASP3_FSR	MCASP2_AXR13	UART7_TXD	VIN6A_D2	PR2_PRU0_GPI13	PR2_PRU0_GPO13	GPIO5_14				
207	MFIO	1.8	-	R9	I2C5_SDA	GPMC_A5	VIN3A_D21	VOUT3_D21	VIN4A_D5	VIN4B_D5	UART6_TXD	GPIO1_27					
208	MFIO	1.8	-	C15	PR2_MII0_RXD0	MCASP2_AXR2	MCASP3_AXR2	VIN6A_D5	PR2_PRU0_GPI16	PR2_PRU0_GPO16	GPIO6_8						
209	MFIO	1.8	-	T9	I2C4_SDA	GPMC_A1	VIN3A_D17	VOUT3_D17	VIN4A_D1	VIN4B_D1	UART5_TXD	GPIO7_4					
210	MFIO	1.8	-	A18	PR2_MII0_RXD1	MCASP2_FSX	VIN6A_D6	PR2_PRU0_GPI19	PR2_PRU0_GPO19								
211	MFIO	1.8	-	G13	MCASP1_AXR2	MCASP6_AXR2	UART6_CTSN	VOUT2_D2	VIN4A_D2	GPIO5_4							
212	MFIO	1.8	-	A19	PR2_MII0_RXD2	MCASP2_ACLKX	VIN6A_D7	PR2_PRU0_GPI18	PR2_PRU0_GPO18								
213	MFIO	1.8	-	J11	MCASP1_AXR3	MCASP6_AXR3	UART6_RTSN	VOUT2_D3	VIN4A_D3	GPIO5_5							
214	MFIO	1.8	-	F14	PR2_MII0_RXD3	MCASP1_AXR15	MCASP7_FSX	MCASP7_FSR	VIN6A_D8	TIMER12	PR2_PRU0_GPI20	PR2_PRU0_GPO20	GPIO6_6				
215	MFIO	1.8	-	N7	GPMC_A8	VIN3A_HSYNC0	VOUT3_HSYNC	VIN4B_HSYNC1	TIMER12	SPI4_SCLK	GPIO1_30						
216	MFIO	1.8	-	A16	PR2_MII0_RXLINK	MCASP2_AXR3	MCASP3_AXR3	VIN6A_D4	PR2_PRU0_GPI17	PR2_PRU0_GPO17	GPIO6_9						
217	MFIO	1.8	-	R4	GPMC_A9	VIN3A_VSYNC0	VOUT3_VSYNC	VIN4B_VSYNC1	TIMER11	SPI4_D1	GPIO1_31						
218	MFIO	1.8	-	F12	PR2_MII_MT0_CLK	MCASP1_AXR1	UART6_TXD	VIN6A_HSYNC0	I2C5_SCL	PR2_PRU1_GPI9	PR2_PRU1_GPO9	GPIO5_3					
219	MFIO	1.8	-	R5	GPMC_A6	VIN3A_D22	VOUT3_D22	VIN4A_D6	VIN4B_D6	UART8_RXD	UART6_CTSN	GPIO1_28					
220	MFIO	1.8	-	B12	PR2_MII0_TXEN	MCASP1_AXR8	MCASP6_AXR0	SPI3_SCLK	VIN6A_D15	TIMER5	PR2_PRU1_GPI10	PR2_PRU1_GPO10	GPIO5_10				

Pin	Type	FPGA Bank or Voltage Domain	FPGA ball	57xx ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10	Signal Option 11	Signal Option 12	Signal Option 13
221	MFIO	1.8	-	R6	I2C4_SCL	GPMC_A0	VIN3A_D16	VOUT3_D16	VIN4A_D0	VIN4B_D0	UART5_RXD	GPIO7_3					
222	MFIO	1.8	-	E14	PR2_MII0_TXD0	MCASP1_AXR12	MCASP7_AXR0	SPI3_CS1	VIN6A_D11	TIMER9	PR2_PRU1_GPI14	PR2_PRU1_GPO14	GPIO4_18				
223	MFIO	1.8	-	F21	GPIO6_16	MCASP1_AXR10	VOUT2_FLD	VIN4A_FLD0	CLKOUT1	TIMER3	GPIO6_16						
224	MFIO	1.8	-	A12	PR2_MII0_TXD1	MCASP1_AXR11	MCASP6_FSX	MCASP6_FSR	SPI3_CS0	VIN6A_D12	TIMER8	PR2_PRU1_GPI13	PR2_PRU1_GPO13	GPIO4_17			
225	GND	-	-	-	GND												
226	MFIO	1.8	-	B13	PR2_MII0_TXD2	MCASP1_AXR10	MCASP6_ACLKX	MCASP6_ACLKR	SPI3_D0	VIN6A_D13	TIMER7	PR2_PRU1_GPI12	PR2_PRU1_GPO12	GPIO5_12			
227	MFIO	1.8	-	E21	UART10_RXD	GPIO6_14	MCASP1_AXR8	DCAN2_TX	VOUT2_HSYNC	VIN4A_HSYNC0	I2C3_SDA	TIMER1	GPIO6_14				
228	MFIO	1.8	-	A11	PR2_MII0_TXD3	MCASP1_AXR9	MCASP6_AXR1	SPI3_D1	VIN6A_D14	TIMER6	PR2_PRU1_GPI11	PR2_PRU1_GPO11	GPIO5_11				
229	MFIO	1.8	-	B22	SPI2_D1	UART3_TXD	GPIO7_15										
230	GND	-	-	-	GND												
231	MFIO	1.8	-	D28	UART2_RXD	UART3_CTSN	UART3_RCTX	MMC4_DAT0	UART1_DCDN	GPIO7_26							
232	MFIO	1.8	-	AC10	USB2_DRVVBUS	TIMER15	GPIO6_13										
233	MFIO	1.8	-	D26	UART2_TXD	UART3_RTSN	UART3_SD	MMC4_DAT1	UART1_DSRN	GPIO7_27							
234	MFIO	1.8	-	E25	GPIO7_24 (USB2_ID)	UART1_CTSN	UART9_RXD	MMC4_CLK									
235	MFIO	1.8	-	G2	VIN2A_DE0	VIN2A_FLD0	VIN2B_FLD1	VIN2B_DE1	VOUT2_DE	EMU6	KBD_ROW1	EQEP1B_IN	PR1_EDIO_DATA_IN1	PR1_EDIO_DATA_OUT1	GPIO3_29		
236	FF	-	-	AE11	USB2_DP												
237	MFIO	1.8	-	G1	GPIO3_31	VIN2A_HSYNC0	VIN2B_HSYNC1	VOUT2_HSYNC	EMU8	UART9_RXD	SPI4_SCLK	KBD_ROW2	EQEP1_STROBE	PR1_UART0_CTS_N	PR1_EDIO_D_IN3	PR1_EDIO_D_OUT3	
238	FF	-	-	AF11	USB2_DM												
239	MFIO	1.8	-	F3	VIN2A_D1	VOUT2_D22	EMU11	UART9_RTSN	SPI4_CS0	KBD_ROW5	EHRPWM1_TRIPZ_IN	PR1_UART0_TXD	PR1_EDIO_DATA_IN6	PR1_EDIO_DATA_OUT6	GPIO4_2		
240	FF	5V – 20V	-	-	USB_VBUS (1)												
241	MFIO	1.8	-	F2	VIN2A_D0	VOUT2_D23	EMU10	UART9_CTSN	SPI4_D0	KBD_ROW4	EHRPWM1B	PR1_UART0_RXD	PR1_EDIO_DATA_IN5	PR1_EDIO_DATA_OUT5	GPIO4_1		
242	GND	-	-	-	GND												
243	MFIO	1.8	-	E1	VIN2A_CLK0	VOUT2_FLD	EMU5	KBD_ROW0	EQEP1A_IN	PR1_EDIO_DATA_IN0	PR1_EDIO_DATA_OUT0	GPIO3_28					
244	MFIO	1.8	-	J14	GPIO5_1	MCASP1_FSR	MCASP7_AXR3	VOUT2_D1	VIN4A_D1	I2C4_SCL							
245	MFIO	1.8	-	E2	VIN2A_D3	VOUT2_D20	EMU13	UART10_TXD	KBD_COL0	EHRPWM1_SYNCI	PR1_EDC_LATCH0_IN	PR1_PRU1_GPI0	PR1_PRU1_GPO0	GPIO4_4			
246	MFIO	1.8	-	F13	GPIO5_7	MCASP1_AXR5	MCASP4_AXR3	VOUT2_D5	VIN4A_D5								

Pin	Type	FPGA Bank or Voltage Domain	FPGA ball	57xx ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10	Signal Option 11	Signal Option 12	Signal Option 13
247	MFIO	1.8	-	D1	VIN2A_D2	VOUT2_D21	EMU12	UART10_RXD	KBD_ROW6	ECAP1_IN_PWM1_OUT	PR1_ECAP0ECAP_CAPIN_APWM_O	PR1_EDIO_DATA_IN7	PR1_EDIO_DATA_OUT7	GPIO4_3			
248	MFIO	1.8	-	C12	GPIO5_8	MCASP1_AXR6	MCASP5_AXR2	VOUT2_D6	VIN4A_D6								
249	MFIO	1.8	-	D2	UART10_CTSN	VIN2A_D4	VOUT2_D19	EMU14	KBD_COL1	EHRPWM1_SYNCO	PR1_EDC_SYNC0_OUT	PR1_PRU1_GPI1	PR1_PRU1_GPO1	GPIO4_5			
250	MFIO	1.8	-	H7	GPIO3_30	VIN2A_FLD0	VIN2B_CLK1	VOUT2_CLK	EMU7	EQEP1_INDEX	PR1_EDIO_DATA_IN2	PR1_EDIO_DATA_OUT2					
251	MFIO	1.8	-	C1	VIN2A_D6	VOUT2_D17	EMU16	MII1_RXD1	KBD_COL3	EQEP2B_IN	PR1_MII_MT1_CLK	PR1_PRU1_GPI3	PR1_PRU1_GPO3	GPIO4_7			
252	MFIO	1.8	-	B14	GPIO5_0	MCASP1_ACLKR	MCASP7_AXR2	VOUT2_D0	VIN4A_D0	I2C4_SDA							
253	MFIO	1.8	-	D3	VIN2A_D10	MDIO_MCLK	VOUT2_D13	KBD_COL7	EHRPWM2B	PR1_MDIO_MDCLK	PR1_PRU1_GPI7	PR1_PRU1_GPO7	GPIO4_11				
254	MFIO	1.8	-	A15	MCASP2_AXR1	VOUT2_D11	VIN4A_D11										
255	MFIO	1.8	-	E4	VIN2A_D7	VOUT2_D16	EMU17	MII1_RXD2	KBD_COL4	EQEP2_INDEX	PR1_MII1_TXEN	PR1_PRU1_GPI4	PR1_PRU1_GPO4	GPIO4_8			
256	MFIO	1.8	-	B15	MCASP2_AXR0	VOUT2_D10	VIN4A_D10										
257	MFIO	1.8	-	F4	UART10_RTSN	VIN2A_D5	VOUT2_D18	EMU15	KBD_COL2	EQEP2A_IN	PR1_EDIO_SOF	PR1_PRU1_GPI2	PR1_PRU1_GPO2	GPIO4_6			
258	MFIO	1.8	-	D15	MCASP8_AXR0	MCASP2_AXR4	VOUT2_D12	VIN4A_D12	GPIO1_4								
259	MFIO	1.8	-	F5	VIN2A_D8	VOUT2_D15	EMU18	MII1_RXD3	KBD_COL5	EQEP2_STROBE	PR1_MII1_TXD3	PR1_PRU1_GPI5	PR1_PRU1_GPO5	GPIO4_9			
260	MFIO	1.8	-	C23	MCASP8_AHCLKX	XREF_CLK3	MCASP2_AXR11	MCASP1_AXR7	MCASP4_AHCLKX	VOUT2_DE	HDQ0	VIN4A_DE0	CLKOUT3	TIMER16	GPIO6_20		
261	MFIO	1.8	-	E6	VIN2A_D9	VOUT2_D14	EMU19	MII1_RXD0	KBD_COL6	EHRPWM2A	PR1_MII1_TXD2	PR1_PRU1_GPI6	PR1_PRU1_GPO6	GPIO4_10			
262	MFIO	1.8	-	B16	MCASP8_AXR1	MCASP2_AXR5	VOUT2_D13	VIN4A_D13	GPIO6_7								
263	MFIO	1.8	-	F6	VIN2A_D11	MDIO_D	VOUT2_D12	KBD_ROW7	EHRPWM2_TRIPZONE_INPUT	PR1_MDIO_DATA	PR1_PRU1_GPI8	PR1_PRU1_GPO8	GPIO4_12				
264	MFIO	1.8	-	A17	MCASP8_FSX	MCASP2_AXR7	MCASP8_FSR	VOUT2_D15	VIN4A_D15	GPIO1_5							
265	MFIO	1.8	-	G6	VIN2A_VSYNC0	VIN2B_VSYNC1	VOUT2_VSYNC	EMU9	UART9_TXD	SPI4_D1	KBD_ROW3	EHRPWM1A	PR1_UART0_RTS_N	PR1_EDIO_DATA_IN4	PR1_EDIO_DATA_OUT4	GPIO4_0	
266	MFIO	1.8	-	B17	MCASP8_ACLKX	MCASP2_AXR6	MCASP8_ACLKR	VOUT2_D14	VIN4A_D14	GPIO2_29							
267	MFIO	1.8	-	B10	VOUT1_DE	VIN4A_DE0	VIN3A_DE0	SPI3_D1	GPIO4_20								
268	MFIO	1.8	-	A20	MCASP2_FSR	MCASP8_AXR3	VOUT2_D9	VIN4A_D9									
269	MFIO	1.8	-	D11	VOUT1_CLK	VIN4A_FLD0	VIN3A_FLD0	SPI3_CS0	GPIO4_19								
270	MFIO	1.8	-	B24	SPI2_CS0	UART3_RTSN	UART5_TXD	GPIO7_17									
271	MFIO	1.8	-	E11	VOUT1_VSYNC	VIN4A_VSYNC0	VIN3A_VSYNC0	SPI3_SCLK	PR2_PRU1_GPI17	PR2_PRU1_GPO17	GPIO4_23						
272	MFIO	1.8	-	A25	SPI1_SCLK	GPIO7_7											

Pin	Type	FPGA Bank or Voltage Domain	FPGA ball	57xx ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10	Signal Option 11	Signal Option 12	Signal Option 13
273	MFIO	1.8	-	D12	MCASP1_AXR7	MCASP5_AXR3	VOUT2_D7	VIN4A_D7	TIMER4	GPIO5_9							
274	MFIO	1.8	-	B25	SPI1_D0	GPIO7_9											
275	MFIO	1.8	-	B27	UART1_RXD	MMC4_SDCD	GPIO7_22										
276	MFIO	1.8	-	A26	SPI2_SCLK	UART3_RXD	GPIO7_14										
277	GND	-	-	-	GND												
278	MFIO	1.8	-	B26	XREF_CLK2	MCASP2_AXR10	MCASP1_AXR6	MCASP3_AHCLKX	MCASP7_AHCLKX	VOUT2_CLK	VIN4A_CLK0	TIMER15	GPIO6_19				
279	MFIO	1.8	-	D27	UART3_RXD	UART2_CTSN	MMC4_DAT2	UART10_RXD	UART1_DTRN	GPIO1_16							
280	GND	-	-	-	GND												
281	MFIO	1.8	-	C28	UART3_TXD	UART2_RTSN	UART3_IRTX	MMC4_DAT3	UART10_TXD	UART1_RIN	GPIO1_17						
E1-1	PWR	5.0	-	-	VDD_5V0												
E1-2	PWR	5.0	-	-	VDD_5V0												
E1-3	PWR	5.0	-	-	VDD_5V0												
E1-4	PWR	5.0	-	-	VDD_5V0												
E1-5	GND	-	-	-	GND												
E1-6	GND	-	-	-	GND												
E1-7	GND	-	-	-	GND												
E1-8	PWR	B34	-	-	VCCIO_34_EXT												
E1-9	PWR	B34	-	-	VCCIO_34_EXT												
E1-10	NC	-	-	-													
E2-1	PWR	5.0	-	-	VDD_5V0												
E2-2	PWR	5.0	-	-	VDD_5V0												
E2-3	PWR	5.0	-	-	VDD_5V0												
E2-4	PWR	5.0	-	-	VDD_5V0												
E2-5	GND	-	-	-	GND												
E2-6	GND	-	-	-	GND												
E2-7	PWR	B15	-	-	VCCO_15_EXT												
E2-8	PWR	B15	-	-	VCCO_15_EXT												
E2-9	OUT	1.8	-	-	VDD_1V8F												

Pin	Type	FPGA Bank or Voltage Domain	FPGA ball	57xx ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10	Signal Option 11	Signal Option 12	Signal Option 13
E2-10	NC	-	-	-													
E3-1	NC	-	-	-													
E3-2	OUT	3.3	-	-	PS_3V3												
E3-3	OUT	3.3	-	-	PS_3V3												
E3-4	PMIO	5.0	-	-	AUXFAN_EN												
E3-5	FF	3.3	-	-	PB_RESETn												
E3-6	PMIO	1.8	-	-	PMIC_POWERGOOD												
E3-7	PMIO	1.8	-	-	PMIC_POWERHOLD												
E3-8	GND	-	-	-	GND												
E3-9	FPGA	B15	A17	-	IO_15_L15_N												
E3-10	FPGA	B15	B16	-	IO_15_L15_P												
E4-1	NC	-	-	-													
E4-2	OUT	-	-	-	VDD_1V8F												
E4-3	OUT	-	-	-	VDD_1V8F												
E4-4	MFIO	1.8	-	-	WAKEUP1	DCAN2_RX	GPIO1_1										
E4-5	GND	-	-	-	GND												
E4-6	FPGA	B15	A9	-	IO_15_L3_N	AD1N											
E4-7	FPGA	B15	B9	-	IO_15_L3_P	AD1P											
E4-8	FPGA	B15	A10	-	IO_15_L5_N	AD9P											
E4-9	FPGA	B15	B10	-	IO_15_L5_P	AD9N											
E4-10	FPGA	B15	C17	-	IO_15_L18_P												

Note 1: See section 3.7 USB Interface for details about USB_VBUS

The J3 HiRose 100-position connector contains additional AM57xx and peripheral pin access. FPGA I/O are not routed to this connector.

Orange shaded rows: for HDMI; some pins may be reassigned if HDMI is not used

Yellow shaded rows: for USB 3.0 / USB-C; some pins may be reassigned if USB 3.0 / USB-C is not used

Red shaded rows: reserved for other SOM functions; do not reassign

Table 2: MitySOM-AM57F Secondary (HiRose) Connector (J3) Pin-out

Pin	Type	FPGA Bank or Voltage Domain	FPGA Ball	AM57xx Ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10
1	GND	-	-	-	GND									
2	GND	-	-	-	GND									
3	FF	1.8 (Vhdmi)	-	AH19	HDMI1_DATA2Y									
4	MFIO	1.8	-	B21	HDMI1_HPD	SPI1_CS2	UART4_RXD	MMC3_SDCD	SPI2_CS2	DCAN2_TX	MDIO_MCLK	GPIO7_12		
5	FF	1.8 (Vhdmi)	-	AG19	HDMI1_DATA2X									
6	MFIO	1.8	-	B20	HDMI1_CEC	SPI1_CS3	UART4_TXD	MMC3_SDWP	SPI2_CS3	DCAN2_RX	MDIO_D	GPIO7_13		
7	GND	-	-	-	GND									
8	MFIO	1.8	-	C25	HDMI1_DDC_SCL	I2C2_SDA								
9	FF	1.8 (Vhdmi)	-	AH18	HDMI1_DATA1Y									
10	MFIO	1.8	-	F17	HDMI1_DDC_SDA	I2C2_SCL								
11	FF	1.8 (Vhdmi)	-	AG18	HDMI1_DATA1X									
12	MFIO	1.8	-	A24	SPI1_CS0	GPIO7_10								
13	GND	-	-	-	GND									
14	MFIO	1.8	-	AG8	VIN1A_CLK0	VOUT3_D16	VOUT3_FLD	GPIO2_30						
15	FF	1.8 (Vhdmi)	-	AH17	HDMI1_DATA0Y									

Pin	Type	FPGA Bank or Voltage Domain	FPGA Ball	AM57xx Ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10
16	GND	-	-	-	GND									
17	FF	1.8 (Vhdmi)	-	AG17	HDMI1_DATA0X									
18	MFIO	1.8	-	AA3	MCASP5_ACLKX	MCASP5_ACLKR	SPI4_SCLK	UART9_RXD	I2C5_SDA	VOUT2_D20	VIN4A_D20	VIN5A_D11	PR2_PRU1_GPI1	PR2_PRU1_GPO1
19	GND	-	-	-	GND									
20	MFIO	1.8	-	AB9	MCASP5_FSX	MCASP5_FSR	SPI4_D1	UART9_TXD	I2C5_SCL	VOUT2_D21	VIN4A_D21	VIN5A_D10	PR2_PRU1_GPI2	PR2_PRU1_GPO2
21	FF	1.8 (Vhdmi)	-	AH16	HDMI1_CLOCKY									
22	MFIO	1.8	-	AD9	GPIO3_0	VIN1A_DE0	VIN1B_HSYNC1	VOUT3_D17	VOUT3_DE	UART7_RXD	TIMER16	SPI3_SCLK	KBD_ROW0	EQEP1A_IN
23	FF	1.8 (Vhdmi)	-	AG16	HDMI1_CLOCKX									
24	MFIO	1.8	-	AD8	GPIO3_5	VIN1A_D1	VOUT3_D6	VOUT3_D22	UART8_TXD	EHRPWM1B				
25	GND	-	-	-	GND									
26	MFIO	1.8	-	AF8	GPIO3_3	VIN1A_VSYNC0	VIN1B_DE1	VOUT3_VSYNC	UART7_RTSN	TIMER13	SPI3_CS0	EQEP1_STROBE		
27	FF	1.8 (Vusb1)	-	AC11	USB1_SSRX_N (2)									
28	MFIO	1.8	-	AE8	GPIO3_4	VIN1A_D0	VOUT3_D7	VOUT3_D23	UART8_RXD	EHRPWM1A				
29	FF	1.8 (Vusb1)	-	AD11	USB1_SSRX_P (2)									
30	MFIO	1.8	-	AF6	VIN1A_D13	VIN1B_D2	VOUT3_D10	GPMC_A25	KBD_ROW7	PR1_EDC_SYNC1_OUT	PR1_PRU0_GPI10	PR1_PRU0_GPO10	GPIO3_17	
31	GND	-	-	-	GND									
32	MFIO	1.8	-	AE6	VIN1A_D21	VIN1B_D2	VOUT3_D2	VIN3A_D5	KBD_COL6	PR1_EDIO_DATA_IN5	PR1_EDIO_DATA_OUT5	PR1_PRU0_GPI18	PR1_PRU0_GPO18	GPIO3_25
33	FF	1.8 (Vusb1)	-	AF12	USB1_SSTX_N									

Pin	Type	FPGA Bank or Voltage Domain	FPGA Ball	AM57xx Ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10
34	MFIO	1.8	-	AA4	MCASP5_AXR1	SPI4_CS0	UART9_RTSN	UART3_TXD	VOUT2_D23	VIN4A_D23	VIN5A_D8	PR2_MDIO_DATA	PR2_PRU1_GPI4	PR2_PRU1_GPO4
35	FF	1.8 (Vusb1)	-	AE12	USB1_SSTX_P									
36	MFIO	1.8	-	AB3	MCASP5_AXR0	SPI4_D0	UART9_CTSN	UART3_RXD	VOUT2_D22	VIN4A_D22	VIN5A_D9	PR2_MDIO_MDCLK	PR2_PRU1_GPI3	PR2_PRU1_GPO3
37	GND	-	-	-	GND									
38	MFIO	1.8	-	AE9	GPIO3_2	VIN1A_HSYNC0	VIN1B_FLD1	VOUT3_HSYNC	UART7_CTSN	TIMER14	SPI3_D0	EQEP1_INDEX		
39	MFIO	1.8	-	C27	GPIO7_25 (USB1_ID)	UART1_RTSN	UART9_TXD	MMC4_CMD						
40	MFIO	1.8	-	AF9	GPIO3_1	VIN1A_FLD0	VIN1B_VSYNC1	VOUT3_CLK	UART7_TXD	TIMER15	SPI3_D1	KBD_ROW1	EQEP1B_IN	
41	MFIO	1.8	-	AB10	USB1_DRVVBUS	TIMER16	GPIO6_12							
42	MFIO	1.8	-	AG7	GPIO3_6	VIN1A_D2	VOUT3_D5	VOUT3_D21	UART8_CTSN	EHRPWM1_TRIPZONE_INPUT				
43	FF	1.8 (Vusb3)	-	AC12	USB1_DM									
44	MFIO	1.8	-	AH7	VIN1B_CLK1	VIN3A_CLK0	GPIO2_31 (USB1_ID_INT_N)							
45	FF	1.8 (Vusb3)-	-	AD12	USB1_DP									
46	MFIO	1.8	-	AG6	VIN1A_D6	VOUT3_D1	VOUT3_D17	EQEP2A_IN	PR1_PRU0_GPI3	PR1_PRU0_GPO3	GPIO3_10 (USB1_VCONN_FAULT_N)			
47	GND	-	-	-	GND									
48	MFIO	1.8	-	AH6	VIN1A_D3	VOUT3_D4	VOUT3_D20	UART8_RTSN	ECAP1_IN_PWM1_OUT	PR1_PRU0_GPI0	PR1_PRU0_GPO0	GPIO3_7 (USB1_DIR)		
49	FF	1.8 (Vsata)	-	AH10	SATA1_TXP0									
50	MFIO	1.8	-	AG5	VIN1A_D11	VIN1B_D4	VOUT3_D12	GPMC_A23	KBD_ROW5	PR1_EDC_LATCH1_IN	PR1_PRU0_GPI8	PR1_PRU0_GPO8	GPIO3_15 (USB1_MUXENABLE)	

Pin	Type	FPGA Bank or Voltage Domain	FPGA Ball	AM57xx Ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10
51	FF	1.8 (Vsata)	-	AG10	SATA1_TXN0									
52	MFIO	1.8	-	AH5	VIN1A_D5	VOUT3_D2	VOUT3_D18	EHRPWM1_SYNCO	PR1_PRU0_GPI2	PR1_PRU0_GPO2	GPIO3_9 (USB1_OVERCURRENT_N)			
53	GND	-	-	-	GND									
54	MFIO	1.8	-	AG4	VIN1A_D8	VIN1B_D7	VOUT3_D15	KBD_ROW2	EQEP2_INDEX	PR1_PRU0_GPI5	PR1_PRU0_GPO5	GPIO3_12		
55	FF	1.8 (Vsata)	-	AH9	SATA1_RXN0									
56	MFIO	1.8	-	AH4	VIN1A_D7	VOUT3_D0	VOUT3_D16	EQEP2B_IN	PR1_PRU0_GPI4	PR1_PRU0_GPO4	GPIO3_11			
57	FF	1.8 (Vsata)	-	AG9	SATA1_RXP0									
58	MFIO	1.8	-	AG3	VIN1A_D10	VIN1B_D5	VOUT3_D13	KBD_ROW4	PR1_EDC_LATCH0_IN	PR1_PRU0_GPI7	PR1_PRU0_GPO7	GPIO3_14		
59	GND	-	-	-	GND									
60	MFIO	1.8	-	AH3	VIN1A_D4	VOUT3_D3	VOUT3_D19	EHRPWM1_SYNCI	PR1_PRU0_GPI1	PR1_PRU0_GPO1	GPIO3_8			
61	MFIO	1.8	-	AE3	VIN1A_D17	VIN1B_D6	VOUT3_D6	VIN3A_D1	KBD_COL2	PR1_EDIO_DATA_IN1	PR1_EDIO_DATA_OUT1	PR1_PRU0_GPI14	PR1_PRU0_GPO14	GPIO3_21
62	MFIO	1.8	-	AG2	VIN1A_D9	VIN1B_D6	VOUT3_D14	KBD_ROW3	EQEP2_STROBE	PR1_PRU0_GPI6	PR1_PRU0_GPO6	GPIO3_13		
63	MFIO	1.8	-	AF4	VIN1A_D15	VIN1B_D0	VOUT3_D8	GPMC_A27	KBD_COL0	PR1_EDIO_SOF	PR1_PRU0_GPI12	PR1_PRU0_GPO12	GPIO3_19	
64	MFIO	1.8	-	AF2	VIN1A_D12	VIN1B_D3	VOUT3_D11	GPMC_A24	KBD_ROW6	PR1_EDC_SYNC0_OUT	PR1_PRU0_GPI9	PR1_PRU0_GPO9	GPIO3_16	
65	MFIO	1.8	-	AE5	VIN1A_D18	VIN1B_D5	VOUT3_D5	VIN3A_D2	KBD_COL3	PR1_EDIO_DATA_IN2	PR1_EDIO_DATA_OUT2	PR1_PRU0_GPI15	PR1_PRU0_GPO15	GPIO3_22
66	MFIO	1.8	-	AF1	VIN1A_D16	VIN1B_D7	VOUT3_D7	VIN3A_D0	KBD_COL1	PR1_EDIO_DATA_IN0	PR1_EDIO_DATA_OUT0	PR1_PRU0_GPI13	PR1_PRU0_GPO13	GPIO3_20
67	MFIO	1.8	-	AD3	VIN1A_D23	VIN1B_D0	VOUT3_D0	VIN3A_D7	KBD_COL8	PR1_EDIO_DATA_IN7	PR1_EDIO_DATA_OUT7	PR1_PRU0_GPI20	PR1_PRU0_GPO20	GPIO3_27

Pin	Type	FPGA Bank or Voltage Domain	FPGA Ball	AM57xx Ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10
68	MFIO	1.8	-	AF3	VIN1A_D14	VIN1B_D1	VOUT3_D9	GPMC_A26	KBD_ROW8	PR1_EDIO_LATCH_IN	PR1_PRU0_GPI11	PR1_PRU0_GPO11	GPIO3_18	
69	GND	-	-	-	GND									
70	MFIO	1.8	-	AE2	VIN1A_D20	VIN1B_D3	VOUT3_D3	VIN3A_D4	KBD_COL5	PR1_EDIO_DATA_IN4	PR1_EDIO_DATA_OUT4	PR1_PRU0_GPI17	PR1_PRU0_GPO17	GPIO3_24
71	XCVR	1.2 (Vmgt)	D6	-	FPGA_GXB_REF_CLK_P									
72	MFIO	1.8	-	AD2	VIN1A_D22	VIN1B_D1	VOUT3_D1	VIN3A_D6	KBD_COL7	PR1_EDIO_DATA_IN6	PR1_EDIO_DATA_OUT6	PR1_PRU0_GPI19	PR1_PRU0_GPO19	GPIO3_26
73	XCVR	1.2 (Vmgt)	D5	-	FPGA_GXB_REF_CLK_N									
74	FF	1.8	-	-	AM57_BOOT_MODE									
75	GND	-	-	-	GND									
76	FF	1.8	-	K14	OTP_VPP[1]									
77	XCVR	1.2 (Vmgt)	C3	-	FPGA_GXB_TX0_N									
78	GND	-	-	-	GND									
79	XCVR	1.2 (Vmgt)	C4	-	FPGA_GXB_TX0_P									
80	FF		-	AC1	RESERVED (NC)									
81	GND	-	-	-	GND									
82	FF		-	AC2	RESERVED (NC)									
83	XCVR	1.2 (Vmgt)	D1	-	FPGA_GXB_RX0_N									
84	FF		-	AB1	RESERVED (NC)									
85	XCVR	1.2 (Vmgt)	D2	-	FPGA_GXB_RX0_P									
86	FF		-	AB2	RESERVED (NC)									

Pin	Type	FPGA Bank or Voltage Domain	FPGA Ball	AM57xx Ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10
87	GND	-	-	-	GND									
88	FF		-	AA1	RESERVED (NC)									
89	XCVR	1.2 (Vmgt)	G3	-	FPGA_GXB_TX1_N									
90	FF		-	AA2	RESERVED (NC)									
91	XCVR	1.2 (Vmgt)	G4	-	FPGA_GXB_TX1_P									
92	GND	-	-	-	GND									
93	GND	-	-	-	GND									
94	FF	1.8 (Vadc)	M9	-	FPGA_DXN									
95	XCVR	1.2 (Vmgt)	B1	-	FPGA_GXB_RX1_N									
96	FF	1.8 (Vadc)	M10	-	FPGA_DXP									
97	XCVR	1.2 (Vmgt)	B2	-	FPGA_GXB_RX1_P									
98	FF	1.8 (Vadc)	L9	-	FPGA_VN_0									
99	GND	-	-	-	GND									
100	FF	1.8 (Vadc)	K10	-	FPGA_VP_0									

Note 1: The OTP_VPP signal, K14, should typically be left floating. Please contact your Critical Link representative for further questions about the usage of this pin.

Note 2: 0.1uF AC coupling caps are installed on the SOM for USB1_SSTX_P/N nets, do not add them to the baseboard.

3 Electrical Requirements

The following sections describe the various electrical requirements for the MitySOM-AM57F modules.

3.1 Power Interface

Input Power Specification

The MitySOM-AM57F is powered from the Carrier Board via the card-edge connector as described below :

- +5.0 VDC supply connects to the VDD_5V0 pins. This is used by on-board devices to supply the AM57xx SoC, FPGA core, DDR3 memory and other peripherals except for FPGA Bank I/O.
- FPGA Bank I/O voltages connect to the VCCO_34_EXT and VCCO_15_EXT pins. These bank voltages may be sourced from active sources on the carrier board (+1.8, +2.5 or +3.3 VDC), or the carrier board may passively route SOM-sourced power output(s) from VDD_1V8F pins (+1.8 VDC) and/or PS_3V3 pins (+3.3 VDC) to the VCCO_15_EXT and VCCO_34_EXT pins.

See Figure 6 for a simplified SOM Power Section Diagram.

See Table 3 for SOM input power specifications.

Table 1: Module Voltage and Current Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_5	Voltage supply, 5 volt input		4.5	5	5.25	Volts
I_5	Quiescent Current draw, 5 volt input			TBS[1,2]	TBS[1,2]	mA
$I_{5\text{-max}}$	Max current draw, positive 5 volt input			TBS[1,2]	TBS[1,2]	mA
$I_{o3.3}$	Max output current 3.3V output				1000	mA
$I_{o1.8}$	Max output current 1.8V output				1500	mA
	1. Power utilization of the MitySOM-AM57F is heavily dependent on end-user application. Major factors include: ARM CPU PLL configuration, DSP Utilization FPGA utilization, and external DDR3L RAM utilization. 2. For power utilization information please visit our Redmine Wiki pages on support.criticallink.com					

SOM Power Control

The MitySOM-AM57F leverages a TPS659037 power management IC (PMIC) for managing the power sources, sequencing and voltage monitoring for the AM57xx SoC device. Additional supply management is performed on the SOM to support proper power sequencing of the on-board DDR3 and FPGA core voltages.

The PMIC will automatically power on when power is applied and the U-boot initialization code will set DEV_CTRL.DEV_ON to 1 to keep the PMIC powered on. This allows the software to power off the SOM at the end of power down by setting this bit to 0. The PMIC_POWERHOLD signal (PMIC ball G9), which is available external to the module at J1 Pin E3-7 should be left floating in this scenario.

Alternatively, control of the module's power state, on/off, from the baseboard can be accomplished with the PMIC_POWERHOLD signal, PMIC ball G9, which is available external to the module at J1 Pin E3-7. Driving this signal high allows the module to stay powered on; driving this signal low will cause the PMIC to begin its sequential power down process. **Note:** driving PMIC_POWERHOLD low does not command the operating system (OS) to power down safely; the OS must be commanded to shut down separately. The shutdown process should complete before driving PMIC_POWERHOLD signal low.

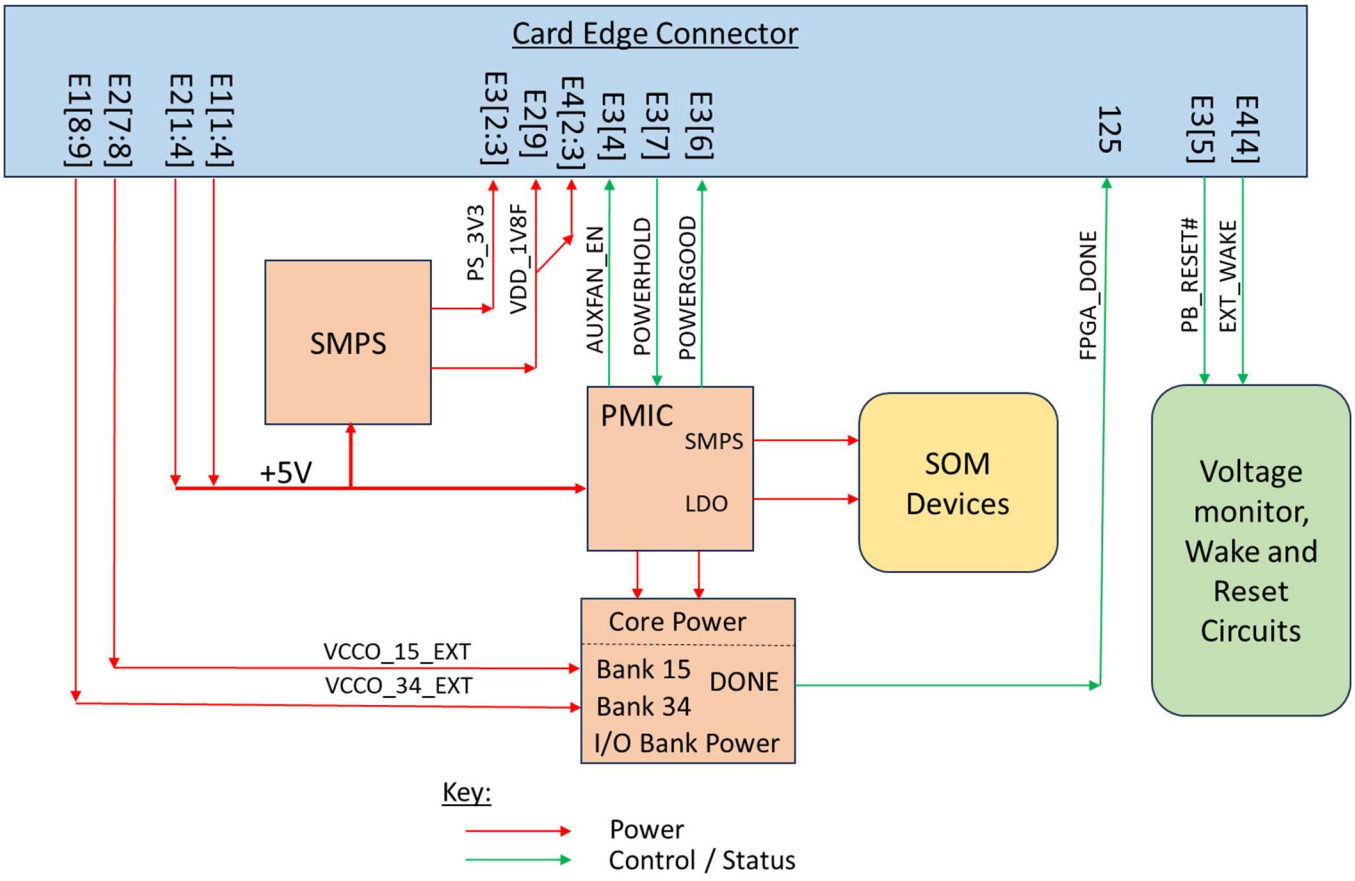


Figure 6: MitySOM-AM57F Power Section

SOM non-PMIC on-board supplies and SYS_POWERGOOD status follow the sequence shown in Figure 7:

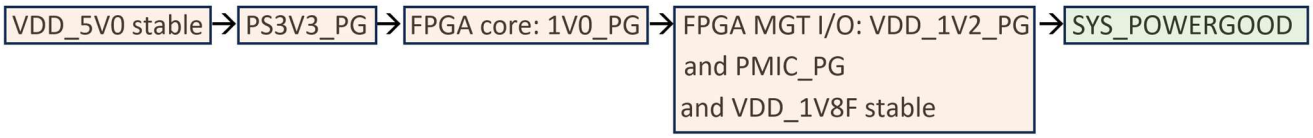


Figure 7: MitySOM-AM57F Power Section

Notes:

- _PG denotes "power good" from supply voltage monitor
- SYS_POWERGOOD is drawn as POWERGOOD in Figure 6, connecting to card-edge E3[6]

Carrier Board Power Control

The carrier board is responsible for sourcing a +5V power source to the SOM and sources for FPGA Bank I/O voltages. See Figure 8 for a block diagram of a typical power section for a carrier board designed to support the MitySOM-AM57F.

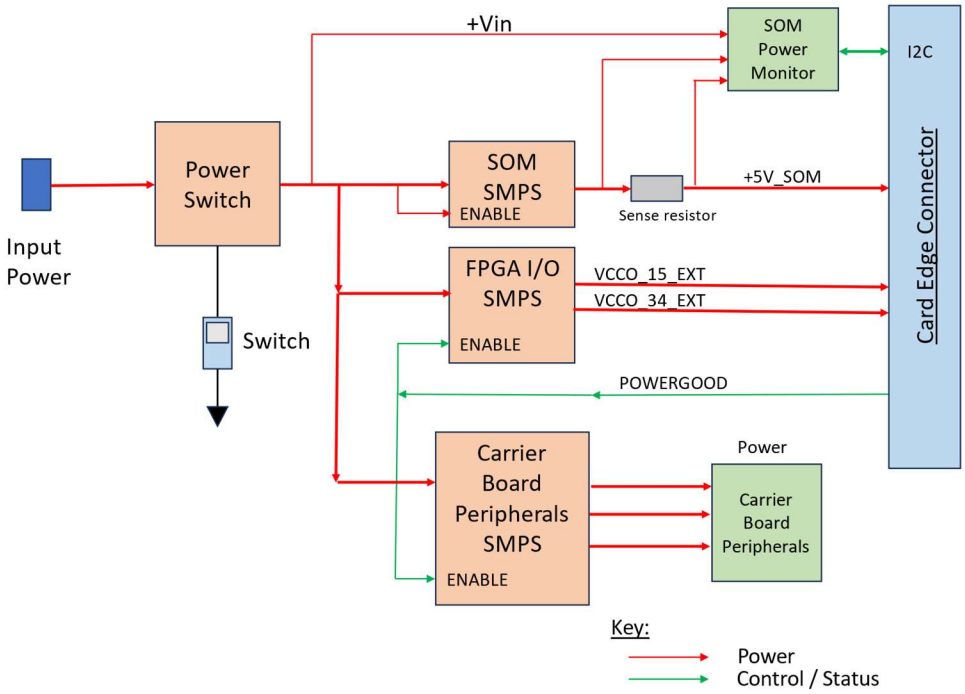


Figure 8: Carrier Board Power Section Block Diagram

Features of Carrier Board Power Section (refer to Figure 8 above):

- Input power, such as +12 VDC, is provided from an external source via a power jack or header, as shown in Figure 8.
- An optional power on/off switch circuit allows power to be removed from the carrier board and SOM without unplugging the external power source.
- As shown, DC-DC converters, or switched mode power supplies (SMPS) are typically used to source power for the SOM, FPGA Bank I/O and peripheral devices.
    - The SMPS sourcing +5V to the SOM is enabled when (switched) input power is applied.
    - FPGA Bank I/O may be sourced from the SOM-generated PS_3V3 (+3.3V) or PS_1V8 (+1.8V) by routing those nets to VCCO_15_EXT and/or VCCO_34_EXT at the MS connector. If this method is used, the design must consider the limits noted in Table 3 above.
    - Other SMPS circuits are enabled by the POWERGOOD signal from the SOM. Using POWERGOOD to enable the peripheral device power ensures that the SOM's PMIC (power management IC) has completed its power-up sequence before the carrier board powers up signals which interface with SOM I/O.
    - Note: POWERGOOD is an open collector signal; a voltage divider network (not shown) may be needed on the carrier board to produce a compatible signal level on the ENABLE input of the SMPS device(s).
- A SOM power monitor (shown) and voltage monitor for other DC voltages (not shown), readable by the SOM over a digital serial interface like I^2C, is optional, but recommended, especially during early stage development.

SOM power usage is highly dependent on the user's application. It is advisable to over-design the SOM power supply capacity for early stage/prototype development, then optimize the size of the power source circuitry according to the application / end user needs during later stages of development.

3.2 Recommended Capacitance

All MitySOM-AM57F family modules include some power supply rail bypass capacitors on-board, however additional capacitance is recommended on the carrier board to minimize the ripple effect caused by changing load currents. It is recommended to place at least 20 µF in bulk capacitors nearby the main +5V supply pins in addition to whatever bulk capacitance is recommended for the SOM +5V supply design. For each of the other power supplies on the carrier board, at least 10 µF in bulk capacitors is recommended. Please note that this is the minimum recommended amount of bulk capacitance, and more is typically better. SMPS controller device datasheets often specify amounts of bulk capacitance and recommend smaller decoupling capacitors placed around the board.

3.3 SOM I/O Interfaces

Voltage Domains

Most I/O pins to the **AM57xx SOC** are powered from +1.8 V supply rails. An exception is the MMC/SD interface at +3.3V. See Table 1 for voltage domains of signals. Fixed function ("FF") signals follow signaling standards which may vary from LVCMOS, LVDS, etc.

FPGA I/O pins can support 1.8V, 2.5V or 3.3V I/O supported by the Xilinx Artix-7 FPGA series. LVDS signal pairs may be supported when the I/O bank voltage is set to 2.5V. Bank 15 and Bank 34 I/O voltages are provided to the SOM by the carrier board via MXM connector pins. Refer to Figure 6 and Figure 8 above.

Protection

I/O signals which interface external to the SOM+Carrier board set must be protected to ensure that no out-of-range voltage conditions occur on all I/O pins which direct connect to the AM57x processor or the FPGA. The carrier board should contain the necessary protection/isolation circuits as required for overvoltage, surge and ESD protection. Please refer to the AM57x and Artix-7 series datasheets for details about maximum voltage ranges for 3.3V and 1.8V I/O domains as the maximum ranges are different.

FPGA_DONE signal sourced from the MitySOM-AM57F indicates when the FPGA has completed its configuration process. The carrier board designer may find this signal to be useful as a control for enabling tri-state buffers, transceiver or other devices which connect to FPGA I/O.

3.4 Module Boot Configuration

The MitySOM-AM57F is capable of booting from several peripherals as defined by the state of the 16 GPMC_AD[15..0] / SYSBOOOT[15..0] pins at the time of a reset. The state of the 16 data lines is sampled on the rising edge of the PORz_OUT signal to determine the search order of peripherals for a valid boot image. Most of the GPMC_AD signals are not routed to the carrier board, and are strapped (via pullup / pulldown resistors) to defined logic levels on the SOM. Only SYSBOOT[2] is available at the carrier through the setting of AM57_BOOT_MODE (at 100-pin HiRose connector). See Table 4 for available boot order options.

AM57_BOOT_MODE:	SYSBOOT[15:0] value:	Boot Order:
0	1000 0001 0010 0110 (0x8126)	QSPI1_CS0, SD, USB
1 (default)	1000 0001 0010 0010 (0x8122)	SD, eMMC2, USB

Table 4: Boot Order Options

AM57_BOOT_MODE is pulled up to +1.8V on the AM57F SOM. The carrier card may provision a jumper to GND to force AM57_BOOT_MODE = 0. If this jumper to GND is not installed, AM57_BOOT_MODE = 1. See the illustration below, where the jumper connects to AM57_BOOT_MODE at the 100-pin HiRose connector.

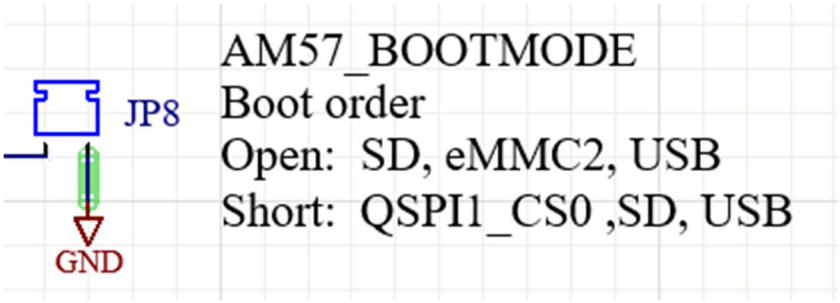


Figure 9: AM57_BOOTMODE jumper on Carrier Board select boot order

For more details on SYSBOOT operations, see the appropriate Technical Reference Manual from Texas Instruments for the AM57x processor installed on the AM57F SOM.

3.5 Module Reset

On the MitySOM-AM57F module, the main power input supply and all on-module generated power supplies are monitored and will trigger a module hard-reset if any of them fails or goes unstable. The main and MCU Power-on-Reset (POR) pin on the AM57x processor, is controlled by the PMIC and is not directly accessible to the carrier board interface. The PMIC provides an external push-button reset input. The PMIC input is pulled up on the SOM. A momentary connection to GND on PB_RESETn, accessed at MXM connector pin E3-5 will cause the SOM to reset.

Resets for peripheral devices on the carrier board are recommended to be sourced from an AM57x GPIO or FPGA I/O.

3.6 Console UART

It is strongly recommended that UART3 be used as a general-purpose monitor port. All of the u-Boot console and kernel console IO data is routed to UART3 (with no HW flow control) by default in the reference software development images. Using UART3 pins for other functions will require modification of low-level boot software (e.g., U-Boot) and the kernel configuration to disable kernel logging to this port. Modern board designs typically use a USB to UART bridge chip to support standard USB style serial ports (COM ports for windows, ttyUSBX ports for Linux). The Critical Link reference design utilizes an FTDI FT230XS UART-to-USB bridge chip to interface UART3 to a USB Type B connector port.

Note: UART3 signals from the AM57x SoC are +1.8V logic; a level shifter to +3.3V logic levels is likely needed in-line between the SOM and UART-to-USB bridge device.

3.7 USB Interface

In addition to USB data lanes (USBn_DP/DM, USB1_SSRX_P/N, USB1_SSTX_P/N), carrier card designs intending to support USB operation on either USB1 or USB2 must utilize the signals listed below depending on intended

operation. Users are encouraged to review the MitySOM-AM57F development kit as a reference design for Dual Role or Host only operation.

Note: 0.1uF AC coupling caps are installed on the SOM for USB1_SSTX_P/N nets, do not add them to the baseboard.

Note: Do not crossover USB1_SS_TX and RX between the SOM and the external connector. The cables are expected to do this when necessary. However it is allowed to swap the plus/minus on either or both of the SS differential pairs, per the USB3 spec.

- **Dual Role**: The USB ID pin from the USB receptacle must be connected to an available GPIO pin with a suitable pullup. The USBn_DRVVBUS must be connected to the enable control of a +5V VBUS power supply for use in Host Mode. There is a single USB_VBUS net which is used in device mode to detect a host is connected. If you want to use both USB ports in dual role, you may need to add a 2nd comparator circuit. Some USB-C mux chips, may have a built-in comparator that might be used for this purpose like the HD3SS3220, though we didn't make use of that feature in the devkit reference design.

- **Host Only**: The USBn_DRVVBUS must be connected to the enable control of a +5V VBUS power supply for use in Host Mode. The USB_VBUS (pin 240 J1) signal should be grounded. Please refer to the AM57x datasheet for additional detail.
- **Device Only**: The USBn_DRVVBUS should be left unconnected. There is a single USB_VBUS net which is used to detect a host is connected. If you want to use both USB ports in dual role, you may need to add a 2nd comparator circuit. Some USB-C mux chips, may have a built-in comparator that might be used for this purpose like the HD3SS3220, though we didn't make use of that feature in the devkit reference design.

The USB_VBUS (pin 240 J1) signal is connected to a comparator on the SOM's TPS6590379 VBUS pin. When USB_VBUS is greater than 2.9V, its VBUSDET signal will go high which is connected to GPIO4_22 on the SOM. This is used by the USB driver to detect USB insertion and enable/disable USBn_DRVVBUS. If not used, this pin should be pulled to ground.

Refer to "TUSB73x0 Board Design and Layout Guidelines – silu149e.pdf" for detailed USB layout guidelines.

4 Interface Descriptions

The sections below provide an overview of peripheral interfaces available to the AM57x SOM-based system designer. Not all AM57x peripherals are available to the carrier board designer. For detailed guidance, please consult the AM57x device datasheets and Technical Reference Manual. Note that most peripheral pins from the AM57x SOC are shared with other peripherals. Establishing a PINMUX configuration for the system design is a necessary first step to determine the mix of peripherals which are available to the user's application.

4.1 Emulator / JTAG

MitySOM-AM57F SOMs include connectivity for DSP emulation and FPGA JTAG. There is a dedicated on-module Hirose header that is intended for use with a Critical Link supplied breakout cable/adaptor.

The DSP emulator connection is used for code download to RAM, and real-time debugging with TI's Code Composer Studio. The FPGA JTAG connection is used for the download of images directly into the FPGA, and for debug with tools such as Xilinx's Integrated Logic Analyzer (ILA). All on-module signals are directly connected to the DSP and FPGA pins. Connection to the emulator/JTAG pods via appropriate headers should be direct and made as short as possible, within reason.

4.2 McASP Port

The MitySOM-AM57F module can support up to 8 Multi-Channel Audio Serial Ports (McASP). The McASP functions as a general-purpose audio serial port optimized for the needs of multichannel audio applications. The McASP:

- is useful for time-division multiplexed (TDM) stream, Inter-Integrated Sound (I2S) protocols, and intercomponent digital audio interface transmission (DIT);
- consists of transmit and receive sections that may operate synchronized, or completely independently with separate master clocks, bit clocks, and frame syncs, and using different transmit modes with different bit-stream formats.
- includes serializers that can be individually enabled for either transmit or receive.

Critical Link's AM57x Development Board includes a reference design for a stereo bidirectional CODEC controlled by a McASP port. Design data is available to developers by request.

4.3 Serial UARTs

The MitySOM-AM57F module can support up to 10 Universal Asynchronous Receive/Transmit (UART) ports with a variety of support for external devices types and flow control. UART3 should be configured as debug UART port; see section 3.6 above (Console UART). Other UARTs may be configured per application needs.

4.4 McSPI Ports

The MitySOM-AM57F module can support up to 4 Multi-Channel Serial Peripheral Interface (McSPI) ports with chip selects directly controlled by the on-chip peripheral. Additional chip selects can be implemented with general GPIO pins if necessary

4.5 QSPI port

The MitySOM-AM57F supports a quad Serial Peripheral Interface (QSPI). The QSPI port is dedicated to supporting serial NOR FLASH on the SOM and is not routed to the carrier board interface.

4.6 I2C Ports

The MitySOM-AM57F module can support up to 5 Inter-Integrated Circuit (I2C) ports, numbered 1-5. I2C[1] is reserved for use by the SOM EEPROM, LED controller and PMIC. I2C[2] and I2C[4] are not routed to the carrier board interface; I2C[3] and I2C[5] are available to the carrier board via the MXM connector. The I2C bus implementations are true open-drain style interfaces when configured correctly, and proper pull-up resistors must be included on the carrier card to the correct bank voltage pin as listed in the MitySOM-AM57F datasheet.

4.7 USB

The MitySOM-AM57F provides two Universal Serial Bus (USB) interfaces which route controller-side PHY connections to the carrier board interface. USB 2.0 and USB 3.0 are supported. See section 3.7 above for additional information.

Both USB ports can operate in Dual Role mode and are USB 2.0 compliant with USB1 also supporting USB3.0 superspeed (5Gbps). Dual role mode protocols support dynamic switching from host mode (e.g., for controlling USB mass storage devices such as thumb drives) to device mode (e.g., for interfacing to a PC) based on application software.

Successful implementation of high-speed USB must consider VUSB switching and protection, data line protection and termination, paired nets, matched lengths and controlled impedance in the carrier board design. Critical Link has reference designs for using USB-C physical interface and multi-port USB hubs. Design data is available to developers by request.

4.8 Display Controllers

The MitySOM-AM57F supports up to 3 LCD controllers and an HDMI 1.4a port. LCD ports 1 and 2 (VIN, VOUT) are routed to the carrier board; LCD port 3 is allocated to the GPMC interface on the SOM.

A successful implementation of HDMI has in-line transformer/choke requirements, data line protection and termination, paired nets, matched lengths and controlled impedance in the carrier board design. Critical Link's AM57x Development Board includes a reference design for an HDMI. Design data is available to developers by request.

Successful implementation of LCD interfaces must account for the targeted display's data formatting, clock speed, resolution, color depth and electrical signal type (single-ended, LVDS, etc.). A serializer device, backlight driver/controller and clock synthesizer are examples of peripherals which may be needed in the system design to adapt the AM57x SOC video interface to the targeted LCD interface.

4.9 CAN Ports

The MitySOM-AM57F supports up to two DCAN (dual Controller Area Network) interfaces. DCAN ports support bit rates up to 1 Mbps, conform to CAN protocol 2.0 A, B, and have DMA and interrupt support. Refer to AM572x datasheet for more information. DCAN signals are routed from the AM57x SOC to the carrier board; the AM57x Development Board does not include CAN interface support.

4.10 Timers

The MitySOM-AM57F supports 16 timers; I/O may be allocated to timer events which may be used the carrier board as PWM outputs or event triggers, for example.

4.11 Multi-Media Card Interfaces

The MitySOM-AM57F module supports up to 4 Multi-Media Card (MMC) interfaces that also support Secure Digital (SD) and Secure Digital Input/Output (SDIO) formats. MMC1 and MMC4 support 4-bit data; MMC2 and MMC3 support 8-bit data. MMC1, MMC2 and MMC3 I/O are routed to the carrier board interface; MMC4 I/O are used as GPIO on the SOM to support USB peripherals.

In general, a 4-bit interface (MMC1) is typically used to interface to a MicroSD card as a boot device and/or external storage. 8-bit devices (MMC2, MMC3) may be used for storage devices like eMMC, though it is often used to integrate with wireless modules that interface with SDIO host controllers.

Critical Link's AM57x Development Board includes a reference design for interfacing MMC1 to a microSD card slot and MMC2 to a wireless Bluetooth module. Note that MMC1 I/O operates at +3.3V; see section 3.3 above. Design data is available to developers by request.

4.12 Serial ATA (SATA)

The MitySOM-AM57F module supports a serial ATA (SATA) port which is typically used to interface with an external hard drive. Successful implementation of a SATA interface must consider data line protection, in-line capacitors on data lines, paired nets, matched lengths and controlled impedance in the carrier board design. Critical Link's AM57x Development Board includes a reference design for a SATA. Design data is available to developers by request.

4.13 General Purpose Memory Controller

The MitySOM-AM57F module contains a General Purpose Memory Controller (GPMC) which is used as a dedicated interface with the FPGA. GPMC lines are also used during boot to set the 16 system mode bits; see section 3.4 of this document. The GPMC is not routed to the carrier board interface. The GPMC supports up to 133 MHz external memory clock performance.

4.14 10/100/1000 Ethernet

The MitySOM-AM57F module supports two Gigabit (1000 Base-T) and two PRUSS 10/100 Megabit Ethernet PHY interfaces. Gigabit Ethernet uses reduced gigabit media independent interfaces (RGMII) to connect to a physical interface (PHY) device, 10/100 Ethernet uses reduced media independent interfaces (RMII). Critical Link's AM57x Development Board includes a reference design for all 4 interfaces.

4.15 PCI Express (PCIe)

The MitySOM-AM57F module supports two PCI Express SuperSpeed (PCIe SS) ports. Two PCIe channels connect between the AM57x SOC and the Artix-7 FPGA. Two PCIe channels are routed from the FPGA to the carrier board interface at the HiRose 100-position connector.

4.16 General Purpose I/O (GPIO)

Many of the AM57x SOC I/O which are not assigned to specified peripheral functions may be configured as General Purpose Input/Output (GPIO) pins, with many available at the carrier board interface. In addition, 96 FPGA I/O are routed to the carrier board interface. Tables 1 and 2 of this document identify available GPIO pins and their voltage domain. Register settings corresponding to each GPIO pin are described in the AM57F datasheet, AM57x SOC datasheet and Technical Reference Manual.

4.17 AM57x SOC-to-FPGA

This section lists, in Xilinx .xdc constraint file format, the AM57x pins which are directly connected to the Artix-7 FPGA. This section of an .xdc may be imported as a portion of the FPGA pin-out for the end application. The FPGA designer will add similar lines to an XDC for signals which interface with the carrier board.

- FPGA package pin location is given after "PACKAGE_PIN"
- AM57x or system net name is given after "get_ports"
- # in column 1 or after a semi-colon indicates a comment

Table 5: AM57x SOC-to-FPGA I/O

```
##################################################
# Package Pin Constraints
##################################################
# set_property PACKAGE_PIN <pin name> [get_ports <port>]
# Start of SOM on-board I/O -------------------------

set_property PACKAGE_PIN R6 [get_ports sys_rst_n]
set_property PACKAGE_PIN J6 [get_ports cpu_nmi_n]
set_property PACKAGE_PIN D10 [get_ports {i_id[0]}]
set_property PACKAGE_PIN H14 [get_ports {i_id[1]}]
#    GPMC Interface
set_property PACKAGE_PIN L14 [get_ports {i_gpmc_ben[1]}]
set_property PACKAGE_PIN N16 [get_ports {i_gpmc_ben[0]}]
set_property PACKAGE_PIN K18 [get_ports i_gpmc_wen]
set_property PACKAGE_PIN R18 [get_ports i_gpmc_oe_n]
set_property PACKAGE_PIN L15 [get_ports i_gpmc_advn_ale]
set_property PACKAGE_PIN T17 [get_ports i_gpmc_cs_n]
set_property PACKAGE_PIN P15 [get_ports i_gpmc_clk]
set_property PACKAGE_PIN P18 [get_ports {io_gpmc_ad[15]}]
set_property PACKAGE_PIN N18 [get_ports {io_gpmc_ad[14]}]
set_property PACKAGE_PIN N17 [get_ports {io_gpmc_ad[13]}]
set_property PACKAGE_PIN N14 [get_ports {io_gpmc_ad[12]}]
set_property PACKAGE_PIN M14 [get_ports {io_gpmc_ad[11]}]
set_property PACKAGE_PIN M17 [get_ports {io_gpmc_ad[10]}]
set_property PACKAGE_PIN M16 [get_ports {io_gpmc_ad[9]}]
set_property PACKAGE_PIN M15 [get_ports {io_gpmc_ad[8]}]
set_property PACKAGE_PIN K15 [get_ports {io_gpmc_ad[7]}]
set_property PACKAGE_PIN J14 [get_ports {io_gpmc_ad[6]}]
set_property PACKAGE_PIN L18 [get_ports {io_gpmc_ad[5]}]
set_property PACKAGE_PIN K17 [get_ports {io_gpmc_ad[4]}]
set_property PACKAGE_PIN J16 [get_ports {io_gpmc_ad[3]}]
set_property PACKAGE_PIN J15 [get_ports {io_gpmc_ad[2]}]
set_property PACKAGE_PIN L17 [get_ports {io_gpmc_ad[1]}]
set_property PACKAGE_PIN K16 [get_ports {io_gpmc_ad[0]}]
#    Interrupts
set_property PACKAGE_PIN J18 [get_ports {sys_nirq[0]}]
set_property PACKAGE_PIN U10 [get_ports {sys_nirq[1]}]
#    Video Port
#set_property PACKAGE_PIN P14 [get_ports VIN_CLK]       ;  # IO14_L12P
#set_property PACKAGE_PIN V12 [get_ports {VIN_D[23]}]   ;  # IO14_L21P
#set_property PACKAGE_PIN U11 [get_ports {VIN_D[22]}]   ;  # IO14_L23P
#set_property PACKAGE_PIN T13 [get_ports {VIN_D[21]}]   ;  # IO14_L19N
#set_property PACKAGE_PIN V11 [get_ports {VIN_D[20]}]   ;  # IO14_L23N
#set_property PACKAGE_PIN V9  [get_ports {VIN_D[19]}]   ;  # IO14_L24N
#set_property PACKAGE_PIN T12 [get_ports {VIN_D[18]}]   ;  # IO14_L22P
#set_property PACKAGE_PIN R13 [get_ports {VIN_D[17]}]   ;  # IO14_L19P
#set_property PACKAGE_PIN U9  [get_ports {VIN_D[16]}]   ;  # IO14_L24P
```

```
#set_property PACKAGE_PIN V14 [get_ports {VIN_D[15]}]   ;  # IO14_L20N
#set_property PACKAGE_PIN T15 [get_ports {VIN_D[14]}]   ;  # IO14_L13N
#set_property PACKAGE_PIN U14 [get_ports {VIN_D[13]}]   ;  # IO14_L20P
#set_property PACKAGE_PIN U15 [get_ports {VIN_D[12]}]   ;  # IO14_L17P
#set_property PACKAGE_PIN V13 [get_ports {VIN_D[11]}]   ;  # IO14_L21N
#set_property PACKAGE_PIN T14 [get_ports {VIN_D[10]}]   ;  # IO14_L13P
#set_property PACKAGE_PIN R15 [get_ports {VIN_D[9]}]    ;  # IO14_L12N
#set_property PACKAGE_PIN U12 [get_ports {VIN_D[8]}]    ;  # IO14_L22N
#set_property PACKAGE_PIN P16 [get_ports {VIN_D[7]}]    ;  # IO14_L11N
#set_property PACKAGE_PIN R17 [get_ports {VIN_D[6]}]    ;  # IO14_L14N
#set_property PACKAGE_PIN T18 [get_ports {VIN_D[5]}]    ;  # IO14_L15N
#set_property PACKAGE_PIN R16 [get_ports {VIN_D[4]}]    ;  # IO14_L14P
#set_property PACKAGE_PIN U17 [get_ports {VIN_D[3]}]    ;  # IO14_L16N
#set_property PACKAGE_PIN U16 [get_ports {VIN_D[2]}]    ;  # IO14_L17N
#set_property PACKAGE_PIN V17 [get_ports {VIN_D[1]}]    ;  # IO14_L18N
#set_property PACKAGE_PIN V16 [get_ports {VIN_D[0]}]    ;  # IO14_L18P
#    PCI EXPRESS INTERFACE
#      PCIe on clock 0 and data pairs 0/1
#set_property PACKAGE_PIN E3 [get_ports {pci_exp_rxn[1]}] ;  # MGT_PRX_N0
#set_property PACKAGE_PIN E4 [get_ports {pci_exp_rxp[1]}] ;  # MGT_PRX_P0
#set_property PACKAGE_PIN H1 [get_ports {pci_exp_txn[1]}] ;  # MGT_PTX_N0
#set_property PACKAGE_PIN H2 [get_ports {pci_exp_txp[1]}] ;  # MGT_PTX_P0
#set_property PACKAGE_PIN A3 [get_ports {pci_exp_rxn[0]}] ;  # MGT_PRX_N1
#set_property PACKAGE_PIN A4 [get_ports {pci_exp_rxp[0]}] ;  # MGT_PRX_P1
#set_property PACKAGE_PIN F1 [get_ports {pci_exp_txn[0]}] ;  # MGT_PTX_N1
#set_property PACKAGE_PIN F2 [get_ports {pci_exp_txp[0]}] ;  # MGT_PTX_P1
#
set_property PACKAGE_PIN B6 [get_ports sys_clk_p]
set_property PACKAGE_PIN B5 [get_ports sys_clk_n]
#
#      PCIe on clock 1 and data pairs 2/3
#set_property PACKAGE_PIN G3 [get_ports {pci_exp_rxn[0]}]  ; # MGT_PRX_N3
#set_property PACKAGE_PIN G4 [get_ports {pci_exp_rxp[0]}]  ; # MGT_PRX_P3
#set_property PACKAGE_PIN B1 [get_ports {pci_exp_txn[0]}]  ; # MGT_PTX_N3
#set_property PACKAGE_PIN B2 [get_ports {pci_exp_txp[0]}]  ; # MGT_PTX_P3
#set_property PACKAGE_PIN C3 [get_ports {pci_exp_rxn[1]}]  ; # MGT_PRX_N2
#set_property PACKAGE_PIN C4 [get_ports {pci_exp_rxp[1]}]  ; # MGT_PRX_P2
#set_property PACKAGE_PIN D1 [get_ports {pci_exp_txn[1]}]  ; # MGT_PTX_N2
#set_property PACKAGE_PIN D2 [get_ports {pci_exp_txp[1]}]  ; # MGT_PTX_P2
#set_property PACKAGE_PIN D5 [get_ports sys_clk_n]       ; # MGT_REFCLK_0N
#set_property PACKAGE_PIN D6 [get_ports sys_clk_p]       ; # MGT_REFCLK_0P
#
# End of SOM on-board I/O ----------------------------
```

Note: Elsewhere in the XDC constraints, the designer must specify the IO Standard and voltage for each FPGA pin. For Bank 15 and Bank 34 I/O, this will depend on the I/O voltage supplied from the carrier board interface.

5 Mechanical Requirements

The following sections describe some of the mechanical requirements of incorporating a MitySOM-AM57F module in a carrier board design. See also sections 1.5, 1.6 and 2 of this document which describe the SOM dimensions, connector set and placement requirements.

5.1 Module Clearance

All AM57x SOM types use an MXM style card edge mated to a receptacle on the carrier board for the primary electrical and mechanical attachment to the carrier board. A secondary 100-position high density connector set provides additional I/O and locks the SOM into position. This connector set, positions the SOM parallel to the carrier board, and as such there is limited clearance between the SOM and the carrier board. Therefore, it is impossible to place high-profile carrier board components underneath the SOM. However, it is possible to utilize most of this space for low-profile components. Please refer to Figure 10 for under-SOM vertical headroom.

A STEP model and an Altium Designer footprint of the SOM is available from the Critical Link support site, and users are encouraged to verify clearance if making use of the space under the module.

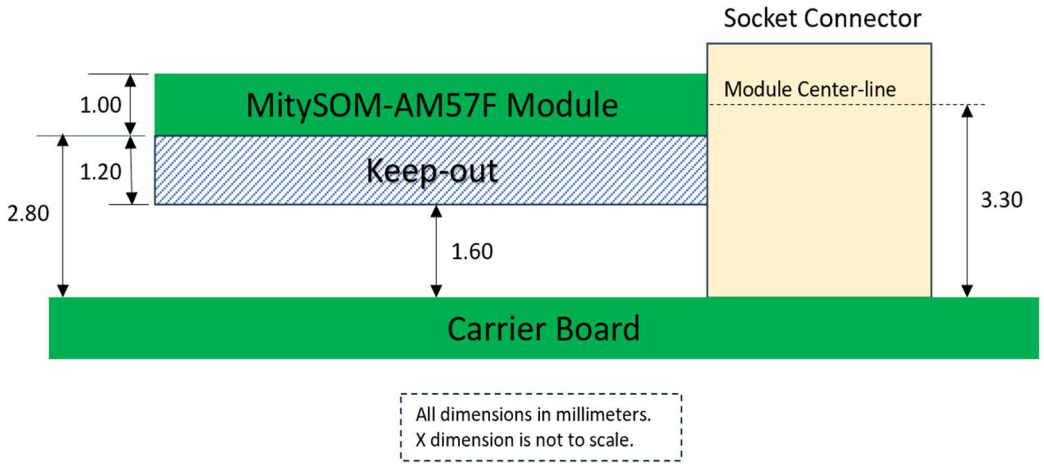


Figure 10: MitySOM-AM57F Module Clearance - Side View

5.2 Mounting Methods

The modules feature an additional optional mechanical attachment method. A hard mechanical attachment by board-to-board standoffs and screw hardware may be used to mount the module. The corners of the free-floating edge of the SOMs feature mounting holes that are compatible with M3 size mounting hardware. The

mechanical drawing in Figure 1 below illustrates the mechanical requirements of this optional attachment method.

Suggested standoff part (on carrier board): Penn Engineering **SMTSO-M3-3ET** or equivalent.
Description: Standoff, round, solderable, threaded, metric, M3 X 5.56 O.D. X 3.00 H.
4.22 (0.166") hole, 6.2 (0.244") pad diam.

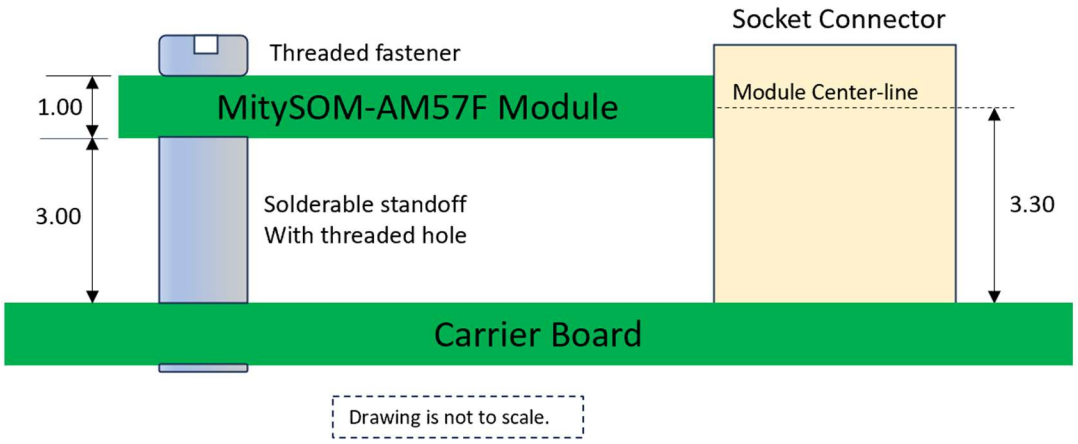


Figure 11: 3.0 mm height standoff mounting: side view

5.3 Shock & Vibration

For customers who are interested in using MitySOM-AM57F modules in rugged environments, the mounting attachment method discussed in section 5.2 above enable these SOMs to tolerate much greater mechanical shock and vibration forces than without any additional mounting support.

5.4 Thermal Management

The MitySOM-AM57F family of SOMs have no specific requirements regarding thermal management. Depending on the core clock speeds, number of processing cores and peripheral modules in use, the AM57F SOM may be operated without heat sinks or air flow, and inside tight enclosures. Customer qualification and testing of SOM device temperatures in the end application is highly recommended. The AM57x SOC and the Artix-7 FPGA feature internal die temperature sensors which may be monitored by the system software. Monitoring the die temperature on highly integrated devices may enable operation at higher temperatures compared to monitoring ambient environment temperatures. It may be necessary or prudent to add thermal management devices to the SOM and/or enclosure or lower the operating temperature specification of the end product.

See section 1.6 of this document for a custom MitySOM-AM57F heat spreader design which can accommodate thermal interfacing with flat surface heatsinks, cold plates or other heat exchangers.

6 Board Layout Recommendations

The following sections discuss topics for successful board layouts incorporating any module.

6.1 Placement

Placement of the module site is crucial to a successful carrier board layout. Because the module connector footprint is fine-pitch and dual-row, it is generally best to place the connector fairly centered in the overall board layout. This placement allows traces to be routed out from both sides of the connector, using mainly top-side copper tracks. The use of less signal layers, and therefore less vias, generally results in a more compact design with better signal integrity than a board using many layers and vias. Of course, central placement is not always possible because of other mechanical constraints.

Mechanically, enough space must be allocated for the full extension of the module. Although it is possible for a module to hang over the edge of its carrier board, this may not be desirable if additional mechanical attachment methods are desired for ruggedness, as discussed in section 5.2. Another thing to keep in mind with placement on the carrier board and in enclosures is the cam-in action of the MitySOM modules into their respective sockets. The modules are generally installed at an angle of about 25° to 30° before swinging down to locked position. Enclosure designs should accommodate this motion.

6.2 Pin-out and Routing

Care must be taken when routing the MitySOM-AM57F high speed interfaces – specifically the USB 2.0 and 3.0 ports, differential pairs, matched length signals, LVDS signals, signals with controlled impedance requirements, clock lines and gigabit Ethernet ports. Please refer to the specific device specification for guidance related to these pins.

6.3 Access issues

Given that it is possible and often desirable to make best use of available space by placing components underneath the MitySOM-AM57F module (refer to section 5.1), hardware and software engineers who will be debugging code on the platform could find themselves in a tough situation if the component they need to access is blocked by the installed MitySOM-AM57F module. Because of these situations it is advisable to either not use the space under the MitySOM-AM57F module for active components that might need live probing with the SOM installed, or only place circuits there that are already tried and tested by engineers on other platforms. If an obscured circuit does need to be probed, it may be necessary to solder temporary wires onto probe points. An even better solution would be to design the board with bottom-side test points, at least in the vicinity of the SOM, when possible, on a given design.

6.4 PCB/PCA Technology

The MitySOM-AM57F module does not have any specific requirements about the PCB technology used for its carrier board. The required socket connectors are available as RoHS compliant and may be used in both leaded and lead-free assembly processes. The only recommendation is to fabricate the carrier board thick enough to rigidly support the MitySOM-AM57F socket connector. In practice, FR-4 with a common finished thickness of 0.062 inches is enough for all types of MitySOM-AM57F modules.

6.5 PCB Footprints

Error! Reference source not found. show the recommended PCB footprint for the JAE MM70-314V1-2-R300 card edge receptacle and the HiRose DF40HC(3.0)-100DS-04V secondary "Hi-Speed" connector. The figures are copied directly from the part drawing. Carrier board designers are advised to check with manufacturers and distributors for the latest versions, application notes or product change notices.

Altium Designer footprints for the MitySOM-AM57F module are available from Critical Link on request for Altium users.

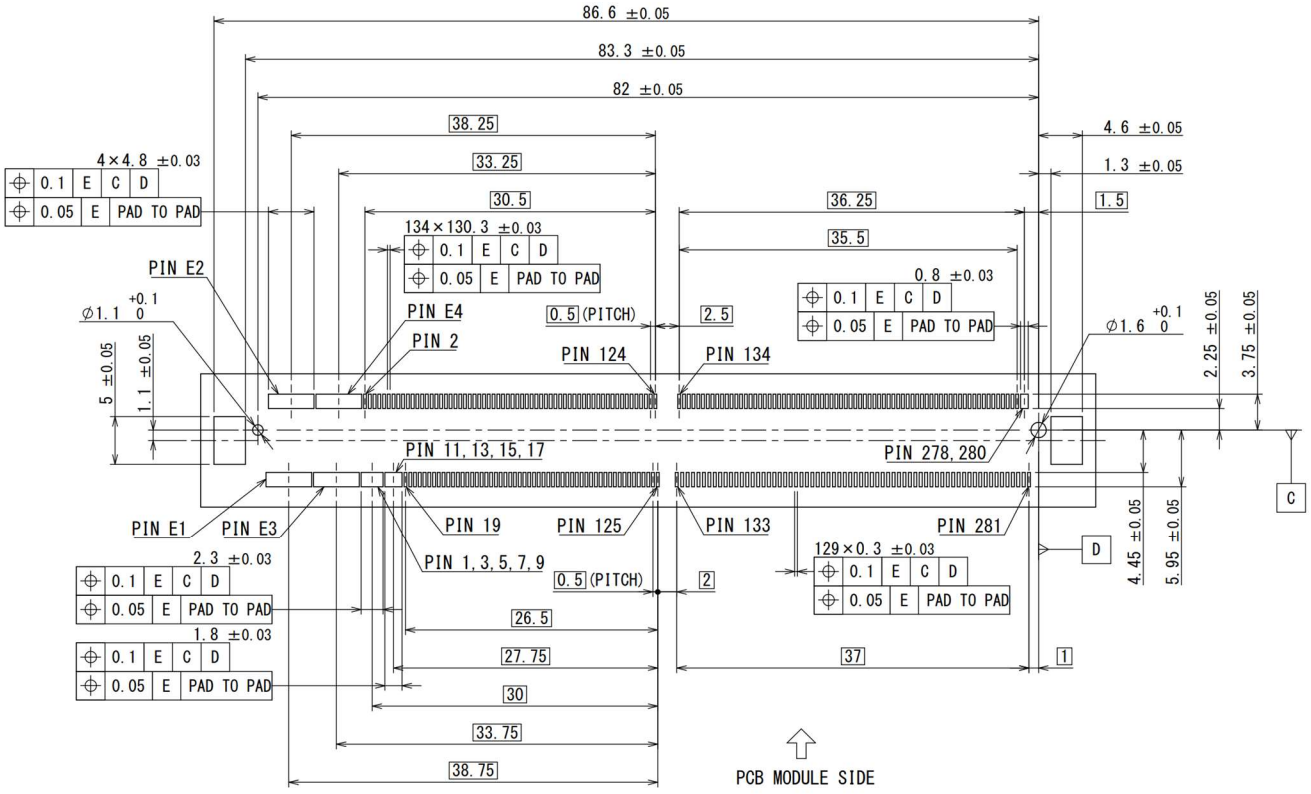
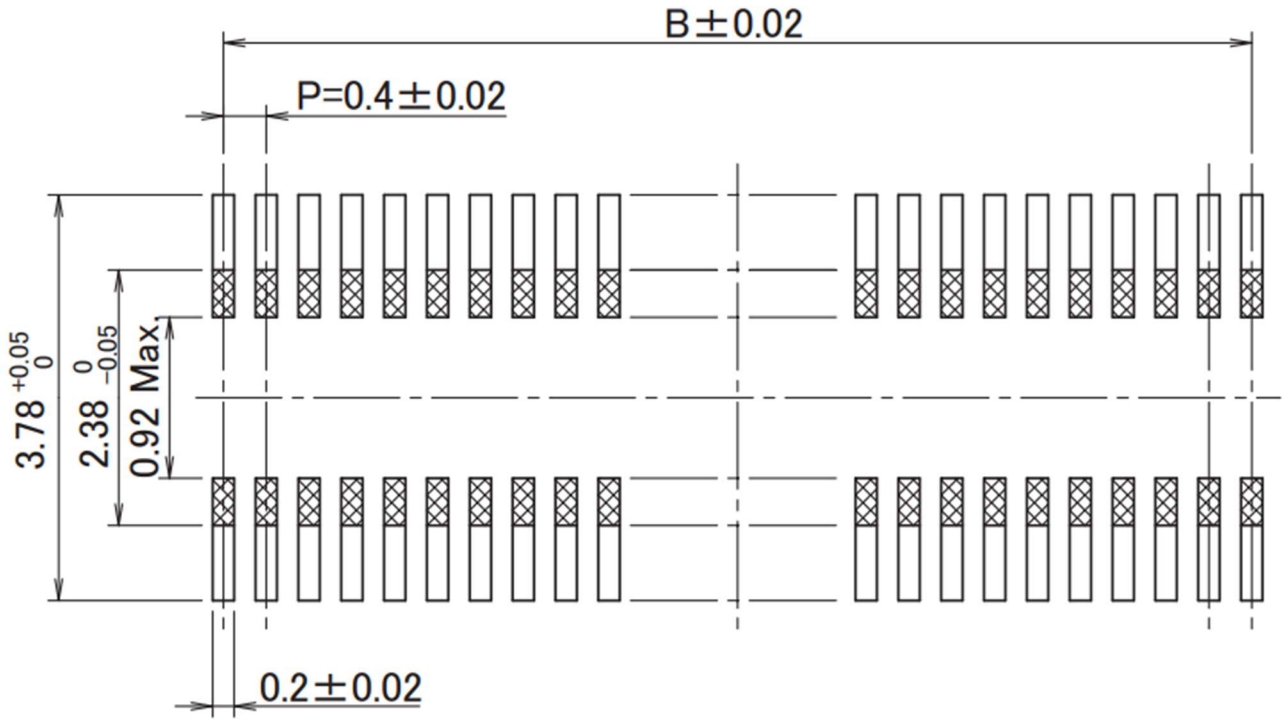


Figure 12: MM70-314B1-2-R300 Recommended PCB Footprint

Recommended PCB Pattern



DF40HC (No Retention Tab)

Stacking Height 3.0mm

Unit : mm

Part No.	HRS No.	No. of Pos.	A	B	C	D	Purchase Unit (##):(51)	Purchase Unit (##):(58)
DF40HC(3.0)-100DS-0.4V(##)	CL0684-4151-0-##	100	22.6	19.6			○	○

【Specification Nmber】
(51) : Embossed Packaging (3,000pcs per reel)
(58) : Embossed Packaging (1,000pcs per reel)

Figure 13: DF40HC(3.0)-100DS-0.4V Recommended PCB Footprint

7 Revision History

Revision	Date	Description of Changes
1.0	20-February-2024	Initial Revision
1.1	5 April 2024	Typo Correction (Table 5 Note)
1.2	5 November 2024	Add reference to carrier schematic checklist (1.2 and 1.7)