FEATURES

MitySOM-A5E Development Board

MitySOM-A5E System on Module

- Agilex™ 5 SoC FPGA E-Series from Altera®: 23mm x 23mm package, with transceivers
- FPGA fabric up to 656 KLE
- Dual-core Cortex-A55 + Dual-core Cortex-A76

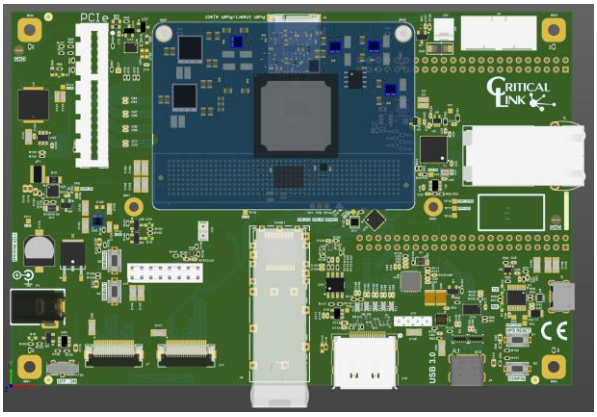
Additional Hardware Included

- USB 2.0 console Cable
- 1 Ethernet Cable
- AC to DC 12V Adapter

Single 12V Power Input

Digital Interfaces

- DisplayPort Video Only Interface supporting 8K video at 60Hz
- USB-C port supporting USB 3.1
- 10/100/1000 Mb Ethernet Interface
- SFP+ supporting up to 10Gb/s
- Micro-USB 2.0 Console Interface
- Micro-SD/MMC Card Socket
- PCIe Gen 4.0 x4 socket
- Two 22-pin 4-lane MIPI camera interface ports
- Dual 46-pin expansion headers



Software and Documentation

- Linux Kernel
- uBoot
- Development Board Schematics
- Development Board Gerber Files
- Development Board BOM

Applications

- Robotics
- Image Processing
- IoT 4.0 edge computing
- Infrastructure and application acceleration
- Artificial intelligence (AI)
- 8K video processing
- Medical Equipment & Imaging
- Automated Test & Measurement
- Embedded Instrumentation
- Retail Automation
- Smart City / Infrastructure
- Broadcast & Pro-AV
- Radar & Defense
- FPGA Prototyping

DESCRIPTION

The MitySOM-A5E Development Board is an interface-rich developer tool, designed to help developers get started developing with Critical Link's MitySOM-A5E, which features the powerful Agilex 5 System On Chip (SoC) FPGA E-Series from Altera, on-board power supplies and memory subsystems. The Agilex 5E SoC is comprised of a dual-core Cortex-A55 processor, dual-core Cortex-A76 processor, and up to 656KLE of FPGA fabric.

The MitySOM-A5E Development kit comes complete with all the connectivity needed in any application well suited for the MitySOM-A5E, including DisplayPort, USB 3.1, Gigabit Ethernet, SFP+ (supporting up to 10 Gb Ethernet), dual x4 lane MIPI CSI camera inputs, and PCIe 4.0. Additionally, the development kit is equipped with a Micro-USB 2.0 console interface, Micro-SD card storage, and a dual 46-pin expansion interface providing support for additional I/O signals.

The on-board DisplayPort supports DisplayPort 1.4 for a total bandwidth of 32.4Gbps with 32 audio channels and 8K video at 60Hz with 10-bit color resolution.

A block diagram of the MitySOM-A5E Development Board is illustrated in Figure 1 below. All available processor interface pins are used directly by the MitySOM-A5E. Control of the onboard interface hardware and connected Expansion IO cards require proper configuration of the Agilex 5E. While not required, it is strongly recommended that the Agilex 5E software development kit and supplied API be used to manage these interfaces.

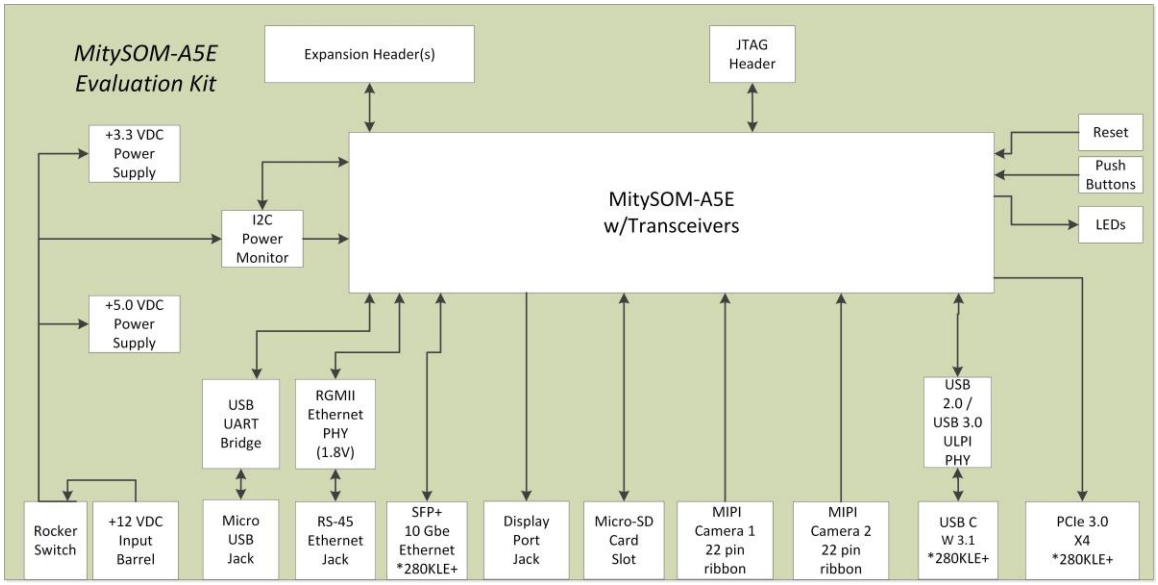


Figure 1: MitySOM-A5E Development Kit Block Diagram

ADDITIONAL DETAILS ABOUT THE ALTERA AGILEX 5, AVAILABLE PERIPHERALS, AND THEIR FEATURES ARE PROVIDED IN THE DATASHEET ON THE ALTERA WEBSITE:
HTTPS://WWW.INTEL.COM/CONTENT/WWW/US/EN/PRODUCTS/DETAILS/FPGA/AGILEX/5.HTML

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FEATURE DESCRIPTIONS

RS-232 / USB Bridge Console Port

The MitySOM-A5E includes a FT230XS UART to USB bridge chip interfacing to the Agilex 5E SoC HPS (Hard Processor System consisting of the dual Cortex-A76 and dual Cortex-A55 processors). With a single micro-USB connection, the console port may be monitored using a standard terminal emulation program.

USB-C 3.1 Interface Description

A USB-C 3.1 is connected to the USB1 interface of the Agilex 5E SoC HPS. The interface is through a USB-C connector, J9, and the port is configured to operate in host mode. Linux drivers are available.

µSD/MMC Card Interface Description

The onboard Micro MultiMedia Card (MMC) slot uses Micro Secure Digital (µSD) connector J4 which supports SD Standard v3.01. It is compatible with standard (SD), SDHC (up to 32GB), and SDXC (Up to 2TB) cards. By default, the MitySOM-A5E boots from this interface.

The MitySOM-A5E development kit includes a µSD flash card. The µSD flash is typically used to store the following types of data:

- Bootloaders
- ARM Linux embedded root file-system
- Runtime ARM software
- Runtime application data (non-volatile storage)

U-Boot configuration information and Linux drivers are available on Critical Link's Support site, https://support.criticallink.com/redmine/projects/mitysom_a5/wiki

Gigabit Ethernet Interface Description

The on-board Ethernet interface features a network PHY capable of running at 10/100/1000 Mbit including link auto-negotiation and MII/MDIO capability. An industry-standard RJ-45 connector is provided (J6) for networking. This Ethernet interface may be used to perform remote code download via U-Boot and FLASH upgrades to the MitySOM-A5E module.

MIPI Camera Interface Description

The MitySOM-A5E Development Board provides two 22-position flat flex cable interfaces, J7 and J11, to the Agilex 5E SoC HPS, MIPI CSI v1.3 compliant devices supporting a data lane at up to 2.5Gbps.

Display Port Interface Description

The MitySOM-A5E Development Board provides a standard display port interface, J10, for external monitor connection. The on-board DisplayPort supports DisplayPort 1.4 for a total bandwidth of 32.4Gbps with 32 audio channels and 8K video at 60Hz with 10-bit color resolution.

SFP+ Interface Description

The Small Form Pluggable interface, J6, supports high data speeds of up to 10Gpbs per data lane.

M.2 PCIe Interface

The MitySOM-A5E Development Board supports PCIe 4.0 on connector J8 and is capable of data rates up to 32Gbps.

TI JTAG Interface Description

A 10-pin 0.1” pitch header, J3, is available onboard for debugging the Agilex 5E SoC HPS with a compatible JTAG Emulator.

Control Pushbuttons

Two debounced normally open, contact to ground, momentary pushbutton is included to signal the Agilex 5E SoC HPS interrupt HPS_COLD_nRESET (button S1), as well as nCONFIG (button S2). Additionally, two debug buttons are connected to HVIO_6D_17 and HVIO_6D_18 (buttons S4 and S5, respectively).

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Maximum Supply Voltage	12 V
Storage Temperature Range	-45 to 85C

OPERATING CONDITIONS

Ambient Temperature Range	-40 to 85C
Humidity	0 to 95% Non-condensing

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Typical	Limit	Units
Maximum Power Supply Output					
I_{Max}	12V Supply (AC Adapter)[1] all components			3.0	A
I_{Max}	12V Supply[2] for external components			1.0	A
I_{Max}	3.3V Supply[2] for external components			1.0	A
Power Dissipation					
V_S	Supply Voltage		12.0±5%		V
I_S	Supply Current[3]		1.0		A

Notes:

1. An alternative higher amperage AC/DC 12V adapter should be considered when using PCIe cards drawing more than 10 Watts (TBC).
2. The maximum current supplied to external components should be limited to the specified maximum for both the 12V and 3.3V supplies.
3. Expansion card not attached, 100% Cortex-A55 and Cortex-A76 utilization, USB, and Dual Ethernet are enabled and active.

ELECTRICAL INTERFACE DESCRIPTIONS

Input Power – P1

The MitySOM-A5E Development Board power interface, P1, requires a single +12Volt power supply. P1 uses a generic barrel connector. Switch S3 is the main power switch and can disable power to the board without having to disconnect P1.

MultiMedia Card (µSD) Interface – J5

The MitySOM-A5E Development Board provides an MMC interface that uses a standard Micro–Secure Digital (µSD) card slot for the physical interface. The slot is supplied with 3.3V for use with standard SD. The pins of the µSD slot are connected to the HPS GPIO pins of the MitySOM-A5E, which allow for multiplexed interfacing.

Table 1: J4 Micro SD Card Connector

J4 Pin	J4 Signal	SoM Interface Signal	J1 Pin
1	DAT2	SDMMC_DATA2	C32
2	CD/DAT3	SDMMC_DATA3	D35
3	CMD	SDMMC_CMD	D33
4	VDD	+3.3V	-
5	CLK	SDMMC_CLK	E36
6	VSS	GND	-
7	DAT0	SDMMC_DATA0	D37
8	DAT1	SDMMC_DATA1	C37
9	Switch (B)	SDCARD_PRSNT	E35
10	Switch(A)	+1.8V	-

USB 3.1 Type-C – J9

The MitySBC-A5E features a USB-C port J9. This interface is a USB 3.1 interface and supports up to 5Gbps throughput speeds and is backward compatible with USB 2.x USB-C devices. The port can supply a maximum of 1A of current at +5V and an overcurrent detection circuit monitors the output power. The pinout for J9 is included in Table 2.

Table 2 USB Host Connector Pin Out, J9

J9 Pin	J9 Signal	U15 Mux or U16 Phy Connection
A1	GND	-
A2	TX1_P	U15 – Pin 14
A3	TX1_N	U15 – Pin 15
A4	VBUS	-
A5	CC1	U15 – Pin 2
A6	USB1_DATA_P	U16 – Pin 18
A7	USB1_DATA_N	U16 – Pin 19
A8	NC	-
A9	VBUS	+5V Supply
A10	RX2_N	U15 – Pin 20
A11	RX2_P	U15 – Pin 21
A12	GND	-
B1	GND	-
B2	TX2_P	U15 – Pin 19
B3	TX2_N	U15 – Pin 18
B4	VBUS	+5V Supply
B5	CC2	U15 – Pin 1
B6	USB1_DATA_P	U16 – Pin 18
B7	USB1_DATA_N	U16 – Pin 19
B8	NC	-
B9	VBUS	-
B10	RX1_N	U15 – Pin 17
B11	RX1_P	U15 – Pin 16
B12	GND	-

USB 3.1 DRP Port Controller – U15

The DRP port controller (MPN: HD3SS3220IRNHR) manages mode configuration, the detection of a USB device, cable orientation detection, role detection and the required power supply for the connected device. All of these can be communicated back to the FPGA via the signals listed below.

Table 3: DRP Port Controller Signals

FPGA Side Signal	J1 Pin	FPGA Pin
USB1_SSRX_P	G43	AU81
USB1_SSRX_N	G42	AU79
I3C1_SDA	F36	E80
I3C1_SCL	D34	F74
USBC_ID_3V3	C18	BV76
USB1_SSTX_N	H44	AV72
USB1_SSTX_P	H45	AV75
USB1_SSTX_P	H45	AV75
USB1_SSTX_N	H44	AV72
I3C1_SDA	F36	E80
I3C1_SCL	D34	F74
USBC_ID_3V3	C18	BV76
USB1_SSRX_N	G42	AU79
USB1_SSRX_P	G43	AU81
USBC_INT_3V3	D19	BR60
USBC_DIR_3V3	D20	BU57
USBC_OR_3V3	D21	BU59
USB1_MuxEnable_3V3	D18	BN60

USB 3.1 ULPI Transceiver – U16

The ULPI transceiver (MPN: USB3320C-EZK) provides role detection and full support for On-The-Go protocol 2.0.

Table 4: ULPI Transceiver Signals

FPGA Sided Signal	J1 Pin	FPGA Pin
USB1_DATA0	C33	K70
USB1_DATA1	D38	A76
USB1_DATA2	E33	B73
USB1_DATA3	D31	K60
USB1_DATA4	E38	A73
USB1_DATA5	F32	F62
USB1_DATA6	F33	B71
USB1_DATA7	E39	A71
USB1_DATA0	C33	K70
USB1_DATA1	D38	A76
USB1_DATA2	E33	B73
USB1_DATA3	D31	K60
USB1_DATA4	E38	A73
USB1_DATA5	F32	F62
USB1_DATA6	F33	B71
USB1_DATA7	E39	A71
USB1_DIR	F37	B76
USB1_NXT	D32	H70
USB1_STP	E37	B78
USB1_CLK	E34	D74

Display Port Interface – J10

The MitySOM-A5E Development Board provides a 20-pin standard display port connector, J10. Supporting display port 1.4, the Agilex 5E can output up to a resolution of 8K at 60Hz.

Table 5: J10 Connector Pin Assignments

J10 Pin	Signal	Type	Standard	J1 Pin	FPGA Pin
1	DispPort Tx0_+	O	HCSL	G35	AP75
2	Shield	Power			-
3	DispPort Tx0_-	O	HCSL	G34	AP72
4	DispPort Tx1_+	O	HCSL	B35	AJ75
5	Shield	Power			-
6	DispPort Tx1_-	O	HCSL	B34	AJ72
7	DispPort Tx2_+	O	HCSL	B39	AC75
8	Shield	Power			-
9	DispPort Tx2_-	O	HCSL	B38	AC72
10	DispPort Tx3_+	O	HCSL	B43	V75
11	Shield	Power			-
12	DispPort Tx3_-	O	HCSL	B42	V72
13	TX_CONFIG1_3V3	I		C25	BV65
14	Reserved	-			-
15	AUX_CH_+	O	HCSL	C24	BV63
16	Shield	Power			-
17	AUX_CH_-	O	HCSL	C23	BV61
18	TX_HPD_3V3	I		C26	BU68
19	GND	Power			-
20	+3.3V	Power			-

Note: The PCIe reference clock is generated by U12 on the development kit, and is on pins G16 (GXBR_REFCLK_P) and G17 (GXBR_REFCLK_P) of J1.

Camera MIPI Interfaces – J7, J11

The MitySOM-A5E Development Board provides two 22-pin 0.5 mm pitch flat flex connectors, J7 and J11, to interface with the Agilex 5E.

Table 6: Camera Mipi Connector Pin Assignments (J7)

J7 Pin	Signal	Type	Standard	J1 Pin	FPGA Pin	Notes
1	+3.3V	Power	-			Max 500 mA
2	CAM1_SDA_3V3	I/O	DPHY_RX	B25	BH74	
3	CAM1_SCL_3V3	I/O	DPHY_RX	B24	BF74	
4	GND	Power	-			
5	CAM1_IO2_3V3	I/O	DPHY_RX	B23	BE69	
6	CAM1_IO1_3V3	I/O	DPHY_RX	B22	BJ69	
7	GND	Power	-			
8	CAM1_CSI_RX3_P	I	DPHY_RX	A05	F15	
9	CAM1_CSI_RX3_N	I	DPHY_RX	A06	H16	
10	GND	Power	-			
11	CAM1_CSI_RX2_P	I	DPHY_RX	B07	K11	
12	CAM1_CSI_RX2_N	I	DPHY_RX	B06	K15	
13	GND	Power	-			
14	CAM1_CSI_RXCLK_P	I	DPHY_RX	A03	F21	
15	CAM1_CSI_RXCLK_N	I	DPHY_RX	A02	D21	
16	GND	Power	-			
17	CAM1_CSI_RX1_P	I	LVCMOS	A08	F24	
18	CAM1_CSI_RX1_N	I	LVCMOS	A09	H24	
19	GND	Power	-			
20	CAM1_CSI_RX0_P	I	LVCMOS / OD	B09	K21	
21	CAM1_CSI_RX0_N	I	LVCMOS / OD	B10	K24	
22	GND	Power	-			

Table 7: Camera Mipi Connector Pin Assignments (J11)

J11 Pin	Signal	Type	Standard	J1 Pin	FPGA Pin	Notes
1	+3.3V	Power	-			Max 500 mA
2	CAM2_SDA_3V3	I/O	DPHY_RX	A24	BK80	
3	CAM2_SCL_3V3	I/O	DPHY_RX	A23	BK81	
4	GND	Power	-			
5	CAM2_IO2_3V3	I/O	DPHY_RX	A22	BG80	
6	CAM2_IO1_3V3	I/O	DPHY_RX	A21	BG81	
7	GND	Power	-			
8	CAM2_CSI_RX3_P	I	DPHY_RX	A17	P27	
9	CAM2_CSI_RX3_N	I	DPHY_RX	A18	P25	
10	GND	Power	-			
11	CAM2_CSI_RX2_P	I	DPHY_RX	B15	V30	
12	CAM2_CSI_RX2_N	I	DPHY_RX	B16	V27	
13	GND	Power	-			
14	CAM2_CSI_RXCLK_P	I	DPHY_RX	A14	P33	
15	CAM2_CSI_RXCLK_N	I	DPHY_RX	A15	V33	
16	GND	Power	-			
17	CAM2_CSI_RX1_P	I	LVCMOS	B13	V35	
18	CAM2_CSI_RX1_N	I	LVCMOS	B12	P35	
19	GND	Power	-			
20	CAM2_CSI_RX0_P	I	LVCMOS / OD	A12	V41	
21	CAM2_CSI_RX0_N	I	LVCMOS / OD	A11	P39	
22	GND	Power	-			

10/100/1000 Ethernet Interface – J2

The MitySOM-A5E Development Board provides an RJ-45 connection for a Gigabit 10/100/1000 Ethernet connection. This connection follows standard TIA/EIA-568B pin-out. By default, the Ethernet PHY will auto-negotiate with its link partner. The J2 connector corresponds to EMAC1 on the Agilex 5E.

Table 8: EMAC1 Signal Connections

Signal	Type	J1 Pin	FPGA Pin
EMAC1_RXD0	I	E42	B65
EMAC1_RXD1	I	D39	K62
EMAC1_RXD2	I	D42	B61
EMAC1_RXD3	I	D45	A61
EMAC1_RX_CLK	I	E47	A51
EMAC1_RX_CTL	I	F41	K67
EMAC1_TXD0	O	E46	B57
EMAC1_TXD1	O	E41	F70
EMAC1_TXD2	O	D44	A65
EMAC1_TXD3	O	F40	H62
EMAC1_TX_CLK	O	D43	B68
EMAC1_TX_CTL	O	E44	A63
I2C_EMAC1_SDA	I/O	E48	A49
I2C_EMAC1_SCL	O	D41	F67

TI JTAG Interface – J3

Table lists the connections to the JTAG interface connector. The connector is intended to support standard Altera USB-Blaster II type JTAG pods.

Table 9: J3 JTAG Pin Assignments

Pin	Schematic Signal	J1 Pin	Type	Standard
1	TCK	H29	I	1.8 V LVCMOS
2	GND	-	Power	-
3	TDO	H30	I	1.8 V LVCMOS
4	+1.8V	-	Power	-
5	TMS	H31	I	1.8 V LVCMOS
6	N/C	-	-	-
7	N/C	-	-	-
8	N/C	-	-	-
9	TDI	H32	I	1.8 V LVCMOS
10	GND	-	Power	-

Fan Header Interface – J15

This header interfaces with the Agilex 5E processor cooling fan. Table lists the connections to the fan header interface. Note: The fan is driven using an active high signal from the SOM pin D47 (FPGA pin B47)

Table 10: J15 Fan Header Pin Assignments

Pin	Schematic Signal	J1 Pin	Type	Standard	Notes
1	+5V	-	Power	-	
2	GND	-	Power	-	Open drain fan enable

IO Expansion Header –P8, P9, J14

The P8 and P9 IO expansion headers provide additional GPIO outputs that can interface with external devices. P8 and P9 are electrically and mechanically compatible with the BeagleBone® Cape connector, but may be used for other board designs are required. The J14 header provides additional GPIO as well as a connection to the I3C bus that is connected to the Agilex 5E.

Table 11: P9 IO Expansion Header Pin Assignments

Pin	Schematic Signal	J1 Pin	Type	Standard	Notes
1	GND	-	Power	-	
2	GND	-	Power	-	
3	+3.3V	-	Power	-	
4	+3.3V	-	Power	-	
5	N/C	-	-	-	
6	N/C	-	-	-	
7	+5.0V	-	Power	-	
8	+5.0V	-	Power	-	
9	HVIO_6D_1	C13	I/O	3.3V CMOS	
10	HVIO_6C_5	E14	I/O	3.3V CMOS	
11	HVIO_6D_2	F14	I/O	3.3V CMOS	
12	HVIO_6C_6	F18	I/O	3.3V CMOS	
13	HVIO_6D_3	C10	I/O	3.3V CMOS	
14	HVIO_6C_7	E17	I/O	3.3V CMOS	
15	HVIO_6D_4	D11	I/O	3.3V CMOS	
16	HVIO_6C_8	E15	I/O	3.3V CMOS	
17	HVIO_6C_20	F19	I/O	3.3V CMOS	
18	HVIO_6C_9	C14	I/O	3.3V CMOS	

19	HVIO_6C_19	E20	I/O	3.3V CMOS	
20	HVIO_6C_10	C11	I/O	3.3V CMOS	
21	HVIO_6D_5	E13	I/O	3.3V CMOS	
22	HVIO_6C_11	D12	I/O	3.3V CMOS	
23	HVIO_6D_6	F13	I/O	3.3V CMOS	
24	HVIO_6C_12	C12	I/O	3.3V CMOS	
25	HVIO_6D_7	D09	I/O	3.3V CMOS	
26	HVIO_6C_13	F17	I/O	3.3V CMOS	
27	HVIO_6D_8	E12	I/O	3.3V CMOS	
28	HVIO_6C_14	D13	I/O	3.3V CMOS	
29	HVIO_6D_9	C08	I/O	3.3V CMOS	
30	HVIO_6C_15	F15	I/O	3.3V CMOS	
31	HVIO_6D_10	C09	I/O	3.3V CMOS	
32	+1.8V	-	Power		
33	HVIO_6D_11	E09	I/O	3.3V CMOS	
34	GND	-	Power		
35	HVIO_6D_12	E05	I/O	3.3V CMOS	
36	HVIO_6C_16	E19	I/O	3.3V CMOS	
37	HVIO_6D_13	E08	I/O	3.3V CMOS	
38	HVIO_6C_17	E18	I/O	3.3V CMOS	
39	HVIO_6D_14	C07	I/O	3.3V CMOS	
40	HVIO_6C_18	E16	I/O	3.3V CMOS	
41	HVIO_6D_15	D07	I/O	3.3V CMOS	
42	HVIO_6D_16	E4	I/O	3.3V CMOS	
43	GND	-	Power	-	
44	GND	-	Power	-	
45	GND	-	Power	-	
46	GND	-	Power	-	

Table 12: P8 IO Expansion Header Pin Assignments

Pin	Schematic Signal	J1 Pin	Type	Standard	Notes
1	GND	-	Power	-	
2	GND	-	Power	-	
3	HVIO_6A_1	F30	I/O	3.3V CMOS	
4	HVIO_6A_3	E30	I/O	3.3V CMOS	
5	HVIO_6A_2	F28	I/O	3.3V CMOS	
6	HVIO_6A_4	F29	I/O	3.3V CMOS	
7	HVIO_6A_13	E22	I/O	3.3V CMOS	
8	HVIO_6C_1	C05	I/O	3.3V CMOS	
9	HVIO_6A_14	E25	I/O	3.3V CMOS	
10	HVIO_6C_2	D14	I/O	3.3V CMOS	
11	HVIO_6A_15	F25	I/O	3.3V CMOS	
12	HVIO_6C_3	D10	I/O	3.3V CMOS	
13	HVIO_6A_16	F21	I/O	3.3V CMOS	
14	HVIO_6C_4	F16	I/O	3.3V CMOS	
15	HVIO_6A_17	F22	I/O	3.3V CMOS	
16	HVIO_6A_19	F23	I/O	3.3V CMOS	
17	HVIO_6A_18	E23	I/O	3.3V CMOS	
18	HVIO_6A_20	E26	I/O	3.3V CMOS	
19	HVIO_6A_5	E31	I/O	3.3V CMOS	
20	HVIO_6A_9	E28	I/O	3.3V CMOS	
21	HVIO_6A_6	E27	I/O	3.3V CMOS	
22	HVIO_6A_10	E24	I/O	3.3V CMOS	
23	HVIO_5A_18	B27	I/O	3.3V CMOS	
24	HVIO_6A_11	F27	I/O	3.3V CMOS	
25	HVIO_6A_8	F26	I/O	3.3V CMOS	
26	HVIO_6A_12	F24	I/O	3.3V CMOS	

27	HVIO_6B_1	G20	I/O	3.3V CMOS	
28	HVIO_6B_11	G26	I/O	3.3V CMOS	
29	HVIO_6B_2	H18	I/O	3.3V CMOS	
30	HVIO_6B_12	H22	I/O	3.3V CMOS	
31	HVIO_6B_3	G21	I/O	3.3V CMOS	
32	HVIO_6B_13	H23	I/O	3.3V CMOS	
33	HVIO_6B_4	G22	I/O	3.3V CMOS	
34	HVIO_6B_14	H25	I/O	3.3V CMOS	
35	HVIO_6B_5	G23	I/O	3.3V CMOS	
36	HVIO_6B_15	H26	I/O	3.3V CMOS	
37	HVIO_6B_6	H19	I/O	3.3V CMOS	
38	HVIO_6B_16	H24	I/O	3.3V CMOS	
39	HVIO_6B_7	G24	I/O	3.3V CMOS	
40	HVIO_6B_17	G28	I/O	3.3V CMOS	
41	HVIO_6B_8	H20	I/O	3.3V CMOS	
42	HVIO_6B_18	G27	I/O	3.3V CMOS	
43	HVIO_6B_9	G25	I/O	3.3V CMOS	
44	HVIO_6B_19	G29	I/O	3.3V CMOS	
45	HVIO_6B_10	H21	I/O	3.3V CMOS	
46	HVIO_6B_20	H27	I/O	3.3V CMOS	

Table 13: J14 IO Expansion Header Pin Assignments

Pin	Schematic Signal	J1 Pin	Type	Standard	Notes
1	+3.3V	-	Power	-	
2	+3.3V	-	Power	-	
3	HVIO_5B_15	C27	I/O	3.3V CMOS	
4	HVIO_5B_10	D26	I/O	3.3V CMOS	
5	HVIO_5B_2	D22	I/O	3.3V CMOS	
6	HVIO_5B_12	D27	I/O	3.3V CMOS	
7	HVIO_5B_5	D23	I/O	3.3V CMOS	
8	N/C	-	-		
9	HVIO_5B_6	D24	I/O	3.3V CMOS	
10	I3C0_SDA_3V3	D46	I/O	3.3V CMOS	Signal passes through a level translator
11	HVIO_5B_11	D25	I/O	3.3V CMOS	
12	I3C0_SCL_3V3	C40	O	3.3V CMOS	Signal passes through a level translator
13	N/C	-	-	-	
14	N/C	-	-	-	
15	GND	-	Power	-	
16	GND	-	Power	-	

INCLUDED COMPONENTS

The following table lists the components that are included with a MitySBC-A5E. See Table for specific ordering information.

Table 14: Included Items

Description	Interface Port	Qty. Included
MitySOM-A5E Development Kit	N/A	Qty. 1
MitySOM-A5E Module	J1	Qty. 1
12V 3A AC to DC Supply	P1	Qty. 1
Ethernet cable – 7 foot	J2	Qty. 1
USB-A to MicroUSB cable	J5	Qty. 1
Fan +5V with adhesive tape	N/A	Qty. 1
MicroSD Card	J4	Qty. 1

MitySOM-A5E Development Kit ORDERING INFORMATION

The following table lists the standard MitySOM-A5E Development Kit configurations. For shipping status, availability, and lead time of these or other configurations please contact Critical Link at info@criticallink.com.

Table 15: Standard Model Numbers

Dev Kit P/N	Module Included	XCVR	Max A76 Speed	FPGA Size	RAM Size	Operating Temp
80-001756	A5EB-B9-C7F-RC-X	Yes	1.8GHz	656 KLE's	8GB	0ºC to +70º C

MECHANICAL INTERFACE DESCRIPTION

Main Board Interface / Mounting

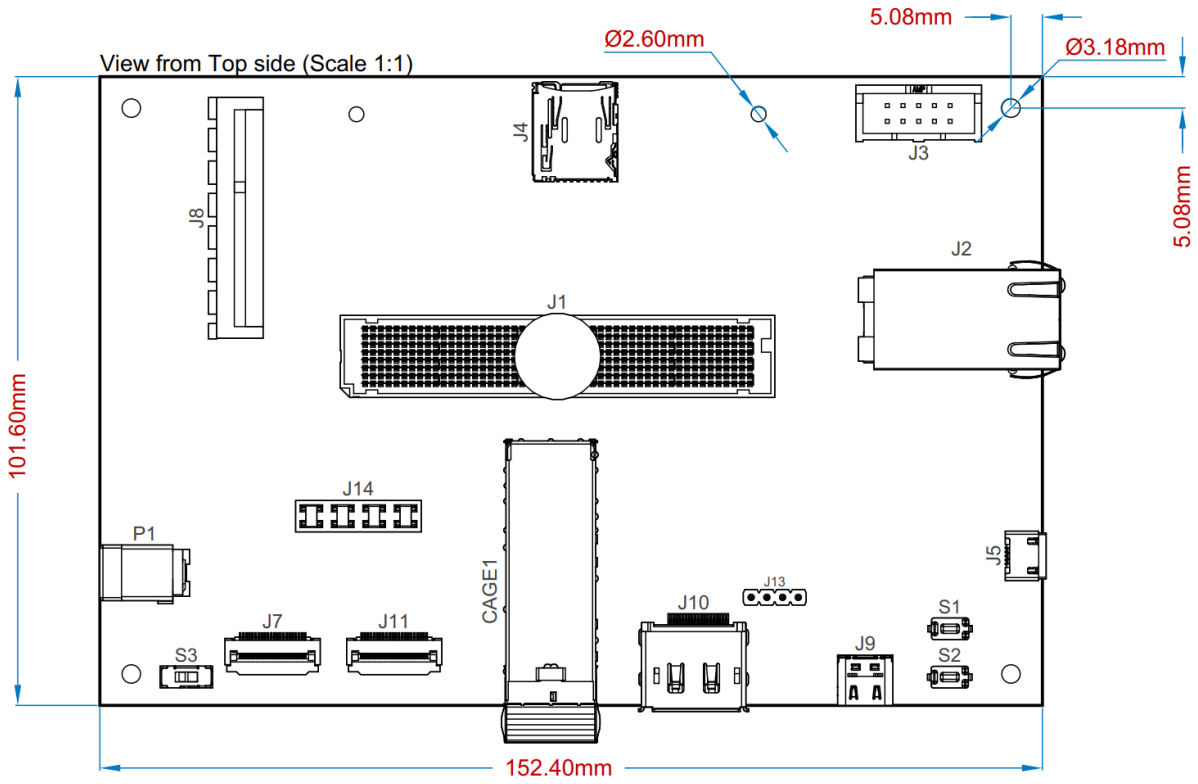

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Figure 2: MitySOM-A5E Development Kit Outline and Mounting Hole Locations (Top View, millimeters)

REVISION HISTORY

Date	Rev	Change Description
29-MAR-2024	A	Initial revision.