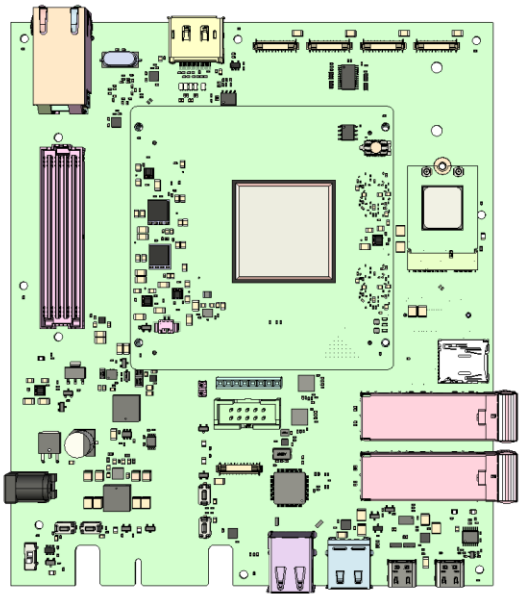
FEATURES



MitySOM-A5E Development Board

MitySOM-A5E System on Module

- Agilex™ 5 SoC FPGA E-Series from Altera®: 32mm x 32mm package, with transceivers
- FPGA fabric up to 656 KLE
- Dual-core Cortex-A55 + Dual-core Cortex-A76

Additional Hardware Included

- USB 2.0 console Cable
- 1 Ethernet Cable
- AC to DC 12V Adapter

Single 12V Power Input

Digital Interfaces

- DisplayPort supporting 8K video at 60Hz
- USB-C port supporting USB 3.1 Gen 1
- 10/100/1000 Mb Ethernet Interface
- 2x SFP+ supporting up to 16Gb/s
- USB-C 2.0 Port Console Interface
- 3x USB Type A connectors (USB 2.0)
- Micro-SD Card Socket
- PCIe Gen 4.0 x4 edge connector
- M.2 E key WIFI interface port
- M.2 M key NVME interface port
- 5 22-pin 4-lane MIPI camera interface
- FMC port with LPC + 8 Transceivers
- I3C Expansion Header

Software and Documentation

- Linux Kernel
- uBoot
- Development Board Schematics
- Development Board Gerber Files
- Development Board BOM

Applications

- Robotics
- Image Processing
- IoT 4.0 edge computing
- Infrastructure and application acceleration
- Artificial intelligence (AI)
- 8K video processing
- Medical Equipment & Imaging
- Automated Test & Measurement
- Embedded Instrumentation
- Retail Automation
- Smart City / Infrastructure
- Broadcast & Pro-AV
- Radar & Defense
- FPGA Prototyping

DESCRIPTION

The MitySOM-A5E Development Board is an interface-rich developer tool, designed to help developers get started developing with Critical Link's MitySOM-A5E, which features the powerful Agilex 5 System On Chip (SoC) FPGA E-Series from Altera, on-board power supplies and memory subsystems. The Agilex 5E SoC is comprised of a dual-core Cortex-A55 processor, dual-core Cortex-A76 processor, and up to 656KLE of FPGA fabric.

The MitySOM-A5E Development kit comes complete with all the connectivity needed in any application well suited for the MitySOM-A5E, including DisplayPort, USB 3.1 Gen 1, Gigabit Ethernet, two SFP+ (supporting up to 10 Gb Ethernet), four x4 lane MIPI CSI camera inputs, and PCIe 4.0. Additionally, the development kit is equipped with a USB-C console interface, Micro-SD card storage, and a LPC FMC expansion interface providing support for additional I/O signals and up to 8 transceiver pairs.

The on-board DisplayPort supports DisplayPort 1.4 for a total bandwidth of 32.4Gbps with 32 audio channels and 8K video at 60Hz with 10-bit color resolution.

A block diagram of the MitySOM-A5E Development Board is illustrated in Figure 1 below. All available processor interface pins are used directly by the MitySOM-A5E. Control of the onboard interface hardware and connected Expansion IO cards require proper configuration of the Agilex 5E. While not required, it is strongly recommended that the Agilex 5E software development kit and supplied API be used to manage these interfaces.

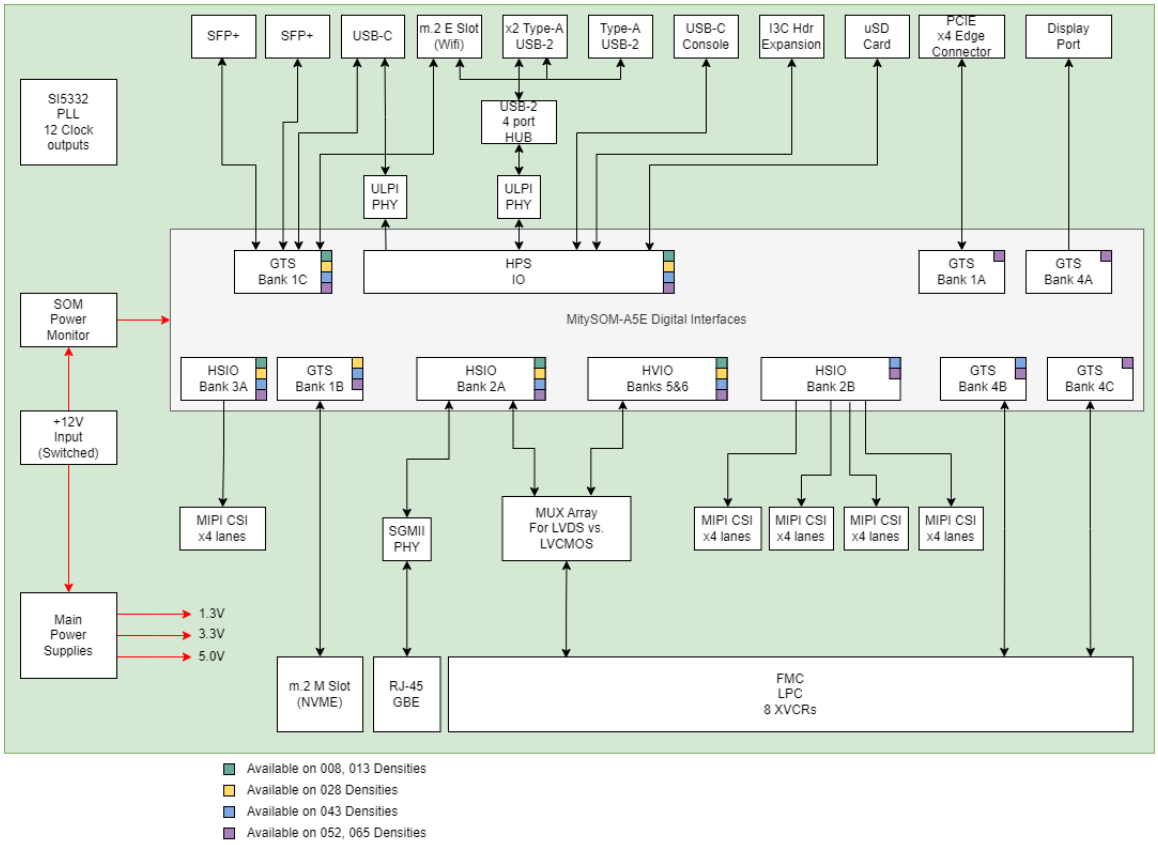


Figure 1: MitySOM-A5E Development Kit Block Diagram

ADDITIONAL DETAILS ABOUT THE ALTERA AGILEX 5, AVAILABLE PERIPHERALS, AND THEIR FEATURES ARE PROVIDED IN THE DATASHEET ON THE ALTERA WEBSITE:
https://www.intel.com/content/www/us/en/products/details/fpga/agilex/5.html

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FEATURE DESCRIPTIONS

RS-232 / USB Bridge Console Port

The MitySOM-A5E Development Board includes a FT230XS UART to USB bridge chip interfacing to the Agilex 5E SoC HPS (Hard Processor System consisting of the dual Cortex-A76 and dual Cortex-A55 processors). With a single USB-C connection, J8, the console port may be monitored using a standard terminal emulation program.

USB-C 3.1 Gen 1 Interface Description

A USB-C 3.1 Gen 1 is connected to the USB1 interface of the Agilex 5E SoC HPS. The interface is through a USB-C connector, J7. The port supports dual-role operation. Linux drivers are available.

µSD Card Interface Description

The Micro Secure Digital (µSD) connector, J4, supports SD Standard v6.1. It is compatible with standard (SD), SDHC (up to 32GB), SDXC (Up to 2TB), and SDUC (up to 128 TB) cards. By default, the MitySOM-A5E boots the linux kernel and mounts a root filesystem from this interface.

The MitySOM-A5E development kit includes a µSD flash card. The µSD flash is typically used to store the following types of data:

- Bootloaders
- ARM Linux embedded root file-system
- Runtime ARM software
- Runtime application data (non-volatile storage)

U-Boot configuration information and Linux drivers are available on Critical Link's Support site, https://support.criticallink.com/redmine/projects/mitysom_a5/wiki

Gigabit Ethernet Interface Description

The on-board Ethernet interface features a network PHY capable of running at 10/100/1000 Mbit including link auto-negotiation and SGMII/MDIO capability. An industry-standard RJ-45 connector is provided (J19) for networking. This Ethernet interface may be used to perform remote code download via U-Boot and FLASH upgrades to the MitySOM-A5E module.

MIPI Camera Interface Description

The MitySOM-A5E Development Board provides five 22-position flat flex cable interfaces - J15, J16, J17, J18, and J20 – that interface with the Agilex 5E SoC HSIO MIPI CSI v1.3 compliant devices supporting a data lane at up to 2.5Gbps.

Display Port Interface Description

The MitySOM-A5E Development Board provides a standard display port interface, J12, for external monitor connection. The on-board DisplayPort supports DisplayPort 1.4 for a total bandwidth of 32.4Gbps with 32 audio channels and 8K video at 60Hz with 10-bit color resolution.

SFP+ Interface Description

Two Small Form Pluggable (plus) interfaces, J5 and J6, support high data speeds of up to 16 Gbps per data lane.

4 Lane PCIe End Point Interface

The MitySOM-A5E Development Board supports up to PCIe Gen 4.0 on connector P1 and can be mated to a 4 lane PCIe riser cable interface to a HOST PC as a card endpoint. Note that the board must be connected to an external power supply. Board power will not be sourced from the P1 edge connector.

FMC Interface

The MitySOM-A5E Development Board includes a 400-pin connector compatible with the ANSI/VITA 57.1 FPGA Mezzanine Connector (FMC) standard. The connector supports up to 8 high speed transceiver pairs and includes support for Low Pin Count (LPC) connections for FPGA IO. The FPGA IO pins can be multiplexed to either an HSIO bank to support true differential signaling or to an HVIO bank to support 1.8V single ended LVCMOS IO on a per pair basis.

M.2 E key Slot (Wifi)

The MitySOM-A5E Development Board includes an M.2 compatible Type-E key connector with support for 1 lane of PCIe, UART, I2C, and USB 2.0 connectivity and will support several Wifi based M.2 E key interface cards. The PCM audio and SDIO interfaces are not supported.

M.2 M key Slot (NVME)

The MitySOM-A5E Development Board includes an M.2 compatible Type-M key connector with support for up to 4 lanes of PCIe and the optional I2C interface and supports most NVME based M.2 cards.

JTAG Interface Description

A 10-pin 0.1” pitch header, J3, is available onboard for programming and debugging the Agilex 5E SoC HPS as well as the programmable logic with a compatible JTAG Emulator.

Control Pushbuttons

Two debounced normally open, contact to ground, momentary pushbuttons are included to signal the Agilex 5E SoC HPS interrupt HPS_COLD_nRESET (button S2), as well as nCONFIG (button S1). Additionally, two debug buttons are connected to HVIO_6D_17 and HVIO_6D_18 (buttons S4 and S5, respectively).

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Maximum Supply Voltage	13.2 V
Storage Temperature Range	-45 to 85C

OPERATING CONDITIONS

Ambient Temperature Range	-40 to 85C
Humidity	0 to 95% Non-condensing

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Typical	Limit	Units
Maximum Power Supply Output					
I_{Max}	12V Supply (AC Adapter)[1] all components			5.0	A
I_{Max}	12V Supply[2] for external components			1.0	A
I_{Max}	3.3V Supply[2] for external components			1.0	A
Power Dissipation					
V_S	Supply Voltage		12.0±10%		V
I_S	Supply Current[3]		1.5		A

Notes:

1. An alternative higher amperage AC/DC 12V adapter should be considered when using FMC cards drawing more than 10 Watts.
2. The maximum current supplied to external components should be limited to the specified maximum for both the 12V and 3.3V supplies.
3. FMC Expansion card not attached, 100% Cortex-A55 and Cortex-A76 utilization, USB, and Ethernet are enabled and active.

ELECTRICAL INTERFACE DESCRIPTIONS

Input Power – P2

The MitySOM-A5E Development Board power interface, P2, requires a single +12Volt power supply. P2 uses a Wurth Electronics 694106301002 2.1mm inner diameter and 5.5mm outer diameter barrel connector. Switch S3 is the main power switch and can disable power to the board without having to disconnect P2.

MultiMedia Card (µSD) Interface – J4

The MitySOM-A5E Development Board provides standard Micro–Secure Digital (µSD) card slot for the physical interface. The slot is supplied with 3.3V for use with standard SD. The pins of the µSD slot are connected to the HPS GPIO pins of the MitySOM-A5E, which allow for multiplexed interfacing.

Table 1: J4 Micro SD Card Connector

J4 Pin	J4 Signal	SoM Interface Signal	SOM Pin	FPGA Pin
1	DAT2	SDMMC_D2	J1-E41	AA135
2	CD/DAT3	SDMMC_D3	J1-E42	V127
3	CMD	SDMMC_CMD	J1-D39	AB132
4	VDD	+3.3V		
5	CLK	SDMMC_CLK	J1-E47	D132
6	VSS	GND		
7	DAT0	SDMMC_D0	J1-D43	E135
8	DAT1	SDMMC_D1	J1-E44	F132
9	Switch (B)	GND		
10	Switch(A)	SDCARD_PRSNT (pulled to +1.8V, active low)	J1-E46	B134

USB 3.1 Gen 1 Type-C – J7

The MitySOM-A5E Development Board features a USB-C port J7. This interface is a USB 3.1 Gen 1 interface and supports up to 5Gbps throughput speeds and is backward compatible with USB 2.x USB-C devices. The port can supply a maximum of 1.5A of current at +5V and an overcurrent detection circuit monitors the output power. The pinout for J9 is included in Table 2.

Table 2 USB Type-C Connector Pin Out, J7

J9 Pin	J9 Signal
A1	GND
A2	TX1_P
A3	TX1_N
A4	VBUS
A5	CC1
A6	USB1_DATA_P
A7	USB1_DATA_N
A8	NC
A9	VBUS
A10	RX2_N
A11	RX2_P
A12	GND
B1	GND
B2	TX2_P
B3	TX2_N
B4	VBUS
B5	CC2
B6	USB1_DATA_P
B7	USB1_DATA_N
B8	NC
B9	VBUS
B10	RX1_N
B11	RX1_P
B12	GND

USB Type-C DRP Port Controller – U3

The DRP port controller (MPN: HD3SS3220IRNHR) manages mode configuration, the detection of a USB device, cable orientation detection, role detection and the required power supply for the connected device. All of these can be communicated back to the FPGA via the signals listed below.

Table 3: DRP Port Controller Signals

FPGA Side Signal	SOM Pin	FPGA Pin
USB1_SSTX_N	J1-B34	AR126
USB1_SSTX_P	J1-B35	AR129
I2C1_SDA	J1-A32	M127
I2C1_SCL	J1-A33	K127
USBC_ID_3V3	J1-C21	BP112
USB1_SSRX_N	J1-A44	AP133
USB1_SSRX_P	J1-A45	AP135
USBC_INT_3V3	J1-C22	BM112
USBC_FAULT_N	J1-C20	BK112
USBC_OR_3V3	J1-C18	BH118
USB1_MuxEnable_3V3	J1-G29	D34

USB 2.0 ULPI Transceiver for USB-C port – U4

The ULPI transceiver (MPN: USB3320C-EZK) provides support for the USB 2.0 data path on the Type-C connector supporting USB1 / USB 3.1 Data Rates.

Table 4: ULPI Transceiver Signals, U4

FPGA Sided Signal	SOM Pin	FPGA Pin
USB1_DATA0	J1-C33	AD135
USB1_DATA1	J1-D38	M132
USB1_DATA2	J1-E33	K132
USB1_DATA3	J1-D31	AG129
USB1_DATA4	J1-E38	J134
USB1_DATA5	J1-F32	AG120
USB1_DATA6	J1-F33	G134
USB1_DATA7	J1-E39	G135
USB1_DIR	J1-F37	J135
USB1_NXT	J1-D32	AD134
USB1_STP	J1-E37	L135
USB1_CLK	J1-E34	P132

USB 2.0 ULPI Transceiver for USB-C port – U9

The ULPI transceiver (MPN: USB3320C-EZK) provides support for the USB 2.0 data path that is leveraging the on-board USB 2.0 HUB, connected to the m.2 Type E Wifi interface card as well as the 3 Type A USB Host Ports.

Table 5: ULPI Transceiver Signals, U9

FPGA Sided Signal	SOM Pin	FPGA Pin
USB0_DATA0	J1-D30	AK115
USB0_DATA1	J1-E35	U134
USB0_DATA2	J1-D35	E134
USB0_DATA3	J1-D33	AG115
USB0_DATA4	J1-F36	N135
USB0_DATA5	J1-D34	AK120
USB0_DATA6	J1-D36	N134
USB0_DATA7	J1-C36	T132
USB0_DIR	J1-E36	W134
USB0_NXT	J1-C32	AL120
USB0_STP	J1-C37	U135
USB0_CLK	J1-D37	W135

Display Port Interface – J12

The MitySOM-A5E Development Board provides a 20-pin standard display port connector, J12. Supporting display port 1.4, the Agilex 5E can output up to a resolution of 8K at 60Hz.

Table 6: J12 Connector Pin Assignments

J10 Pin	Signal	Type	Standard	SOM Pin	FPGA Pin	Comments
1	DispPort Tx0_+	O	HCSL	J2-A02	BY7	
2	Shield	Power				
3	DispPort Tx0_-	O	HCSL	J2-A03	BY10	
4	DispPort Tx1_+	O	HCSL	J2-A06	BT7	
5	Shield	Power				
6	DispPort Tx1_-	O	HCSL	J2-A07	BT10	
7	DispPort Tx2_+	O	HCSL	J2-A10	BL7	
8	Shield	Power				
9	DispPort Tx2_-	O	HCSL	J2-A11	BL10	
10	DispPort Tx3_+	O	HCSL	J2-A14	BG7	
11	Shield	Power				
12	DispPort Tx3_-	O	HCSL	J2-A15	BG10	
13	TX_CONFIG1_3V3	I	LVCMOS	J1-B22	CK125	
14	Reserved	-				
15	AUX_CH_+	IO	LVDS	J1-B30, J1-A30, J1-A28, J1-B27	BR118, CA118. BW118, CL130	LVDS OE LVDS Out LVDS In LVCMOS IO*
16	Shield	Power				
17	AUX_CH_-	IO	LVDS	J1-B30, J1-A30, J1-A28, J1-B28	BR118, CA118. BW118, CL128	LVDS OE LVDS Out LVDS In LVCMOS IO*
18	TX_HPD_3V3	I	LVCMOS	J1-B23	CK128	Pulled up on board
19	GND	Power				
20	+3.3V	Power				

* on-board LVDS translator provided for AUX_CH P/N when in DisplayPort Mode. When in HDMI mode, CL130 and CK128 should be used with 3.3V logic for DDC interface. CL130 and CK128 should be tri-stated when using DisplayPort standard.

PCIe Edge Interface – P1

The MitySOM-A5E Development Board provides a standard x4 PCIe Edge Connector, P1. The interface will support PCIe Gen 4 speeds and can be used to interface to an external PCIe Host device using a riser cable or similar device. Note: The MitySOM-A5E DevKit Board cannot be powered via the P1 interface. External Power will be required and the grounds will be tied to the host via the riser cable interface. Contact Critical Link for information interfacing to this port.

Table 7 P1 Connector Pin Assignments

P1	Signal	Type	Standard	SOM Pin	FPGA Pin	Notes
A1	GND	Power				
B1	+12V	Power				Not Used
A2	+12V	Power				Not Used
B2	+12V	Power				Not Used
A3	+12V	Power				Not Used
B3	+12V	Power				Not Used
A4	GND	Power				
B4	GND	Power				
A5	JTAG_TCK	I				N/C
B5	PCIE_EDGE_SMBCLK	IO	LVCMOS/OD	J1-B25	CF128	
A6	JTAG_TDI	I				N/C
B6	PCIE_EDGE_SMBDAT	IO	LVCMOS/OD	J1-B24	CK134	
A7	JTAG_TDO	O				N/C
B7	GND	Power				
A8	JTAG_TMS	I				N/C
B8	+3.3V	Power				Not Used
A9	+3.3V	Power				Not Used
B9	JTAG_TRSTn	I				N/C
A10	+3.3V	Power				Not Used
B10	+3.3VAUX	Power				Not Used
A11	PCIE_EDGE_RESET_N	I	LVCMOS/OD	J1-A24	CH132	
B11	PCIE_EDGE_WAKE_N	O	LVCMOS/OD	J1-A23	CF132	
A12	GND	Power				
B12	RSVD1					N/C
A13	PCIE_CLK0_P	I	HCSL	J1-G16	BC111	
B13	GND	Power				
A14	PCIE_CLK0_N	I	HCSL	J1-G17	BC107	
B14	PCIE_RX0_P	I	HCSL	J1-F10	BV135	
A15	GND	Power				
B15	PCIE_RX0_N	I	HCSL	J1-F11	BV133	
A16	PCIE_TX0_P	O	HCSL	J1-H14	BY129	
B16	GND	Power				
A17	PCIE_TX0_N	O	HCSL	J1-H15	BY126	
B17	PCIE_EDGE_PRSNT#		LCVMOS/OD			Tied Low
A18	GND	Power				
B18	GND	Power				
A19	RSVD2					N/C
B19	PCIE_RX1_P	I	HCSL	J1-G08	BN135	
A20	GND	Power				
B20	PCIE_RX1_N	I	HCSL	J1-G09	BN133	
A21	PCIE_TX_1_P	O	HCSL	J1-H10	BT129	
B21	GND	Power				
A22	PCIE_TX1_N	O	HCSL	J1-H11	BT126	
B22	GND	Power				
A23	GND	Power				
B23	PCIE_RX2_P	I	HCSL	J1-F06	BJ135	
A24	GND	Power				
B24	PCIE_RX2_N	I	HCSL	J1-F07	BJ133	
A25	PCIE_TX2_P	O	HCSL	J1-H06	BL129	
B25	GND	Power				
A26	PCIE_TX_2_N	O	HCSL	J1-H07	BL126	
B26	GND	Power				
A27	GND	Power				
B27	PCIE_RX3_P	I	HCSL	J1-G04	BF135	
A28	GND	Power				
B28	PCIE_RX3_N	I	HCSL	J1-G05	BF133	
A29	PCIE_TX_3_P	O	HCSL	J1-H02	BG129	
B29	GND	Power				
A30	PCIE_TX_3_N	O	HCSL	J1-H03	BG126	
B30	RSVD3					N/C
A31	GND	Power				
B31	PCIE_EDGE_PRSNT#	O	LVCMOS/OD			Tied Low
A32	RSVD4					N/C

P1	Signal	Type	Standard	SOM Pin	FPGA Pin	Notes
B32	GND	Power				

SFP+ Interfaces – J5 and J6

The MitySOM-A5E Development Board provides two standard enhanced Small Form-factor Pluggable (SFP+) interface on J5 and J6. Several of the status GPIO pins on the SFP+ connectors are routed to an I2C port expander, U44 (PCAL6416PW118). U44 is configured for I2C address 0x20 on the I2C_EMAC2 HPS I2C Bus. Those connections are noted in the connector pin tables.

Table 8 J5 Connector Pin Assignments

J5	Signal	Type	Standard	SOM Pin	FPGA Pin	Notes
1	GND	Power				
2	SFP1_TX_FLT_3V3	I	LVCMOS			U44 P0[0] [1]
3	SFP1_TX_DIS_3V3	O	LVCMOS			U44 P0[1] [1]
4	SFP1_SDA_3V3	IO	LVCMOS	J1-A21	CD134	[1]
5	SFP1_SCL_3V3	IO	LVCMOS	J1-A29	CD135	[1]
6	SFP1_MOD0_PRSNT_N_3V3	I	LVCMOS			U44 P0[2] [1]
7	SFP1_RS0_3V3	O	LVCMOS			U44 P0[3] [1]
8	SFP1_LOS_3V3	I	LVCMOS			U44 P0[4] [1]
9	GND	Power				
10	GND	Power				
11	GND	Power				
12	SFP1_RX_-	I	HSSI / SFI	J1-A48	AK133	
13	SFP1_RX_+	I	HSSI / SFI	J1-A49	AK135	
14	GND	Power				
15	+3.3V	Power				
16	+3.3V	Power				
17	GND	Power				
18	SFP1_TX_+	O	HSSI / SFI	J1-B43	AL129	
19	SFP1_TX_-	O	HSSI / SFI	J1-B42	AL126	
20	GND	Power				

[1] Noted signals are pulled up to 3.3V using a 4.7K pullup resistor.

Table 9 J6 Connector Pin Assignments

J6	Signal	Type	Standard	SOM Pin	FPGA Pin	Notes
1	GND	Power				
2	SFP2_TX_FLT_3V3	I	LVCMOS			U44 P1[7] [1]
3	SFP2_TX_DIS_3V3	O	LVCMOS			U44 P1[6] [1]
4	SFP2_SDA_3V3	IO	LVCMOS	J1-A22	CG134	[1]
5	SFP2_SCL_3V3	IO	LVCMOS	J1-B26	CG135	[1]
6	SFP2_MOD0_PRSNT_N_3V3	I	LVCMOS			U44 P1[5] [1]
7	SFP2_RS0_3V3	O	LVCMOS			U44 P1[4] [1]
8	SFP2_LOS_3V3	I	LVCMOS			U44 P1[3] [1]
9	GND	Power				
10	GND	Power				
11	GND	Power				
12	SFP2_RX_-	I	HSSI / SFI	J1-B46	AM133	
13	SFP2_RX_+	I	HSSI / SFI	J1-B47	AM135	
14	GND	Power				
15	+3.3V	Power				
16	+3.3V	Power				
17	GND	Power				
18	SFP2_TX_+	O	HSSI / SFI	J1-B39	AN129	
19	SFP2_TX_-	O	HSSI / SFI	J1-B38	AN126	
20	GND	Power				

[1] Noted signals are pulled up to 3.3V using a 4.7K pullup resistor.

Camera MIPI Interfaces – J15, J16, J17, J18, and J20

The MitySOM-A5E Development Board provides 5 22-pin 0.5 mm pitch flat flex connectors, J15, J16, J17, J18, and J20 to interface with the Agilex 5E HSIO bank pins. J20 is connected to HSIO Bank 3A and requires special considerations as this bank is shared with the HPS DDR interface. J15, J16, J17, and J18 are connected to HSIO Bank 2B and are recommended when using MitySOM-A5E devices with Bank 2B IO available.

For all the camera ports, the I2C bus used for the command channel is HPS I2C_EMAC0. The SOM Pin and FPGA pins for the I2C bus pin multiplexer are noted in the tables below. The I2C bus is routed through a PCA9548APW I2C bridge chip. The bridge address / number for each camera interface is noted in the tables below.

Table 10: Camera MIPI Connector Pin Assignments (J15)

J15 Pin	Signal	Type	Standard	SOM Pin	FPGA Pin	Notes
1	+3.3V	Power	-			Max 500 mA
2	CAM2_SDA_3V3	I/O	LVCMOS/OD	J1-E49	F124	Bridge Offset 1
3	CAM2_SCL_3V3	I/O	LVCMOS/OD	J1-D47	D124	Bridge Offset 1
4	GND	Power	-			
5	CAM2_IO2_3V3	I/O	LVCMOS	J1-D19	BF115	
6	CAM2_IO1_3V3	I/O	LVCMOS	J1-D18	BE115	
7	GND	Power	-			
8	CSI2_RX3_P	I	DPHY_RX	J2-G41	CK11	
9	CSI2_RX3_N	I	DPHY_RX	J2-G40	CL8	
10	GND	Power	-			
11	CSI2_RX2_P	I	DPHY_RX	J2-F43	CL14	
12	CSI2_RX2_N	I	DPHY_RX	J2-F42	CL11	
13	GND	Power	-			
14	CSI2_RXCLK_P	I	DPHY_RX	J2-C39	CK17	
15	CSI2_RXCLK_N	I	DPHY_RX	J2-C40	CL17	
16	GND	Power	-			
17	CSI2_RX1_P	I	DPHY_RX	J2-F46	CL20	
18	CSI2_RX1_N	I	DPHY_RX	J2-F45	CK20	
19	GND	Power	-			
20	CSI2_RX0_P	I	DPHY_RX	J2-G43	CL23	
21	CSI2_RX0_N	I	DPHY_RX	J2-G44	CK26	
22	GND	Power	-			

Table 11: Camera MIPI Connector Pin Assignments (J16)

J16 Pin	Signal	Type	Standard	SOM Pin	FPGA Pin	Notes
1	+3.3V	Power	-			Max 500 mA
2	CAM1_SDA_3V3	I/O	LVCMOS/OD	J1-E49	F124	Bridge Offset 0
3	CAM1_SCL_3V3	I/O	LVCMOS/OD	J1-D47	D124	Bridge Offset 0
4	GND	Power	-			
5	CAM1_IO2_3V3	I/O	LVCMOS	J1-D22	BH109	
6	CAM1_IO1_3V3	I/O	LVCMOS	J1-D20	BF111	
7	GND	Power	-			
8	CSI1_RX3_P	I	DPHY_RX	J2-H48	CF22	
9	CSI1_RX3_N	I	DPHY_RX	J2-H47	CH22	
10	GND	Power	-			
11	CSI1_RX2_P	I	DPHY_RX	J2-G47	CC22	
12	CSI1_RX2_N	I	DPHY_RX	J2-G46	CA22	
13	GND	Power	-			
14	CSI1_RXCLK_P	I	DPHY_RX	J2-E46	CF28	
15	CSI1_RXCLK_N	I	DPHY_RX	J2-E47	CC28	
16	GND	Power	-			
17	CSI1_RX1_P	I	DPHY_RX	J2-F48	CA31	
18	CSI1_RX1_N	I	DPHY_RX	J2-F49	CC31	
19	GND	Power	-			
20	CSI1_RX0_P	I	DPHY_RX	J2-H49	CH31	
21	CSI1_RX0_N	I	DPHY_RX	J2-H50	CF31	
22	GND	Power	-			

Table 12: Camera MIPI Connector Pin Assignments (J17)

J17 Pin	Signal	Type	Standard	SOM Pin	FPGA Pin	Notes
1	+3.3V	Power	-			Max 500 mA
2	CAM3_SDA_3V3	I/O	LVCMOS/OD	J1-E49	F124	Bridge Offset 2
3	CAM3_SCL_3V3	I/O	LVCMOS/OD	J1-D47	D124	Bridge Offset 2
4	GND	Power	-			
5	CAM3_IO2_3V3	I/O	LVCMOS	J1-D25	BE111	
6	CAM3_IO1_3V3	I/O	LVCMOS	J1-D23	BF115	
7	GND	Power	-			
8	CSI3_RX3_P	I	DPHY_RX	J2-H44	BF50	
9	CSI3_RX3_N	I	DPHY_RX	J2-H45	BE50	
10	GND	Power	-			
11	CSI3_RX2_P	I	DPHY_RX	J2-D40	BF57	
12	CSI3_RX2_N	I	DPHY_RX	J2-D41	BF53	
13	GND	Power	-			
14	CSI3_RXCLK_P	I	DPHY_RX	J2-E40	BE61	
15	CSI3_RXCLK_N	I	DPHY_RX	J2-E41	BE57	
16	GND	Power	-			
17	CSI3_RX1_P	I	DPHY_RX	J2-D38	BE64	
18	CSI3_RX1_N	I	DPHY_RX	J2-D39	BF64	
19	GND	Power	-			
20	CSI3_RX0_P	I	DPHY_RX	J2-H39	BF68	
21	CSI3_RX0_N	I	DPHY_RX	J2-H38	BE68	
22	GND	Power	-			

Table 13: Camera MIPI Connector Pin Assignments (J18)

J18 Pin	Signal	Type	Standard	SOM Pin	FPGA Pin	Notes
1	+3.3V	Power	-			Max 500 mA
2	CAM4_SDA_3V3	I/O	LVCMOS/OD	J1-E49	F124	Bridge Offset 3
3	CAM4_SCL_3V3	I/O	LVCMOS/OD	J1-D47	D124	Bridge Offset 3
4	GND	Power	-			
5	CAM4_IO2_3V3	I/O	LVCMOS	J1-D27	BM109	
6	CAM4_IO1_3V3	I/O	LVCMOS	J1-C26	BR112	
7	GND	Power	-			
8	CSI4_RX3_P	I	DPHY_RX	J2-D45	BH38	
9	CSI4_RX3_N	I	DPHY_RX	J2-D44	BH41	
10	GND	Power	-			
11	CSI4_RX2_P	I	DPHY_RX	J2-F39	BP41	
12	CSI4_RX2_N	I	DPHY_RX	J2-F40	BM41	
13	GND	Power	-			
14	CSI4_RXCLK_P	I	DPHY_RX	J2-E43	BK49	
15	CSI4_RXCLK_N	I	DPHY_RX	J2-E42	BM49	
16	GND	Power	-			
17	CSI4_RX1_P	I	DPHY_RX	J2-H42	BH49	
18	CSI4_RX1_N	I	DPHY_RX	J2-H41	BH52	
19	GND	Power	-			
20	CSI4_RX0_P	I	DPHY_RX	J2-D47	BM52	
21	CSI4_RX0_N	I	DPHY_RX	J2-D46	BP52	
22	GND	Power	-			

Table 14: Camera MIPI Connector Pin Assignments (J20)

J20 Pin	Signal	Type	Standard	SOM Pin	FPGA Pin	Notes
1	+3.3V	Power	-			Max 500 mA
2	CAM5_SDA_3V3	I/O	LVCMOS/OD	J1-E49	F124	Bridge Offset 4
3	CAM5_SCL_3V3	I/O	LVCMOS/OD	J1-D47	D124	Bridge Offset 4
4	GND	Power	-			
5	CAM5_IO2_3V3	I/O	LVCMOS	J1-C27	BM118	
6	CAM5_IO1_3V3	I/O	LVCMOS	J1-C25	BK118	
7	GND	Power	-			
8	CSI5_RX3_P	I	DPHY_RX	J1-A18	Y95	
9	CSI5_RX3_N	I	DPHY_RX	J1-A17	Y98	
10	GND	Power	-			
11	CSI5_RX2_P	I	DPHY_RX	J1-B16	AC86	
12	CSI5_RX2_N	I	DPHY_RX	J1-B15	AC90	
13	GND	Power	-			
14	CSI5_RXCLK_P	I	DPHY_RX	J1-A15	AG93	
15	CSI5_RXCLK_N	I	DPHY_RX	J1-A14	AG90	
16	GND	Power	-			
17	CSI5_RX1_P	I	DPHY_RX	J1-B12	AC96	
18	CSI5_RX1_N	I	DPHY_RX	J1-B13	AC100	
19	GND	Power	-			
20	CSI5_RX0_P	I	DPHY_RX	J1-A11	AH104	
21	CSI5_RX0_N	I	DPHY_RX	J1-A12	AG100	
22	GND	Power	-			

10/100/1000 Ethernet Interface – J19

The MitySOM-A5E Development Board uses a DP83867ISRGZ SGMII PHY to provide an RJ-45 connection for a Gigabit 10/100/1000 Ethernet connection. This connection follows standard TIA/EIA-568B pin-out. By default, the Ethernet PHY will auto-negotiate with its link partner. The SGMII PHY is connected to soft CDR HSIO pins and HVIO pins as shown in the following table. The reference clock intended for the FPGA SGMII interface is generated by the onboard clock PLL and the interface pins are also identified in the table.

Table 15: SGMII / PHY Signal Connections

Signal	Type	SOM Pin	FPGA Pin
SGMII_RX_P	I	J1-G04	CK97
SGMII_RX_N	I	J1-G03	CL97
SGMII_TX_P	O	J1-H07	CK85
SGMII_TX_B	O	J1-H06	CL85
SGMII_REF_CLK_P	I	J1-D15	BW78
SGMII_REF_CLK_N	I	J1-D14	CA78
SGMII_MDIO*	I/O	J2-G10	CC92
SGMII_MDC*	O	J2-G09	CA92

*SGMII_MDIO and MDC pins have a 1.3V to 1.8V level translator inline to SGMII PHY.

JTAG Interface – J3

Table 16 lists the connections to the JTAG interface connector. The connector is intended to support standard Altera USB-Blaster II type JTAG pods.

Table 16 J3 JTAG Pin Assignments

Pin	Schematic Signal	J1 Pin	FPGA Pin	Type	Standard
1	TCK	H29	CA109	I	1.8 V LVCMOS
2	GND	-		Power	-
3	TDO	H30	BW109	O	1.8 V LVCMOS
4	+1.8V	-		Power	-
5	TMS	H31	CA112	I	1.8 V LVCMOS
6	N/C	-		-	-
7	N/C	-		-	-
8	N/C	-		-	-
9	TDI	H32	BW112	I	1.8 V LVCMOS
10	GND	-		Power	-

FMC Expansion Header – J13

The MitySOM-A5E provides an FMC expansion connector on the top of the board. An ASP-134486-01 connector is used and mates with TBD. 3.3V and +12V supply pins are provided on the connector to support powering external cards. All power to the FMC connector is gated by FMC_EN_3V3 which is tied to SOM pin (FPGA pin BU118, HVIO_5A_13). Table 17 provides signal descriptions for each pin.

Note: For all the GPIO pin pair (HA_XX_P/N pin pairs), the development board includes an array of high-speed analog multiplexer circuits that allow routing the pair to either an HVIO bank pin (for single ended 1.8V or 3.3V LVCMOS based on the FMC VADJ voltage) or an HSIO bank pin (for LVDS signaling). The intent is to support the full FMC electrical standard with the Agilex-5 IO restrictions.

Table 17: J3 Connector Pin Assignments

Pin	Schematic Signal	Type	Standard	SOM Pin	FPGA Pin	Notes
A1	GND	PWR	-		-	
A2	DP1_M2C_P	I	-	J2-G21	BD1	GTSR4B_RX_CH1P
A3	DP1_M2C_N	I	-	J2-G22	BD3	GTSR4B_RX_CH1N
A4	GND	PWR	-		-	
A5	GND	PWR	-		-	
A6	DP2_M2C_P	I	-	J2-G25	BB1	GTSR4B_RX_CH2P
A7	DP2_M2C_N	I	-	J2-G26	BB3	GTSR4B_RX_CH2N
A8	GND	PWR	-		-	
A9	GND	PWR	-		-	
A10	DP3_M2C_P	I	-	J2-G29	AY1	GTSR4B_RX_CH3P
A11	DP3_M2C_N	I	-	J2-G30	AY3	GTSR4B_RX_CH3N
A12	GND	PWR	-		-	
A13	GND	PWR	-		-	
A14	DP4_M2C_P	I	-	J2-B34	AV1	GTSR4C_RX_CH0P
A15	DP4_M2C_N	I	-	J2-B35	AV3	GTSR4C_RX_CH0N
A16	GND	PWR	-		-	
A17	GND	PWR	-		-	
A18	DP5_M2C_P	I	-	J2-B38	AT1	GTSR4C_RX_CH1P
A19	DP5_M2C_N	I	-	J2-B39	AT3	GTSR4C_RX_CH1N
A20	GND	PWR	-		-	
A21	GND	PWR	-		-	
A22	DP1_C2M_P	O	-	J2-H23	BC7	GTSR4B_TX_CH1P
A23	DP1_C2M_N	O	-	J2-H24	BC10	GTSR4B_TX_CH1N
A24	GND	PWR	-		-	
A25	GND	PWR	-		-	
A26	DP2_C2M_P	O	-	J2-H27	BA7	GTSR4B_TX_CH2P
A27	DP2_C2M_N	O	-	J2-H28	BA10	GTSR4B_TX_CH2N
A28	GND	PWR	-		-	
A29	GND	PWR	-		-	
A30	DP3_C2M_P	O	-	J2-H31	AW7	GTSR4B_TX_CH3P
A31	DP3_C2M_N	O	-	J2-H32	AW10	GTSR4B_TX_CH3N
A32	GND	PWR	-		-	
A33	GND	PWR	-		-	
A34	DP4_C2M_P	O	-	J2-A36	AU7	GTSR4C_TX_CH0P
A35	DP4_C2M_N	O	-	J2-A37	AU10	GTSR4C_TX_CH0N
A36	GND	PWR	-		-	
A37	GND	PWR	-		-	
A38	DP5_C2M_P	O	-	J2-A40	AR7	GTSR4C_TX_CH1P
A39	DP5_C2M_N	O	-	J2-A41	AR10	GTSR4C_TX_CH1N
A40	GND	PWR	-		-	
B1	N/C	-	-		-	
B2	GND	PWR	-		-	
B3	GND	PWR	-		-	
B4	N/C	-	-		-	
B5	N/C	-	-		-	
B6	GND	PWR	-		-	
B7	GND	PWR	-		-	
B8	N/C	-	-		-	
B9	N/C	-	-		-	
B10	GND	PWR	-		-	
B11	GND	PWR	-		-	
B12	DP7_M2C_P	I	-	J2-B46	AM1	GTSR4C_RX_CH3P
B13	DP7_M2C_N	I	-	J2-B47	AM3	GTSR4C_RX_CH3N
B14	GND	PWR	-		-	
B15	GND	PWR	-		-	
B16	DP6_M2C_P	I	-	J2-B42	AP1	GTSR4C_RX_CH2P
B17	DP6_M2C_N	I	-	J2-B43	AP3	GTSR4C_RX_CH2N
B18	GND	PWR	-		-	
B19	GND	PWR	-		-	
B20	GBTCLK1_M2C_P	I	LVDS	J2-C44	AT16	REFCLK_GTSR4C_RX_P
B21	GBTCLK1_M2C_N	I	LVDS	J2-C45	AT21	REFCLK_GTSR4C_RX_N
B22	GND	PWR	-		-	

Pin	Schematic Signal	Type	Standard	SOM Pin	FPGA Pin	Notes
B23	GND	PWR	-		-	
B24	N/C	-	-		-	
B25	N/C	-	-		-	
B26	GND	PWR	-		-	
B27	GND	PWR	-		-	
B28	N/C	-	-		-	
B29	N/C	-	-		-	
B30	GND	PWR	-		-	
B31	GND	PWR	-		-	
B32	DP7_C2M_P	O	-	J2-A48	AL7	GTSR4C_TX_CH3P
B33	DP7_C2M_N	O	-	J2-A49	AL10	GTSR4C_TX_CH3N
B34	GND	PWR	-		-	
B35	GND	PWR	-		-	
B36	DP6_C2M_P	O	-	J2-A44	AN7	GTSR4C_TX_CH2P
B37	DP6_C2M_N	O	-	J2-A45	AN10	GTSR4C_TX_CH2N
B38	GND	PWR	-		-	
B39	GND	PWR	-		-	
B40	N/C	-	-		-	
C1	GND	PWR	-		-	
C2	DP0_C2M_P	O	-	J2-H19	BE7	GTSR4B_TX_CH0P
C3	DP0_C2M_N	O	-	J2-H20	BE10	GTSR4B_TX_CH0N
C4	GND	PWR	-		-	
C5	GND	PWR	-		-	
C6	DP0_M2C_P	I	-	J2-G17	BF1	GTSR4B_RX_CH0P
C7	DP0_M2C_N	I	-	J2-G18	BF3	GTSR4B_RX_CH0N
C8	GND	PWR	-		-	
C9	GND	PWR	-		-	
C10	LA06_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-F17 J2-F15	BR22 CF71	HVIO_6A_13 (1.8 or 3.3V) HSIO_2A_T6_P
C11	LA06_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-D13 J2-F16	CH12 CH71	HVIO_6A_14 (1.8 or 3.3V) HSIO_2A_T6_N
C12	GND	PWR	-		-	
C13	GND	PWR	-		-	
C14	LA10_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-C13 J2-C19	BF21 BW69	HVIO_6B_1 (1.8 or 3.3V) HSIO_2A_T10_P
C15	LA10_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-F14 J2-C18	BE21 CA69	HVIO_6B_2 (1.8 or 3.3V) HSIO_2A_T10_N
C16	GND	PWR	-		-	
C17	GND	PWR	-		-	
C18	LA14_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-E09 J2-B20	BF16 BH62	HVIO_6B_11 (1.8 or 3.3V) HSIO_2A_T14_P
C19	LA14_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-E05 J2-B19	BH19 BH59	HVIO_6B_12 (1.8 or 3.3V) HSIO_2A_T14_N
C20	GND	PWR	-		-	
C21	GND	PWR	-		-	
C22	LA18_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-D06 J2-D21	CK4 BE79	HVIO_6B_19 (1.8 or 3.3V) HSIO_2A_T20_P
C23	LA18_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-D08 J2-D20	CH4 BE75	HVIO_6B_20 (1.8 or 3.3V) HSIO_2A_T20_N
C24	GND	PWR	-		-	
C25	GND	PWR	-		-	
C26	LA27_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-F23 J2-D11	J1 CA81	HVIO_6C_19 (1.8 or 3.3V) HSIO_2A_B14_P

Pin	Schematic Signal	Type	Standard	SOM Pin	FPGA Pin	Notes
C27	LA27_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-E26 J2-D12	G1 CC81	HVIO_6C_20 (1.8 or 3.3V) HSIO_2A_B14_N
C28	GND	PWR	-		-	
C29	GND	PWR	-		-	
C30	FMC_SCL	I/O	-	J1-A25	CF121	HVIO_5A_11 (3.3V)
C31	FMC_SDA	I/O	-	J1-C24	BE107	HVIO_5B_9 (3.3V)
C32	GND	PWR	-		-	
C33	GND	PWR	-		-	
C34	GND	PWR	-		-	
C35	+12V_FMC	PWR	-		-	
C36	GND	PWR	-		-	
C37	+12V_FMC	PWR	-		-	
C38	GND	PWR	-		-	
C39	+3.3V_FMC	PWR	-		-	
C40	GND	PWR	-		-	
D1	PG_C2M_3V3	PWR	-		-	
D2	GND	PWR	-		-	
D3	GND	PWR	-		-	
D4	GBTCLK0_M2C_P	I	LVDS	J2-H15	AY16	REFCLK_GTSR4B_RX_P
D5	GBTCLK0_M2C_N	I	LVDS	J2-H16	AY21	REFCLK_GTSR4B_RX_N
D6	GND	PWR	-		-	
D7	GND	PWR	-		-	
D8	LA01_CC_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-C05 J2-C21	BU28 CF59	HVIO_6A_1 (1.8 or 3.3V) HSIO_2A_T1_P
D9	LA01_CC_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-D14 J2-C22	BP31 CH59	HVIO_6A_2 (1.8 or 3.3V) HSIO_2A_T2_N
D10	GND	PWR	-			
D11	LA05_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-D12 J2-C16	BK28 CC71	HVIO_6A_11 (1.8 or 3.3V) HSIO_2A_T5_P
D12	LA05_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-C12 J2-C15	BR22 CA71	HVIO_6A_12 (1.8 or 3.3V) HSIO_2A_T5_N
D13	GND	PWR	-			
D14	LA09_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-E20 J2-A24	BK19 BU62	HVIO_6A_19 (1.8 or 3.3V) HSIO_2A_T9_P
D15	LA09_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-F19 J2-A23	CF9 BR62	HVIO_6A_20 (1.8 or 3.3V) HSIO_2A_T9_N
D16	GND	PWR	-			
D17	LA13_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-D09 J2-E17	BF32 BM59	HVIO_6B_7 (1.8 or 3.3V) HSIO_2A_T13_P
D18	LA13_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-E12 J2-E16	BF36 BK59	HVIO_6B_8 (1.8 or 3.3V) HSIO_2A_T13_N
D19	GND	PWR	-			
D20	LA17_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-C06 J2-A26	CK2 BH69	HVIO_6B_17 (1.8 or 3.3V) HSIO_2A_T17_P
D21	LA17_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-D05 J2-A27	CJ2 BH71	HVIO_6B_18 (1.8 or 3.3V) HSIO_2A_T17_N
D22	GND	PWR	-			
D23	LA23_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-F27 J2-E07	F8 BM78	HVIO_6C_11 (1.8 or 3.3V) HSIO_2A_B1_P
D24	LA23_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-F24 J2-E08	H8 BK78	HVIO_6C_12 (1.8 or 3.3V) HSIO_2A_B1_N
D25	GND	PWR	-			

Pin	Schematic Signal	Type	Standard	SOM Pin	FPGA Pin	Notes
D26	LA26_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-F22 J2-F05	G2 BK89	HVIO_6C_17 (1.8 or 3.3V) HSIO_2A_B4_P
D27	LA26_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-E23 J2-F06	J2 BM89	HVIO_6C_18 (1.8 or 3.3V) HSIO_2A_B4_N
D28	GND	PWR	-		-	
D29	N/C	-	-		-	
D30	N/C	-	-		-	
D31	N/C	-	-		-	
D32	+3.3V	PWR	-		-	
D33	N/C	-	-		-	
D34	N/C	-	-		-	
D35	GND	PWR	-		-	
D36	+3.3V_FMC	PWR	-		-	
D37	GND	PWR	-		-	
D38	+3.3V_FMC	PWR	-		-	
D39	GND	PWR	-		-	
D40	+3.3V_FMC	PWR	-		-	
E1	GND	PWR	-		-	
E2	N/C	-	-		-	
E3	N/C	-	-		-	
E4	GND	PWR	-		-	
E5	GND	PWR	-		-	
E6	N/C	-	-		-	
E7	N/C	-	-		-	
E8	GND	PWR	-		-	
E9	N/C	-	-		-	
E10	N/C	-	-		-	
E11	GND	PWR	-		-	
E12	N/C	-	-		-	
E13	N/C	-	-		-	
E14	GND	PWR	-		-	
E15	N/C	-	-		-	
E16	N/C	-	-		-	
E17	GND	PWR	-		-	
E18	N/C	-	-		-	
E19	N/C	-	-		-	
E20	GND	PWR	-		-	
E21	N/C	-	-		-	
E22	N/C	-	-		-	
E23	GND	PWR	-		-	
E24	N/C	-	-		-	
E25	N/C	-	-		-	
E26	GND	PWR	-		-	
E27	N/C	-	-		-	
E28	N/C	-	-		-	
E29	GND	PWR	-		-	
E30	N/C	-	-		-	
E31	N/C	-	-		-	
E32	GND	PWR	-		-	
E33	N/C	-	-		-	
E34	N/C	-	-		-	
E35	GND	PWR	-		-	
E36	N/C	-	-		-	
E37	N/C	-	-		-	
E38	GND	PWR	-		-	
E39	VADJ	PWR	-		-	1.8V, can be changed to +3.3
E40	GND	PWR	-		-	
F1	PMC_PG_M2C_3V3	PWR	-		-	
F2	GND	PWR	-		-	
F3	GND	PWR	-		-	
F4	N/C	-	-		-	

Pin	Schematic Signal	Type	Standard	SOM Pin	FPGA Pin	Notes
F5	N/C	-	-		-	
F6	GND	PWR	-		-	
F7	N/C	-	-		-	
F8	N/C	-	-		-	
F9	GND	PWR	-		-	
F10	N/C	-	-		-	
F11	N/C	-	-		-	
F12	GND	PWR	-		-	
F13	N/C	-	-		-	
F14	N/C	-	-		-	
F15	GND	PWR	-		-	
F16	N/C	-	-		-	
F17	N/C	-	-		-	
F18	GND	PWR	-		-	
F19	N/C	-	-		-	
F20	N/C	-	-		-	
F21	GND	PWR	-		-	
F22	N/C	-	-		-	
F23	N/C	-	-		-	
F24	GND	PWR	-		-	
F25	N/C	-	-		-	
F26	N/C	-	-		-	
F27	GND	PWR	-		-	
F28	N/C	-	-		-	
F29	N/C	-	-		-	
F30	GND	PWR	-		-	
F31	N/C	-	-		-	
F32	N/C	-	-		-	
F33	GND	PWR	-		-	
F34	N/C	-	-		-	
F35	N/C	-	-		-	
F36	GND	PWR	-		-	
F37	N/C	-	-		-	
F38	N/C	-	-		-	
F39	GND	PWR	-		-	
F40	VADJ	PWR	-		-	1.8V, can be changed to +3.3
G1	GND	PWR	-		-	
G2	N/C	-	-		-	
G3	N/C	-	-		-	
G4	GND	PWR	-		-	
G5	GND	PWR	-		-	
G6	LA00_CC_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-C14 J2-G11	BK31 BM71	HVIO_6A_9 (1.8 or 3.3V) HSIO_2A_T18_P
G7	LA00_CC_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-C11 J2-G12	BP22 BP71	HVIO_6A_10 (1.8 or 3.3V) HSIO_2A_T18_N
G8	GND	PWR	-		-	
G9	LA03_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-E14 J2-E21	BU31 CA62	HVIO_6A_5 (1.8 or 3.3V) HSIO_2A_T3_P
G10	LA03_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-F18 J2-E22	BM28 CC62	HVIO_6A_6 (1.8 or 3.3V) HSIO_2A_T3_N
G11	GND	PWR	-		-	
G12	LA08_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-E18 J2-F24	BM22 BU59	HVIO_6A_17 (1.8 or 3.3V) HSIO_2A_T8_P
G13	LA08_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-E16 J2-F23	CF12 BR59	HVIO_6A_18 (1.8 or 3.3V) HSIO_2A_T8_N
G14	GND	PWR	-		-	

Pin	Schematic Signal	Type	Standard	SOM Pin	FPGA Pin	Notes
G15	LA12_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-E13 J2-E19	BM22 BR69	HVIO_6B_5 (1.8 or 3.3V) HSIO_2A_T12_P
G16	LA12_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-F13 J2-E20	CF12 BU69	HVIO_6B_6 (1.8 or 3.3V) HSIO_2A_T12_N
G17	GND	PWR	-		-	
G18	LA16_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-D07 J2-B24	BU19 BM69	HVIO_6B_15 (1.8 or 3.3V) HSIO_2A_T16_P
G19	LA16_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-E04 J2-B25	BR19 BK69	HVIO_6B_16 (1.8 or 3.3V) HSIO_2A_T16_N
G20	GND	PWR	-		-	
G21	LA20_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-E30 J2-G14	H27 BF86	HVIO_6C_3 (1.8 or 3.3V) HSIO_2A_T22_P
G22	LA20_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-F29 J2-G13	D24 BE86	HVIO_6C_4 (1.8 or 3.3V) HSIO_2A_T22_N
G23	GND	PWR	-		-	
G24	LA22_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-E29 J2-E26	F18 BE96	HVIO_6C_7 (1.8 or 3.3V) HSIO_2A_T24_P
G25	LA22_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-F26 J2-E25	F15 BE93	HVIO_6C_8 (1.8 or 3.3V) HSIO_2A_T24_N
G26	GND	PWR	-		-	
G27	LA25_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-F25 J2-D08	F4 BM81	HVIO_6C_15 (1.8 or 3.3V) HSIO_2A_B3_P
G28	LA25_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-F21 J2-D09	K4 BP81	HVIO_6C_16 (1.8 or 3.3V) HSIO_2A_B3_N
G29	GND	PWR	-		-	
G30	LA29_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-G21 J2-F10	A11 BR81	HVIO_6D_3 (1.8 or 3.3V) HSIO_2A_B9_P
G31	LA29_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-G22 J2-F09	B11 BU81	HVIO_6D_4 (1.8 or 3.3V) HSIO_2A_B9_N
G32	GND	PWR	-		-	
G33	LA31_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-G24 J2-D04	A20 BR92	HVIO_6D_7 (1.8 or 3.3V) HSIO_2A_B11_P
G34	LA31_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-H20 J2-D05	A17 BU92	HVIO_6D_8 (1.8 or 3.3V) HSIO_2A_B11_N
G35	GND	PWR	-		-	
G36	LA33_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-E18 J2-E11	A35 CH78	HVIO_6D_15 (1.8 or 3.3V) HSIO_2A_B13_P
G37	LA33_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-E16 J2-E10	A33 CF78	HVIO_6D_16 (1.8 or 3.3V) HSIO_2A_B13_N
G38	GND	PWR	-		-	
G39	VADJ	PWR	-		-	1.8V, can be changed to +3.3
G40	GND	PWR	-		-	
H1	N/C	-	-		-	
H2	FMC_PRSNT_N_3V3	PWR	-		-	
H3	GND	PWR	-		-	
H4	N/C	-	-		-	
H5	N/C	-	-		-	
H6	GND	PWR	-		-	

Pin	Schematic Signal	Type	Standard	SOM Pin	FPGA Pin	Notes
H7	LA02_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-D10 J2-A21	BR28 CF62	HVIO_6A_3 (1.8 or 3.3V) HSIO_2A_T2_P
H8	LA02_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-F16 J2-A22	VR31 CH62	HVIO_6A_4 (1.8 or 3.3V) HSIO_2A_T2_P
H9	GND	PWR	-		-	
H10	LA04_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-E17 J2-F20	BW28 CH69	HVIO_6A_7 (1.8 or 3.3V) HSIO_2A_T4_P
H11	LA04_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-E15 J2-F19	BM31 CF69	HVIO_6A_8 (1.8 or 3.3V) HSIO_2A_T4_N
H12	GND	PWR	-		-	
H13	LA07_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-F15 J2-C25	BW19 BW59	HVIO_6A_15 (1.8 or 3.3V) HSIO_2A_T7_P
H14	LA07_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-E19 J2-C24	BH28 CA59	HVIO_6A_16 (1.8 or 3.3V) HSIO_2A_T7_N
H15	GND	PWR	-		-	
H16	LA11_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-C10 J2-D17	BE43 BR71	HVIO_6B_3 (1.8 or 3.3V) HSIO_2A_T11_P
H17	LA11_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-D11 J2-D18	BF40 BU71	HVIO_6B_4 (1.8 or 3.3V) HSIO_2A_T11_N
H18	GND	PWR	-		-	
H19	LA15_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-E08 J2-B21	BK22 BM62	HVIO_6B_13 (1.8 or 3.3V) HSIO_2A_T15_P
H20	LA15_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-C07 J2-B22	BM19 BP62	HVIO_6B_14 (1.8 or 3.3V) HSIO_2A_T15_N
H21	GND	PWR	-		-	
H22	LA19_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-F30 J2-B28	F27 BE83	HVIO_6C_1 (1.8 or 3.3V) HSIO_2A_T21_P
H23	LA19_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-F28 J2-B27	F24 BF83	HVIO_6C_2 (1.8 or 3.3V) HSIO_2A_T21_N
H24	GND	PWR	-		-	
H25	LA21_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-E31 J2-E24	H18 BF93	HVIO_6C_5 (1.8 or 3.3V) HSIO_2A_T23_P
H26	LA21_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-E27 J2-E23	D15 BF90	HVIO_6C_6 (1.8 or 3.3V) HSIO_2A_T23_N
H27	GND	PWR	-		-	
H28	LA24_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-E22 J2-F06	C2 BH81	HVIO_6C_13 (1.8 or 3.3V) HSIO_2A_B2_P
H29	LA24_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-E25 J2-F07	D4 BH78	HVIO_6C_14 (1.8 or 3.3V) HSIO_2A_B2_N
H30	GND	PWR	-		-	
H31	LA28_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-G20 J2-E14	A8 BR78	HVIO_6D_1 (1.8 or 3.3V) HSIO_2A_B8_P
H32	LA28_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-H18 J2-E13	B4 BU78	HVIO_6D_2 (1.8 or 3.3V) HSIO_2A_B8_N
H33	GND	PWR	-		-	

Pin	Schematic Signal	Type	Standard	SOM Pin	FPGA Pin	Notes
H34	LA30_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-G23 J2-C10	B14 BW89	HVIO_6D_5 (1.8 or 3.3V) HSIO_2A_B10_P
H35	LA30_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-H19 J2-C09	A14 CA89	HVIO_6D_6 (1.8 or 3.3V) HSIO_2A_B10_N
H36	GND	PWR	-		-	
H37	LA32_P	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-H23 J2-C07	B30 BR89	HVIO_6D_13 (1.8 or 3.3V) HSIO_2A_B12_P
H38	LA32_N	I/O	1.8V/ 3.3V LVCMOS / LVDS	J1-H25 J2-C06	A30 BU89	HVIO_6D_14 (1.8 or 3.3V) HSIO_2A_B12_N
H39	GND	PWR	-		-	
H40	VADJ	PWR	-		1.8V	1.8V, can be changed to +3.3
J1	GND	PWR	-		-	
J2	N/C	-	-		-	
J3	N/C	-	-		-	
J4	GND	PWR	-		-	
J5	GND	PWR	-		-	
J6	N/C	-	-		-	
J7	N/C	-	-		-	
J8	GND	PWR	-		-	
J9	N/C	-	-		-	
J10	N/C	-	-		-	
J11	GND	PWR	-		-	
J12	N/C	-	-		-	
J13	N/C	-	-		-	
J14	GND	PWR	-		-	
J15	N/C	-	-		-	
J16	N/C	-	-		-	
J17	GND	PWR	-		-	
J18	N/C	-	-		-	
J19	N/C	-	-		-	
J20	GND	PWR	-		-	
J21	N/C	-	-		-	
J22	N/C	-	-		-	
J23	GND	PWR	-		-	
J24	N/C	-	-		-	
J25	N/C	-	-		-	
J26	GND	PWR	-		-	
J27	N/C	-	-		-	
J28	N/C	-	-		-	
J29	GND	PWR	-		-	
J30	N/C	-	-		-	
J31	N/C	-	-		-	
J32	GND	PWR	-		-	
J33	N/C	-	-		-	
J34	N/C	-	-		-	
J35	GND	PWR	-		-	
J36	N/C	-	-		-	
J37	N/C	-	-		-	
J38	GND	PWR	-		-	
J39	FMC_VIO_B_M2C	PWR	-		-	
J40	GND	PWR	-		-	
K1	N/C	-	-		-	
K2	GND	PWR	-		-	
K3	GND	PWR	-		-	
K4	N/C	-	-		-	
K5	N/C	-	-		-	
K6	GND	PWR	-		-	
K7	N/C	-	-		-	
K8	N/C	-	-		-	
K9	GND	PWR	-		-	

Pin	Schematic Signal	Type	Standard	SOM Pin	FPGA Pin	Notes
K10	N/C	-	-		-	
K11	N/C	-	-		-	
K12	GND	PWR	-		-	
K13	N/C	-	-		-	
K14	N/C	-	-		-	
K15	GND	PWR	-		-	
K16	N/C	-	-		-	
K17	N/C	-	-		-	
K18	GND	PWR	-		-	
K19	N/C	-	-		-	
K20	N/C	-	-		-	
K21	GND	PWR	-		-	
K22	N/C	-	-		-	
K23	N/C	-	-		-	
K24	GND	PWR	-		-	
K25	N/C	-	-		-	
K26	N/C	-	-		-	
K27	GND	PWR	-		-	
K28	N/C	-	-		-	
K29	N/C	-	-		-	
K30	GND	PWR	-		-	
K31	N/C	-	-		-	
K32	N/C	-	-		-	
K33	GND	PWR	-		-	
K34	N/C	-	-		-	
K35	N/C	-	-		-	
K36	GND	PWR	-		-	
K37	N/C	-	-		-	
K38	N/C	-	-		-	
K39	GND	PWR	-		-	
K40	FMC_VIO_B_M2C	PWR	-		-	

FMC HSIO / HVIO Mux Table

To support compatibility with the FMC standard, the system must support running either LVDS or single ended electrical standards to the LA_XX GPIO signals on the connector. The MitySOM-A5E Development Kit board meets this requirement by providing an array of analog muxes to route each pairing of LA_XX signals to either an HVIO bank (referencing the VADJ level of either 1.8V or 3.3V) or an HSIO bank (referencing the 1.3V IO to support true differential signaling / LVDS) as shown in Figure 2.

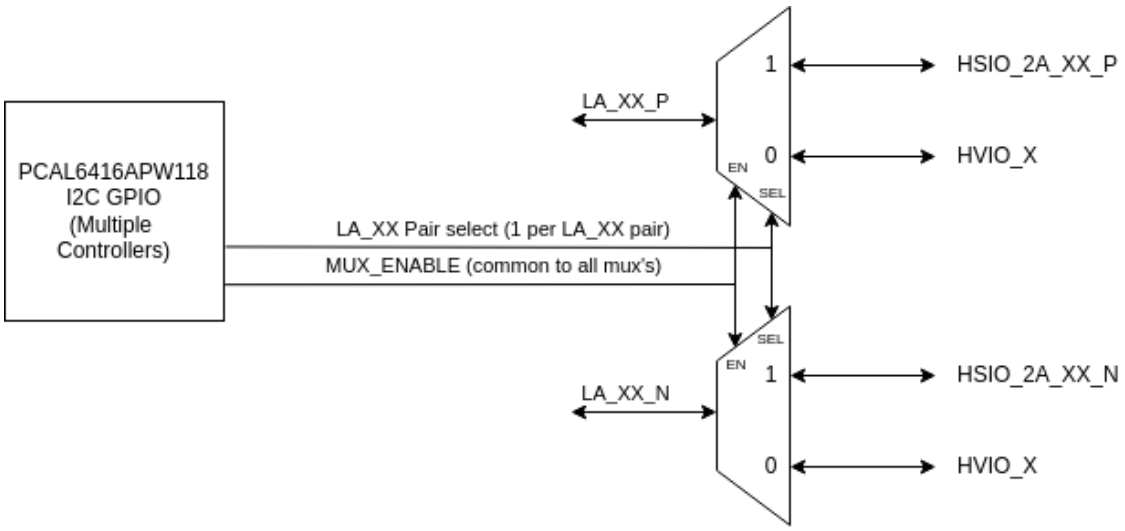

Figure 2 FMC LA_XX signal pair routing to HSIO or HVIO bank pins.

Table 18: FMC HVIO/HSIO Mux Controls

FMC Pair	MUX Net	I2C BUS	I2C ADDR	PORT
ALL	FMX_MUX_EN	I2C_EMAC2	0x20	P0[5]
LA00	FMC_SEL_10	I2C_EMAC1	0x20	P1[1]
LA01	FMC_SEL_11	I2C_EMAC1	0x20	P1[2]
LA02	FMC_SEL_6	I2C_EMAC1	0x20	P0[5]
LA03	FMC_SEL_7	I2C_EMAC1	0x20	P0[6]
LA04	FMC_SEL_25	I2C_EMAC2	0x21	P1[0]
LA05	FMC_SEL_12	I2C_EMAC1	0x20	P1[3]
LA06	FMC_SEL_1	I2C_EMAC1	0x20	P0[0]
LA07	FMC_SEL_26	I2C_EMAC2	0x21	P1[1]
LA08	FMC_SEL_8	I2C_EMAC1	0x20	P0[7]
LA09	FMC_SEL_13	I2C_EMAC1	0x20	P1[4]
LA10	FMC_SEL_2	I2C_EMAC1	0x20	P0[1]
LA11	FMC_SEL_27	I2C_EMAC2	0x21	P1[2]
LA12	FMC_SEL_18	I2C_EMAC2	0x21	P0[1]
LA13	FMC_SEL_14	I2C_EMAC1	0x20	P1[5]
LA14	FMC_SEL_3	I2C_EMAC1	0x20	P0[2]
LA15	FMC_SEL_28	I2C_EMAC2	0x21	P1[3]
LA16	FMC_SEL_17	I2C_EMAC2	0x21	P0[0]
LA17	FMC_SEL_15	I2C_EMAC1	0x20	P1[6]
LA18	FMC_SEL_4	I2C_EMAC1	0x20	P0[3]
LA19	FMC_SEL_29	I2C_EMAC2	0x21	P1[4]
LA20	FMC_SEL_19	I2C_EMAC2	0x21	P0[2]
LA21	FMC_SEL_30	I2C_EMAC2	0x21	P1[5]
LA22	FMC_SEL_20	I2C_EMAC2	0x21	P0[3]
LA23	FMC_SEL_16	I2C_EMAC1	0x20	P1[7]
LA24	FMC_SEL_31	I2C_EMAC2	0x21	P1[6]
LA25	FMC_SEL_21	I2C_EMAC2	0x21	P0[4]
LA26	FMC_SEL_5	I2C_EMAC1	0x20	P0[4]
LA27	FMC_SEL_9	I2C_EMAC1	0x20	P1[0]
LA28	FMC_SEL_32	I2C_EMAC2	0x21	P1[7]
LA29	FMC_SEL_22	I2C_EMAC2	0x21	P0[5]
LA30	FMC_SEL_33	I2C_EMAC2	0x20	P1[0]
LA31	FMC_SEL_23	I2C_EMAC2	0x21	P0[6]
LA32	FMC_SEL_34	I2C_EMAC2	0x20	P1[1]
LA33	FMC_SEL_24	I2C_EMAC2	0x21	P0[7]
CLK1_M2C	FMC_SEL_35	I2C_EMAC2	0x20	P1[2]
CLK0_M2C	FMC_SEL_36	I2C_EMAC2	0x20	P0[7]

M.2 M Type Key Interface (J10)

The MitySOM-A5E Development Board M Key Connector pinout is listed in Table 19.

Table 19: M.2 NVME / M Type Key Connector Pin Assignments (J10)

J10 Pin	Signal	Type	Standard	SOM Pin	FPGA Pin	Notes
1	GND	PWR	-	-	-	
2	+3.3V	PWR	-	-	-	
3	GND	PWR	-	-	-	
4	+3.3V	PWR	-	-	-	
5	PERn3	I	HCSL	J1-A40	AV133	GTSL1B_RX_CH3_N
6	NC	-	-	-	-	
7	PERp3	I	HCSL	J1-A41	AV135	GTSL1B_RX_CH3_P
8	NC	-	-	-	-	
9	GND	PWR	-	-	-	
10	DAS/DSS#	OD	-	-	-	Connected to D10
11	PETn3	O	HCSL	J1-H48	AW126	GTSL1B_TX_CH3_N
12	+3.3V	PWR	-	-	-	
13	PETp3	O	HCSL	J1-H49	AW129	GTSL1B_TX_CH3_P
14	+3.3V	PWR	-	-	-	
15	GND	PWR	-	-	-	
16	+3.3V	PWR	-	-	-	
17	PERn2	I	HCSL	J1-G42	AY133	GTSL1B_RX_CH2_N
18	NC	-	-	-	-	
19	PERp2	I	HCSL	J1-G43	AY135	GTSL1B_RX_CH2_P
20	NC	-	-	-	-	
21	GND	PWR	-	-	-	
22	NC	-	-	-	-	
23	PETn2	O	HCSL	J1-H44	BA126	GTSL1B_TX_CH2_N
24	NC	-	-	-	-	
25	PETp2	O	HCSL	J1-H45	BA129	GTSL1B_TX_CH2_P
26	NC	-	-	-	-	
27	GND	PWR	-	-	-	
28	NC	-	-	-	-	
29	PERn1	I	HCSL	J1-A36	BB133	GTSL1B_RX_CH1_N
30	NC	-	-	-	-	
31	PERp1	I	HCSL	J1-A37	BB135	GTSL1B_RX_CH1_P
32	NC	-	-	-	-	
33	GND	PWR	-	-	-	
34	NC	-	-	-	-	
35	PETn1	O	HCSL	J1-H40	BC126	GTSL1B_TX_CH1_N
36	NC	-	-	-	-	
37	PETp1	O	HCSL	J1-H41	BC129	GTSL1B_TX_CH1_P
38	NC	-	-	-	-	
39	GND	PWR	-	-	-	
40	SMB_CLK	O	1.8V	J1-F40	Y132	I2C_EMAC2_SCL
41	PERn0	I	HCSL	J1-G38	BD133	GTSL1B_RX_CH0_N
42	SMB_DATA	IO	1.8V	J1-D44	T127	I2C_EMAC2_SDA
43	PERp0	I	HCSL	J1-G39	BD135	GTSL1B_RX_CH0_P
44	NC	-	-	-	-	
45	GND	PWR	-	-	-	
46	NC	-	-	-	-	
47	PETn0	O	HCSL	J1-H36	BE126	GTSL1B_TX_CH0_N
48	NC	-	-	-	-	
49	PETp0	O	HCSL	J1-H37	BE129	GTSL1B_TX_CH0_P
50	PERST#	O	3.3V	J1-D24	BU109	PIN_PERST_N_VCP_L1B_1
51	GND	PWR	-	-	-	
52	CLKREQ	I	3.3V	-	-	Pullup to 3.3V
53	REFCLKN	O	HCSL	-	-	
54	PEWake#	I	3.3V	J1-C23	BR109	HVIO_5B_8
55	REFCLKP	O	HCSL			
56	NC	-	-	-	-	
57	GND	PWR	-	-	-	
58	NC	-	-	-	-	
KEY	KEY	KEY	KEY	KEY	KEY	KEY
59	NC	-	-	-	-	
60	NC	-	-	-	-	
61	PEDET	I	3.3V	-	-	Pullup to 3.3V
62	+3.3V	PWR	-	-	-	
63	GND	PWR	-	-	-	

64	+3.3V	PWR	-	-	-	
65	GND	PWR	-	-	-	
66	+3.3V	PWR	-	-	-	
67	GND	PWR	-	-	-	

M.2 E Type Key Interface (J11)

The MitySOM-A5E Development Board E Key Connector pinout is listed below.

Table 20: M.2 NVME / E Type Key Connector Pin Assignments (J11)

J10 Pin	Signal	Type	Standard	SOM Pin	FPGA Pin	Notes
1	GND	PWR	-	-	-	
2	+3.3V	PWR	-	-	-	
3	USB_D+	IO	USB 2.0	-	-	Connected to USB HUB
4	+3.3V	PWR	-	-	-	
5	USB_D-	IO	USB 2.0	-	-	Connected to USB HUB
6	LED1#	I	-	-	-	Connected to D25
7	GND	PWR	-	-	-	
8	NC	-	-	-	-	
9	NC	-	-	-	-	
10	NC	-	-	-	-	
11	NC	-	-	-	-	
12	NC	-	-	-	-	
13	NC	-	-	-	-	
14	NC	-	-	-	-	
15	NC	-	-	-	-	
16	NC	-	-	-	-	
17	NC	-	-	-	-	
18	GND	PWR	-	-	-	
19	NC	-	-	-	-	
20	UART_WAKE	I	3.3V	-	-	Pulled to +3.3V R224.
21	NC	-	-	-	-	
22	UART_TXD	I	1.8V	J2-F13	CH92	HSIO_2A_B17_N (1.3V)
23	NC	-	-	-	-	
24	KEY	KEY	KEY	KEY	KEY	
25	KEY	KEY	KEY	KEY	KEY	
26	KEY	KEY	KEY	KEY	KEY	
27	KEY	KEY	KEY	KEY	KEY	
28	KEY	KEY	KEY	KEY	KEY	
29	KEY	KEY	KEY	KEY	KEY	
30	KEY	KEY	KEY	KEY	KEY	
31	KEY	KEY	KEY	KEY	KEY	
32	UART_RXD	O	1.8V	J2-D06	CF89	HSIO_2A_B16_N (1.3V)
33	GND	PWR	-	-	-	
34	UART_RTS	I	1.8V	J2-D07	CH89	HSIO_2A_B16_P (1.3V)
35	PETp0	O	HCSL	J1-G35	AU129	GTSL1C_TX_CH0_P
36	UART_CTS	O	1.8V	J2-C12	CF81	HSIO_2A_B15_P (1.3V)
37	PETn0	O	HCSL	J1-G34	AE126	GTSL1C_TX_CH0_N
38	NC	-	-	-	-	
39	GND	PWR	-	-	-	
40	NC	-	-	-	-	
41	PERp0	I	HCSL	J1_G47	AT135	GTSL1C_RX_CH0_P
42	NC	-	-	-	-	
43	PERn0	I	HCSL	J1-G46	AT133	GTSL1C_RX_CH0_N
44	NC	-	-	-	-	
45	GND	PWR	-	-	-	
46	NC	-	-	-	-	
47	REFCLKp0	O	HCSL	-	-	
48	NC	-	-	-	-	
49	REFCLKn0	O	HCSL	-	-	
50	SUSCLK	O	3.3V	-	-	32KHz
51	GND	PWR	-	-	-	
52	PERST0#	O	3.3V	J1-D21	BF104	PIN_PERST_N_CVP_L1C_1
53	CLKREQ0#	I	3.3V	-	-	Pulled up R189
54	W_DISABLE2#	O	3.3V	-	-	Pulled up R191
55	PEWAKE0#	I	3.3V	J1-D26	BK109	HVIO_5B_10
56	W_DISABLE1#	O	3.3V	-	-	Pulled up R192
57	GND	PWR	-	-	-	
58	I2C_DATA	IO	1.8V	J1-D44	T127	I2C_EMAC2_SDA
59	NC	-	-	-	-	
60	I2C_CLK	O	1.8V	J1-F40	Y132	I2C_EMAC2_SCL
61	NC	-	-	-	-	
62	NC	-	-	-	-	
63	GND	PWR	-	-	-	
64	NC	-	-	-	-	

65	NC	-	-	-	-	
66	NC	-	-	-	-	
67	NC	-	-	-	-	
68	NC	-	-	-	-	
69	GND	PWR	-	-	-	
70	NC	-	-	-	-	
71	NC	-	-	-	-	
72	+3.3V	PWR	-	-	-	
73	NC	-	-	-	-	
74	+3.3V	PWR	-	-	-	
75	GND	PWR	-	-	-	

Debug Buttons and LEDS

The MitySOM-A5E Development Board includes 2 momentary contact pushbuttons that may be used for user applications and debug. Each button output to the SOM is pulled up to 3.3V and a button press will ground the signal. There are also 2 LEDs that can be driven by the SOM FPGA IO. The FPGA controls are active high to enable the LED.

Table 21 Pushbutton and debug LED pin assignments

Description	Net Name	J1 Pin	Type	Standard	Notes
DEBUG1 Pushbutton / S4	HVIO_6D_17	G28	I	3.3V LVCMOS	Active low when pressed.
DEBUG2 Pushbutton / S5	HVIO_6D_18	G27	I	3.3V LVCMOS	Active low when pressed.
Debug LED 1 / D18	HVIO_6D_20	H22	O	3.3V LVCMOS	Active High to enable LED.
Debug LED 2 / D19	HVIO_6D_19	G26	O	3.3V LVCMOS	Active High to enable LED.

INCLUDED COMPONENTS

The following table lists the components that are included with a MitySOM-A5E Development Kit. See Table 23 for specific ordering information.

Table 22 Included Items

Description	Interface Port	Qty. Included
MitySOM-A5E Development Board	N/A	Qty. 1
MitySOM-A5E Module		Qty. 1
12V 7.5A AC to DC Supply		Qty. 1
Ethernet cable – 7 foot		Qty. 1
USB-A to MicroUSB cable		Qty. 1
Fan +12V heat sink and FPGA package clip		Qty. 1
MicroSD Card		Qty. 1

MitySOM-A5E DEVELOPMENT KIT ORDERING INFORMATION

The following table lists the standard MitySOM-A5E Development Kit configurations. For shipping status, availability, and lead time of these or other configurations please contact Critical Link at info@criticallink.com.

Table 23 MitySOM-A5E Development Kit Model Numbers

Dev Kit P/N	Module Included	XCVR	Speed Grade	FPGA Size	HPS RAM Size	FPGA RAM Size	On-board Flash	Operating Temp
80-001854	A5ED-B64-144-SRI	24	4	656 KLE	4GB	4GB	32MB	-40ºC to +85º C
80-001855	A5ED-B46-144-SRI	16	6	434 KLE	4GB	4GB	32MB	-40ºC to +85º C

MECHANICAL INTERFACE DESCRIPTION

Main Board Interface / Mounting

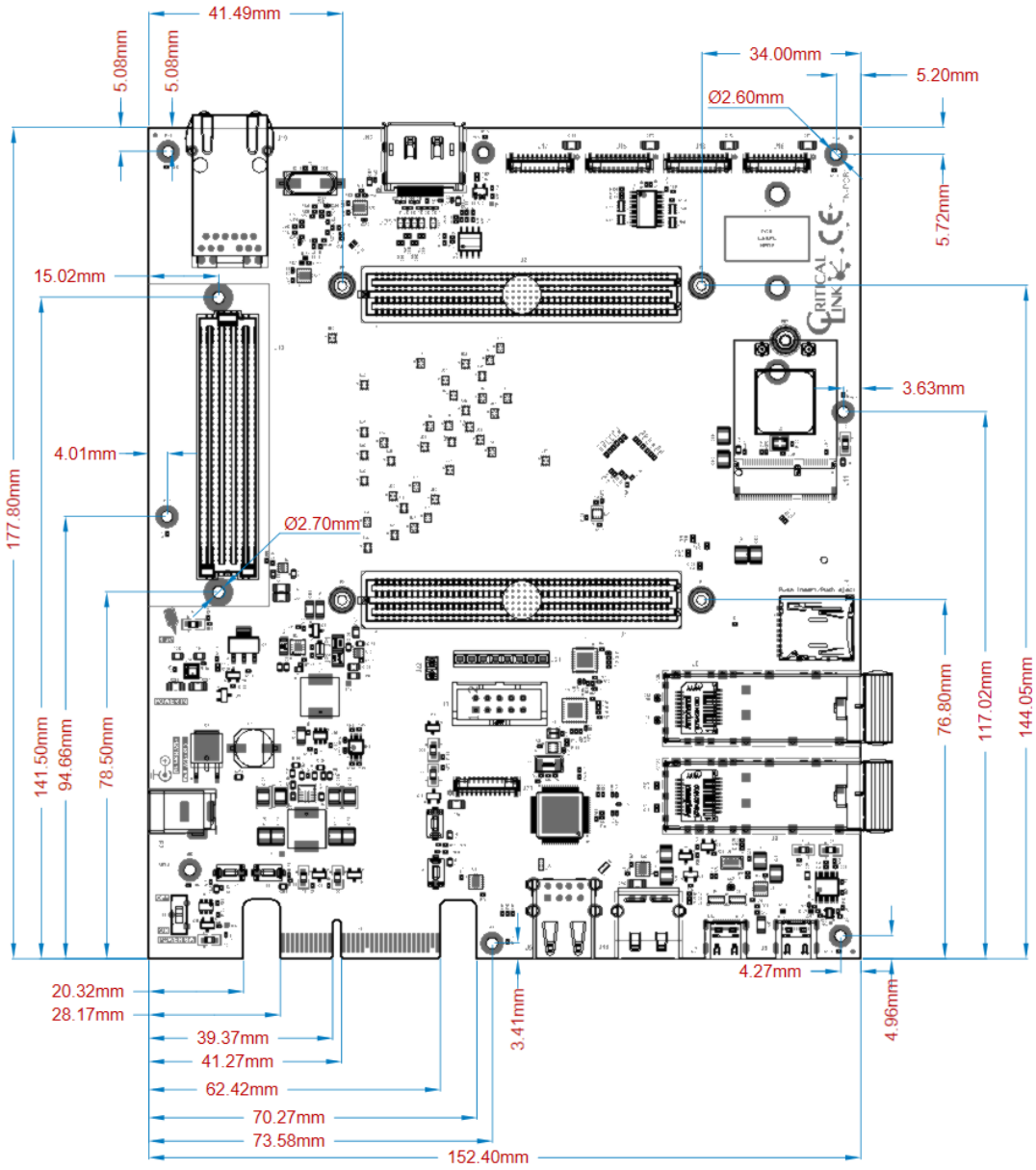

Figure 3: MitySOM-A5E Development Kit Outline and Mounting Hole Locations (Top View)

REVISION HISTORY

Date	Rev	Change Description
09-July-2025	1A	Initial revision.