

FEATURES

- **Agilex 5 E-Series FPGA / Processor from Altera**
 - Device Group A or B support
 - Up to Quad Hard Processor System
 - Dual core Cortex-A76@1.4/1.8 GHz*
 - 64 KB L1 Instruction Cache
 - 64 KB L1 Data Cache
 - 256 KB L2 Unified Cache
 - Dual core Cortex-A55@1.2/1.5 GHz*
 - 64 KB L1 Instruction Cache
 - 64 KB L1 Data Cache
 - 128 KB L2 Unified Cache
 - 2 MB L3 Cache (Shared)
 - 512 KB on-chip RAM
- **Memory**
 - Up to 8 GB LPDDR4
 - 32 bits wide
 - 14.9/10.6 GB/sec burst rate*
 - Shared between FPGA and HPS
 - 32 MB QSPI Configuration FLASH
- **FPGA Fabric**
 - Up To 656K Logic Elements (LE)
 - Up to 1 GHz Clock Routing
 - Up To 31.4 Mb M20K Memory
 - Up to 6.8 Mb MLAB Memory
 - Up To 1692 Fixed Point Multipliers
 - Up to 26/22 TOPS w/AI Tensor Blocks*
 - 32 Global Clock Networks
- **FPGA IO**
 - 120 User FPGA HVIO Pins
 - 1.8/2.5/3.3V CMOS
 - 24 User FPGA HSIO Pins
 - 1.1V Single Ended
 - Biased LVDS
 - MIPI D-PHY to 3.5/2.5 Gbps*
 - 48 HPS IO Pins
 - Up to 12 Transceiver Pairs
- **Serial Transceivers**
 - Up to twelve at 28.1/17.16 Gbps*
 - Up to three x4 PCIe 4.0 Hard IP Blocks, End Point or Root Port
 - 25/10 GbE MAC*, PCS, FEC

* Dual parameters above represent Agilex 5E Device Group A vs Device Group B specified performance; Critical Link offers options for both device groups.



- **Mechanical**
 - 70.25mm (2.76") x 50.8mm (2") size
 - 400 pin board to board connector
- **Hard Processor System (HPS) IO**
 - Up to 3 10/100/1000/2500 Mbps Ethernet MACs with TSN Support
 - 1 USB 2.0 On-The-Go (OTG) Port
 - 1 USB 3.1 Gen 1 Superspeed Port
 - 2 UARTs
 - 1 MMC/SD/SDIO
 - 2 SPI Masters and 2 SPI Slaves
 - 5 I2C controllers
 - 2 I3C controllers
- Integrated Power Management
- Power, Reset and Clock Management
- Integrated Secure Device Manager with encryption acceleration.

APPLICATIONS

- Robotics
- Image Processing
- Test and Measurement
- Embedded AI processing
- Embedded Instrumentation
- Industrial Automation and Control
- Industrial Instrumentation
- Medical Instrumentation

BENEFITS

- Rapid Development / Deployment
- Multiple Connectivity and I/O Options
- Rich User Interfaces
- High System Integration
- Supports Altera FPGA AI Suite
- Supports HLS acceleration
- High Level OS Support
 - Embedded Linux

DESCRIPTION

The MitySOM-A5E is a highly configurable, small form-factor System-on-Module (SOM) featuring an Agilex 5 SoC FPGA E-Series from Altera. In addition to the processor, the module includes on-board power supplies, an LPDDR4 RAM memory subsystem, and SPI NOR Flash configuration memory. The MitySOM-A5E provides a complete and flexible CPU infrastructure for highly integrated embedded systems.

The MitySOM-A5E is available with up to a 656K Logic Element (KLE) Agilex 5E which provides a Quad Core Hard Processor Subsystem (HPS) including a dual-core Cortex-A76 and a dual-core Cortex-A55. Options for 85, 138, 282, 434, and 524 KLE devices are also possible. The HPS can run a rich set of real-time operating systems containing software applications programming interfaces (APIs) expected by modern system designers. The ARM architecture supports several operating systems, including Linux.

Figure 1 illustrates a block diagram of the MitySOM-A5E. As shown in the figure, the primary interface to the MitySOM-A5E is through a 400 Pin vertical board-to-board mezzanine connector. The MitySOM-A5E is intended to interface to a carrier card base module for applications development. Details of the board-to-board interfaces are included in the Interface Description section.

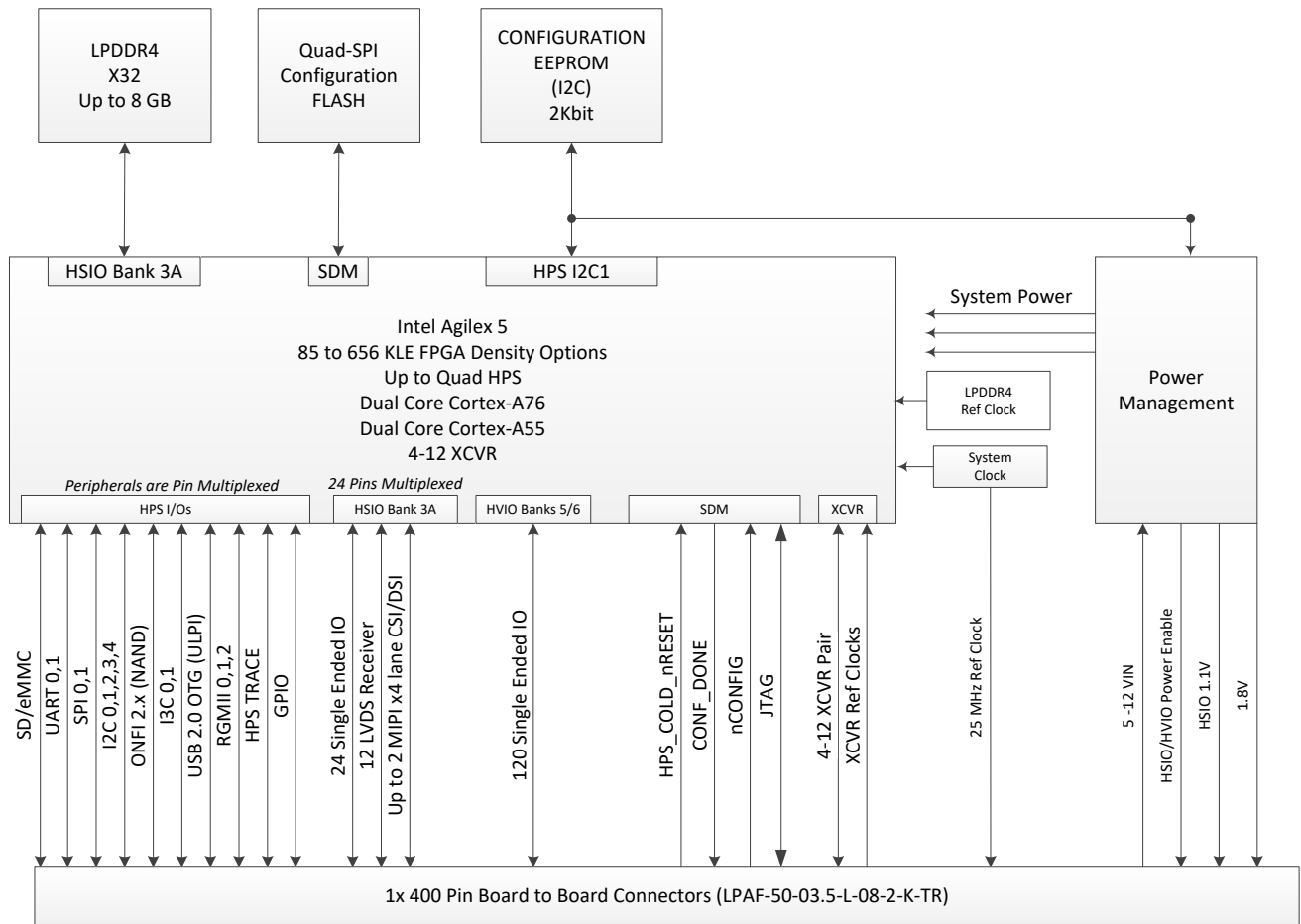


Figure 1 MitySOM-A5E Block Diagram

LPDDR4 Memory – HPS Shared Memory

The MitySOM-A5E includes a dedicated 32-bit LPDDR4 memory interface that can address a maximum of 8GB of RAM. This LPDDR4 memory is available for both the HPS as well as the FPGA fabric through an AXI high speed interface internal to the Agilex 5E.

The MitySOM-A5E family adheres to Altera’s Agilex 5E maximum memory speeds. The HPS memory is clocked at 1333Mhz by default.

HPS-FPGA AXI

The high bandwidth HPS-FPGA AXI bridges provided by Altera in the Agilex 5E SoC allow masters in the FPGA fabric to communicate with slaves in the HPS logic and vice versa. These bridges can be configured for 32, 64, or 128 bit widths.

For example, designers can instantiate additional memories or peripherals in the FPGA fabric, and master interfaces belonging to components in the HPS logic can access them. Designers can also instantiate components such as a Nios® V processor in the FPGA fabric and their master interfaces can access memories or peripherals in the HPS logic, including LPLPDDR4 Memory – HPS Shared Memory.

Configuration EEPROM

MitySOM-A5E modules contain a 2048 x 8-bit EEPROM that is used to hold factory configuration data for the module. The EEPROM is connected to the Agilex 5E using the HPS I2C1 interface. This EEPROM contains information such as the module type, Serial Number, and MAC addresses for the Ethernet interface(s). This EEPROM is not available for customer use.

Dedicated HPS Interfaces

The following HPS interfaces have been dedicated as fixed function in order to support proper operation. The module was designed to allow as many HPS fixed and Shared IO pins to be user accessible as possible. See the J1 connector interface description for information on HPS and FPGA Shared IO pins that may be user defined.

Console Serial port

The console serial port (UART1) is supported on pins E40 (RX) and F37 (TX) of the 400 pin Samtec connector (J1) with 1.8V compatible asynchronous UART I/O. By default, the flow control signals are not enabled but can be added to the console serial interface if desired.

I2C1 Interface

The I2C1 peripheral is consumed local to the module. It is used for the Configuration EEPROM, as well as power supply monitoring.

Table 1: I2C0 Peripherals

Address	Device	Feature
1010000	CAT24C256WI-GT3	256Kbit EEPROM for factory configuration parameters
0001110	FS1525	0.7-0.85V Core Power Supply
0001101	FS1525	0.7-0.85V Core Power Supply*
0001011	FS1406	1.1V Power Supply
0001010	FS1406	1.0V Power Supply
0001001	FS1406	1.2V Power Supply
0001000	FS1406	1.8V Power Supply

- This supply may not be installed on smaller density devices.

Debug JTAG

The JTAG interface signals for the Agilex 5E FPGA fabric processor are available through the 400-pin Samtec connector.

JTAG Signal	Samtec Connector Pin	FPGA Pin
TCK	D44	BJ58
TMS	F40	BJ56
TDO	D42	BN55
TDI	D45	BJ53

SOM Clocking

The MitySOM-A5E has multiple oscillators to drive both the HPS and FPGA. There is a dedicated 25Mhz oscillator to drive the HPS reference clock. The SOM clock network is shown in Figure 2.

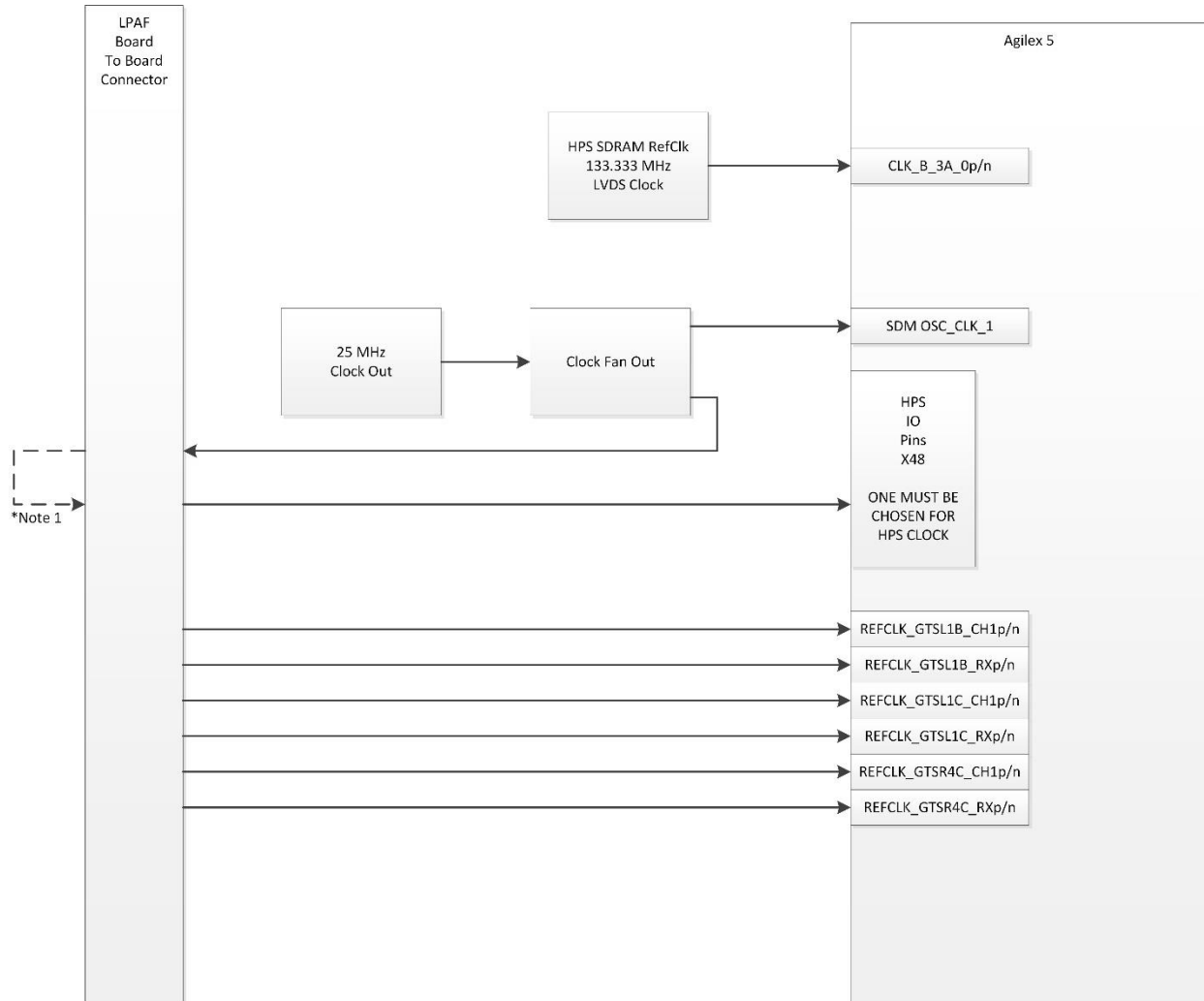


Figure 2: SOM Clocking

Note 1: The HPS clock *must* be looped back into an HPS IO pin, otherwise the module will not boot. The user may use any HPS IO pin for the HPS clock source. The SOM design requires looping the clock back on the baseboard to allow for maximum flexibility in multiplexed HPS IO selection so as not to remove a desired interface option.

External Interfaces

The Agilex 5E makes extensive use of functional pin multiplexing to provide a highly configurable device that can be tailored to a multitude of applications.

HPS Interfaces

A list of the interfaces/functions that are available to the user from the HPS is provided below.

- 1 Universal Serial Bus (USB) 3.1 Gen 1 Super-Speed Controller
- 1 Universal Serial Bus (USB) 2.0 High-Speed On-The-Go Controller
- 2 Improved Inter-Integrated Circuit (I3C) Ports
- 5 Inter-Integrated Circuit (I2C) Ports
 - I2C1 is dedicated for use on J1 (pins A32/A33) with 4.7k ohm pull-up resistors at 1.8V and is available for user access.
 -
- Up to 2 Serial Peripheral (SPI) Ports
- 2 Universal Asynchronous Receive/Transmit (UART) Ports
- Up to 3 Ethernet MACs (10/100/1000/2500 Mbps) with TSN Support

Additionally, most of the pin multiplexed signals can be configured as general purpose I/O signals with interrupt capability.

FPGA Interfaces

GPIO

The Agilex 5E offers up to 48 HPS GPIO signals and up to 144 general FPGA IO pins, all of which are available externally to the module.

The FPGA IO pins provided on J1(A to D) and are connected to Banks 3A, 5, and 6 of the Agilex 5E FPGA. Banks 5 and 6 have 120 pins supporting 1.8/2.5/3.3V CMOS logic, while Bank 3A supports 24 1.1V single ended logic signals.

Several of the pins on banks 5 and 6 of the Agilex 5E also provide alternate functions for routing clock signals into the FPGA for use by the fabric and transceiver subsystems. Users are encouraged to refer to the Agilex 5E datasheet and technical reference manuals for more information.

LVDS / MIPI

Up to 12 LVDS pairs may be configured as transmitters or receivers utilizing the 24 pins available from Bank 3A. This pins support differential signaling and include support for MIPI DPHY transmitter or receiver configuration. Note: The differential IO pairs must honor the Agilex 5 Datasheet requirements for HSIO Bank pins. This requires adjusting the common mode of standard LVDS signals such that the maximum value of the pins do not exceed the Bank voltage levels.

Transceivers

A maximum of twelve high speed transceiver pairs are available on the module for supporting high speed serial interfaces.

Maximum transceiver speed supported is 28Gbps for SOM modules configured with Agilex 5E device group A devices and 17Gbps for those configured with Agilex 5E device group B.

The number of transceiver pairs available is dependent upon device density. All twelve pairs are available in the 282KLE, 434KLE, 524KLE, and 656KLE FPGA densities and a total of four transceiver pairs are available in the 85KLE and 138KLE FPGA densities. All twelve pairs are routed to J1(A). These pairs may be bonded to support protocols such as HDMI, DisplayPort, CoaXpress, PCIe, 10Gb Ethernet, Interlaken, CIPRI, JESD204B, etc. Altera

Configuration and Boot Modes

The Agilex 5E MSEL pins (SDM_IO5, SDM_IO7, SDM_IO9) are used to configure the boot source for the SDM. On the MitySOM-A5E, the MSEL pins are strapped to fixed settings on the board as described below. The MitySOM-A5E provides a local 25 MHz clock source to the OSC_CLK_1 pin for SDM booting purposes.

Boot Media Configuration

The Agilex 5E is configured to boot from its Quad SPI flash using the MSEL pins set to [2:0] '011'b. The MSEL pins are pulled up to 1.8V or down to ground using 4.7k resistors on the SOM, selecting the boot mode "AS (Normal Mode)," as referenced in the Technical Reference Manual (TRM). These bootstrapping pins are not accessible to the user through the Samtec connector. The Agilex 5E may also be configured using the HPS or a JTAG interface.

Debug LEDs

There are 3 debug LEDs on the MitySOM-A5E module.

Power Status LEDs

D3 illuminates, green, when the MitySOM-A5E on-module power supplies have been enabled in sequence and are operating correctly.

Configuration Debug

D2 is connected to the INIT_DONE pin on the Agilex 5E. When lit, green, it indicates the device has been initialized.

D1 is connected to the CONF_DONE pin on the Agilex 5E. When lit, green, it indicates the device configuration has been completed.

Power Interfaces

Input Voltage

The MitySOM-A5E is powered using the VCC_IN input and ground pins on J1. The MitySOM-A5E accepts an input voltage from +5V DC up to +12V DC, and generates +2.5V, +1.8V, +1.2V, +1.1V, +1.0V, and +0.8V on the SOM.

Power utilization of the MitySOM-A5E is heavily dependent on end-user application. Major factors include: ARM CPU PLL configuration, CPU Utilization, and external LPDDR4 RAM utilization. Customers should use Altera's Early Power Estimator (EPE) for the Agilex 5E to better understand the power requirements of the system for power supply sizing for custom baseboards. This utility will assist in estimating the potential power usage of the processor for a given application.

Power Sequencing

The state of the local power supplies is provided on J1 (G30) via the HVIO_ENABLE signal. Until this signal is asserted, the local FPGA power supplies should not be assumed to be on and stable. This signal should be used to sequence or enable any user IO to the module.

Software and FPGA Development Support

Users of the MitySOM-A5E are encouraged to develop applications using the GCC based MitySOM-A5E software development kit (SDK) provided by Critical Link LLC. The SDK is an expansion of the Altera platform support package for the Agilex 5E and includes an implementation of a Yocto Project-compatible board support package providing a Linux root filesystem/distribution and compatible gcc compiler tool-chain with debugger.

FPGA developers should use the Altera FPGA Quartus Pro Design Suite when working with the MitySOM-A5E.

Growth Options

The MitySOM-A5E has been designed to support several upgrade options. These options include a range of speed grades, FPGA density, HPS DDR memory configurations, and operating temperature specifications including commercial and industrial temperature ranges. The available options are listed in the section below containing ordering information. For additional ordering information and details regarding these options, or to inquire about a configuration not listed below, please contact Critical Link at info@criticallink.com.

Absolute Maximum Ratings

If Military/Aerospace specified cards are required, please contact Critical Link at info@criticallink.com for availability and specifications.

Table 2: Absolute Maximum Ratings

Maximum Supply Voltage (VCC_IN)	13.2 V
Storage Temperature Range	-55°C to 150°C

Operating Conditions

The following are the minimum temperature ratings for the components that are installed on a MitySOM-A5E. For specifications not contained in this table please contact Critical Link at info@criticallink.com.

Table 3: Module Component Temperature Ratings

Temperature Range	Component Ratings*
Commercial (-RC)	0°C to 70°C
Industrial (-RI)	-40°C to 85°C

** Please see the Thermal Management section below for ambient/operating temperature recommendations.*

Thermal Management

The MitySOM-A5E module requires careful consideration of thermal management. Depending on load, different thermal management will be required for operation at room temperatures and above. The primary thermal concern is with the Agilex 5E SoC device. Even when idle, case temperature on this device rises significantly. Additional processing activity will require more power consumption and more heat dissipation.

Thermal management is a system level issue that must be addressed in conjunction with the overall system design. Some systems may have available airflow with limited space for a heat sink; others may have room for a heat sink with or without the possibility for additional airflow. As a result, the approach taken for thermal management is a design consideration that must be addressed by the overall system designers when integrating the MitySOM-A5E.

Every end product is different and it is advisable to perform thorough testing to ensure that the product will meet desired performance and longevity specifications. Customers should use Altera's Early Power Estimator (EPE) for the Agilex 5E. This utility will assist in estimating the potential power usage of the processor for a given application. To achieve reliable operation at the maximum specified operating temperatures it has been determined that some form of thermal management (e.g., forced air, heat sink, etc.) will be required.

J1 Connector Interface

The next sections outline the connector pin interface. The pin interfaces are grouped into the signal classes defined in the table below.

Table 5: Connector Interface Signal Class Groups

Class	Applicable IO Standard	Description
POWER	N/A	These are module power input pins and corresponding return pins.
XCVR_TX	High Speed Differential I/O	These pins are directly connected to the Gigabit Transceiver Transmit lanes of the Agilex 5.
XCVR_RX	High Speed Differential I/O	These pins are directly connected to the Gigabit Transceiver Receive lanes of the Agilex 5.
XCVR_REFCLK	High Speed Differential I/O	These pins are directly connected to the Gigabit Transceiver Reference input clocks.
HSIO	GPIO, PHYSLITE, LVDS SERDES, MIPI	These pins are directly connected to FPGA Bank 3A HSIO pins. The Bank voltage is 1.1 V. These pins are on the same bank as the on-board HPS LPDDR4.
HVIO	1.8V CMOS, 2.5V CMOS, 3.3V CMOS	These pins provide single-ended IO buffers that support 1.8V, 2.5V, or 3.3V CMOS logic according to the power inputs bins associated with their FPGA bank location
HPS I/O	1.8V CMOS	These pins provide I/O buffer and support to interface with the HPS. These pins may be configured to support interfaces such as JTAG, mass storage flash, etc. The bank voltage for these pins is 1.8V.
SDM I/O	1.8V CMOS	These pins are connected to the Secure Data Manager subsystem may be used as I/O pins, but can also be configured to support internal pull up and pull down resistors, open-drain output, Schmitt Trigger input buffers, and more. See the interface description for details.

J1 Interface Description

The connector used for J1 is a 400 Pin Samtec SEAM series connector, LPAF-50-03.5-L-08-2-K-TR, which mates with Samtec LPAM-50-01.0-L-08-2-K-TR (the mating height, indicated by the 01.0 in the part number may be taller if desired). The connector is logically broken up into 8 groups (rows) of 50 pins as documented below.



Table contains a summary of the MitySOM-A5E J1 Interface pin-mapping.

For more information about pin definitions and pin connection guidelines please refer to the Agilex 5 Device Family Pin Connection Guidelines.



Table 6: MitySOM-A5E J1(A) Connector Pin-Out

Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10
A1	POWER	GND	-	-										
A2	HSIO	DIFF_IO_3A_T16_N	3A_T	D21										
A3	HSIO	DIFF_IO_3A_T16_P	3A_T	F21										
A4	POWER	GND	-	-										
A5	HSIO	DIFF_IO_3A_T14_P	3A_T	F15										
A6	HSIO	DIFF_IO_3A_T14_N	3A_T	H15										
A7	POWER	GND	-	-										
A8	HSIO	DIFF_IO_3A_T17_P	3A_T	F24										
A9	HSIO	DIFF_IO_3A_T17_N	3A_T	H24										
A10	POWER	GND	-	-										
A11	HSIO	DIFF_IO_3A_T24_N	3A_T	P39										
A12	HSIO	DIFF_IO_3A_T24_P	3A_T	V41										
A13	POWER	GND	-	-										
A14	HSIO	DIFF_IO_3A_T22_P	3A_T	P33										
A15	HSIO	DIFF_IO_3A_T22_N	3A_T	V33										
A16	POWER	GND	-	-										
A17	HSIO	DIFF_IO_3A_T20_P	3A_T	P27										
A18	HSIO	DIFF_IO_3A_T20_N	3A_T	P25										
A19	POWER	VCCIO_6A6B	6A & 6B	-										
A20	POWER	VCCIO_6A6B	6A & 6B	-										
A21	HVIO	HVIO_5A_1	5A	BG81	HVIO_5A_1	TXCLK1	Data_Ctrl1.BG81							
A22	HVIO	HVIO_5A_3	5A	BG80	HVIO_5A_3	TXCLK3	Data_Ctrl3.BG80							
A23	HVIO	HVIO_5A_6	5A	BK81	HVIO_5A_6	PIN_PERST_N_CVP_L1B_0	TXCLK6	Data_Ctrl6.BK81						
A24	HVIO	HVIO_5A_5	5A	BK80	HVIO_5A_5	PIN_PERST_N_CVP_L1A_0	TXCLK5	Data_Ctrl5.BK80						
A25	HVIO	HVIO_5A_11	5A	BP81	HVIO_5A_11	SOURCE_SYNC_CLK1	TXCLK11	RXCLK3	Data_Ctrl11.BP81					
A26	HVIO	HVIO_5A_10	5A	BM80	HVIO_5A_10	PLLREFCLK2	TXCLK10	RXCLK2	Data_Ctrl10.BM80					
A27	HVIO	HVIO_5A_12	5A	BP80	HVIO_5A_12	SOURCE_SYNC_CLK2	TXCLK12	RXCLK4	Data_Ctrl12.BP80					
A28	HVIO	HVIO_5A_16	5A	BU80	HVIO_5A_16	TXCLK16	Data_Ctrl16.BU80							
A29	HVIO	HVIO_5A_2	5A	BD81	HVIO_5A_2	TXCLK2	Data_Ctrl2.BD81							
A30	HVIO	HVIO_5A_15	5A	BU78	HVIO_5A_15	TXCLK15	Data_Ctrl15.BU78							
A31	POWER	GND	-	-										
A32	HPS IO	I2CL_SDA	HPS IOB	B59										
A33	HPS IO	I2CL_SCL	HPS IOB	A59										
A34	POWER	GND	-	-										
A35	POWER	GND	-	-										
A36	XCVR_RX	GTSLIB_RX_CH1_N	1B	AW79										
A37	XCVR_RX	GTSLIB_RX_CH1_P	1B	AW81										
A38	POWER	GND	-	-										
A39	POWER	GND	-	-										
A40	XCVR_RX	GTSLIB_RX_CH3_N	1B	AR79										
A41	XCVR_RX	GTSLIB_RX_CH3_P	1B	AR81										
A42	POWER	GND	-	-										
A43	POWER	GND	-	-										
A44	XCVR_RX	GTSLIC_RX_CH1_N	1C	AF79										
A45	XCVR_RX	GTSLIC_RX_CH1_P	1C	AF81										
A46	POWER	GND	-	-										
A47	POWER	GND	-	-										
A48	XCVR_RX	GTSLIC_RX_CH3_N	1C	P79										
A49	XCVR_RX	GTSLIC_RX_CH3_P	1C	P81										
A50	POWER	GND	-	-										



Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10
B1	POWER	+1.8V	-	-										
B2	POWER	+1.8V	-	-										
B3	HSIO	DIFF_IO_3A_T13_P	3A_T	D11										
B4	HSIO	DIFF_IO_3A_T13_N	3A_T	F11										
B5	POWER	GND	-	-										
B6	HSIO	DIFF_IO_3A_T15_N	3A_T	K15										
B7	HSIO	DIFF_IO_3A_T15_P	3A_T	K11										
B8	POWER	GND	-	-										
B9	HSIO	DIFF_IO_3A_T18_P	3A_T	K21										
B10	HSIO	DIFF_IO_3A_T18_N	3A_T	K24										
B11	POWER	GND	-	-										
B12	HSIO	DIFF_IO_3A_T23_N	3A_T	P35										
B13	HSIO	DIFF_IO_3A_T23_P	3A_T	V35										
B14	POWER	GND	-	-										
B15	HSIO	DIFF_IO_3A_T21_P	3A_T	V30										
B16	DHSIO	DIFF_IO_3A_T21_N	3A_T	V27										
B17	POWER	GND	-	-										
B18	HSIO	DIFF_IO_3A_T19_P	3A_T	P22										
B19	HSIO	DIFF_IO_3A_T19_N	3A_T	V22										
B20	POWER	+1.1V	3A_T	-										
B21	POWER	+1.1V	3A_T	-										
B22	HVIO	HVIO_5A_19	5A	Bj69	HVIO_5A_19	TXCLK19	Data_Ctrl19.Bj69							
B23	HVIO	HVIO_5A_20	5A	BE69	HVIO_5A_20	TXCLK20	Data_Ctrl20.BE69							
B24	HVIO	HVIO_5A_8	5A	BF74	HVIO_5A_8	TXCLK8	Data_Ctrl8.BF74							
B25	HVIO	HVIO_5A_7	5A	BH74	HVIO_5A_7	PIN_PERST_N_CVP_L1C_0	TXCLK7	Data_Ctrl7.BH74						
B26	HVIO	HVIO_5A_4	5A	BF78	HVIO_5A_4	TXCLK4	Data_Ctrl4.BF78							
B27	HVIO	HVIO_5A_18	5A	BN74	HVIO_5A_18	TXCLK18	Data_Ctrl18.BN74							
B28	HVIO	HVIO_5A_17	5A	BR74	HVIO_5A_17	TXCLK17	Data_Ctrl17.BR74							
B29	HVIO	HVIO_5A_9	5A	BL78	HVIO_5A_9	PLLREFCLK1	TXCLK9	RXCLK1	Data_Ctrl9.BL78					
B30	HVIO	HVIO_5A_14	5A	BN78	HVIO_5A_14	TXCLK14	Data_Ctrl14.BN78							
B31	HVIO	HVIO_5A_13	5A	BR78	HVIO_5A_13	TXCLK13	Data_Ctrl13.BR78							
B32	POWER	GND	-	-										
B33	POWER	GND	-	-										
B34	XCVR_TX	GTSLIC_TX_CH1_N	1C	AJ72										
B35	XCVR_TX	GTSLIC_TX_CH1_P	1C	AJ75										
B36	POWER	GND	-	-										
B37	POWER	GND	-	-										
B38	XCVR_TX	GTSLIC_TX_CH2_N	1C	AC72										
B39	XCVR_TX	GTSLIC_TX_CH2_P	1C	AC75										
B40	POWER	GND	-	-										
B41	POWER	GND	-	-										
B42	XCVR_TX	GTSLIC_TX_CH3_N	1C	V72										
B43	XCVR_TX	GTSLIC_TX_CH3_P	1C	V75										
B44	POWER	GND	-	-										
B45	POWER	GND	-	-										
B46	XCVR_RX	GTSLIC_RX_CH2_N	1C	Y79										
B47	XCVR_RX	GTSLIC_RX_CH2_P	1C	Y81										
B48	POWER	GND	-	-										
B49	POWER	GND	-	-										
B50	SDM I/O	INIT_DONE	SDM	BU34										



Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10
C1	POWER	VCC_IN	-	-										
C2	POWER	VCC_IN	-	-										
C3	POWER	GND	-	-										
C4	POWER	GND	-	-										
C5	HVIO	HVIO_6C_1	6C	P19	HVIO_6C_1	TXCLK1	Data_Ctrl1.P19							
C6	HVIO	HVIO_6D_17	6D	R10	HVIO_6D_17	TXCLK17	Data_Ctrl17.R10							
C7	HVIO	HVIO_6D_14	6D	U5	HVIO_6D_14	TXCLK14	Data_Ctrl14.U5							
C8	HVIO	HVIO_6D_9	6D	AA1	HVIO_6D_9	PLLREFCLK1	TXCLK9	RXCLK1	Data_Ctrl9.AA1					
C9	HVIO	HVIO_6D_10	6D	AD1	HVIO_6D_10	PLLREFCLK2	TXCLK10	RXCLK2	Data_Ctrl10.AD1					
C10	HVIO	HVIO_6D_3	6D	AG1	HVIO_6D_3	TXCLK3	Data_Ctrl3.AG1							
C11	HVIO	HVIO_6C_10	6C	AB7	HVIO_6C_10	PLLREFCLK2	TXCLK10	RXCLK2	Data_Ctrl10.AB7					
C12	HVIO	HVIO_6C_12	6C	AE7	HVIO_6C_12	SOURCE_SYNC_CLK2	TXCLK12	RXCLK4	Data_Ctrl12.AE7					
C13	HVIO	HVIO_6D_1	6D	AN1	HVIO_6D_1	TXCLK1	Data_Ctrl1.AN1							
C14	HVIO	HVIO_6C_9	6C	AE14	HVIO_6C_9	PLLREFCLK1	TXCLK9	RXCLK1	Data_Ctrl9.AE14					
C15	POWER	GND	-	-										
C16	POWER	GND	-	-										
C17	POWER	GND	-	-										
C18	HVIO	HVIO_5B_19	5B	BV76	HVIO_5B_19	SYSPLLREFCLK_L1C_0	TXCLK19	Data_Ctrl19.BV76						
C19	HVIO	HVIO_5B_20	5B	BU73	HVIO_5B_20	TXCLK20	Data_Ctrl20.BU73							
C20	HVIO	HVIO_5B_18	5B	BV73	HVIO_5B_18	TXCLK18	Data_Ctrl18.BV73							
C21	HVIO	HVIO_5B_16	5B	BU71	HVIO_5B_16	TXCLK16	Data_Ctrl16.BU71							
C22	HVIO	HVIO_5B_17	5B	BV71	HVIO_5B_17	TXCLK17	Data_Ctrl17.BV71							
C23	HVIO	HVIO_5B_8	5B	BV61	HVIO_5B_8	TXCLK8	Data_Ctrl8.BV61							
C24	HVIO	HVIO_5B_9	5B	BV63	HVIO_5B_9	PLLREFCLK1	TXCLK9	RXCLK1	Data_Ctrl9.BV63					
C25	HVIO	HVIO_5B_14	5B	BV65	HVIO_5B_14	TXCLK14	Data_Ctrl14.BV65							
C26	HVIO	HVIO_5B_13	5B	BU68	HVIO_5B_13	TXCLK13	Data_Ctrl13.BU68							
C27	HVIO	HVIO_5B_15	5B	BN70	HVIO_5B_15	TXCLK15	Data_Ctrl15.BN70							
C28	POWER	GND	-	-										
C29	SDM I/O	HPS_COLD_nRESET	SDM	BN28										
C30	SDM I/O	SDM_IO13	SDM	BJ45										
C31	SDM I/O	SDM_IO8	SDM	BJ39										
C32	HSIO	GPIO0_IO5	HPS IOA	P64	GPIO0_5	SPIM0_MOSI	UART1_RTS_N	I2C0_SCL	NAND_ADQ2	SDMMC_D2	USB0_NXT	EMAC2_PPSTRIG2	TRC_D5.P64	
C33	HSIO	GPIO0_IO15	HPS IOA	K70	GPIO0_15	NAND_DQS	SDMMC_D_STROBE	USB1_D0	EMAC0_RX_CTL	TRC_D7.K70				
C34	POWER	GND	-	-										
C35	POWER	GND	-	-										
C36	HPS IO	GPIO0_IO11	HPS IOA	F78	GPIO0_11	SPIM1_SS0_N	SPI1_MISO	MDIO0_MDC	I2C_EMAC0_SCL	NAND_ADQ7	SDMMC_D7	USB0_D7	I3C0_SCL	TRC_D11.F78
C37	HPS IO	GPIO0_IO1	HPS IOA	C80	GPIO0_1	SPIM1_SS1_N	SPI0_MOSI	UART0_RTS_N	NAND_ADQ1	SDMMC_D1	USB0_STP	EMAC0_PPSTRIG0	TRC_D9.C80	
C38	POWER	GND	-	-										
C39	POWER	GND	-	-										
C40	HPS IO	GPIO1_IO17	HPS IOB	D60	GPIO1_17	SPIM0_SS1_N	UART1_RTS_N	NAND_ADO9	I3C0_SCL	EMAC2_TXD1	TRC_D5.D60			
C41	HPS IO	GPIO1_IO21	HPS IOB	D67	GPIO1_21	SPIM0_MOSI	SPI1_MOSI	I2C_EMAC2_SCL	NAND_ADQ13	EMAC2_TXD3	TRC_D1.D67			
C42	POWER	GND	-	-										
C43	POWER	GND	-	-										
C44	XCVR REFCLK	REFCLK_GTSLIB_RX_N	1B	BA69										
C45	XCVR REFCLK	REFCLK_GTSLIB_RX_P	1B	BA66										
C46	POWER	GND	-	-										
C47	POWER	GND	-	-										
C48	XCVR REFCLK	REFCLK_GTSLIC_CH1_P	1B	AR69										
C49	XCVR REFCLK	REFCLK_GTSLIC_CH1_N	1B	AR66										
C50	POWER	GND	-	-										



Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10
D1	POWER	VCC_IN	-	-										
D2	POWER	VCC_IN	-	-										
D3	POWER	GND	-	-										
D4	POWER	GND	-	-										
D5	HVIO	HVIO_6D_18	6D	K4	HVIO_6D_18	TXCLK18	Data_Ctrl18.K4							
D6	HVIO	HVIO_6D_19	6D	R14	HVIO_6D_19	TXCLK19	Data_Ctrl19.R14							
D7	HVIO	HVIO_6D_15	6D	R7	HVIO_6D_15	TXCLK15	Data_Ctrl15.R7							
D8	HVIO	HVIO_6D_20	6D	U14	HVIO_6D_20	TXCLK20	Data_Ctrl20.U14							
D9	HVIO	HVIO_6D_7	6D	AD2	HVIO_6D_7	TXCLK7	Data_Ctrl7.AD2							
D10	HVIO	HVIO_6C_3	6C	V19	HVIO_6C_3	TXCLK3	Data_Ctrl3.V19							
D11	HVIO	HVIO_6D_4	6D	AG2	HVIO_6D_4	TXCLK4	Data_Ctrl4.AG2							
D12	HVIO	HVIO_6C_11	6C	AE5	HVIO_6C_11	SOURCE_SYNC_CLK1	TXCLK11	RXCLK3	Data_Ctrl11.AE5					
D13	HVIO	HVIO_6C_14	6C	AB10	HVIO_6C_14	TXCLK14	Data_Ctrl14.AB10							
D14	HVIO	HVIO_6C_2	6C	Y22	HVIO_6C_2	TXCLK2	Data_Ctrl2.Y22							
D15	POWER	VCCIO_6C6D	6C & 6D	-										
D16	POWER	VCCIO_6C6D	6C & 6D	-										
D17	POWER	GND	-	-										
D18	HVIO	HVIO_5B_3	5B	BN60	HVIO_5B_3	SYSPLLREFCLK_L1B_0	TXCLK3	Data_Ctrl3.BN60						
D19	HVIO	HVIO_5B_4	5B	BR60	HVIO_5B_4	SYSPLLREFCLK_L1B_1	TXCLK4	Data_Ctrl4.BR60						
D20	HVIO	HVIO_5B_1	5B	BU57	HVIO_5B_1	SYSPLLREFCLK_L1A_0	TXCLK1	Data_Ctrl1.BU57						
D21	HVIO	HVIO_5B_7	5B	BU59	HVIO_5B_7	PIN_PERST_N_CVP_L1C_1	TXCLK7	Data_Ctrl7.BU59						
D22	HVIO	HVIO_5B_2	5B	BN62	HVIO_5B_2	SYSPLLREFCLK_L1A_1	TXCLK2	Data_Ctrl2.BN62						
D23	HVIO	HVIO_5B_5	5B	BV59	HVIO_5B_5	PIN_PERST_N_CVP_L1A_1	TXCLK5	Data_Ctrl5.BV59						
D24	HVIO	HVIO_5B_6	5B	BU61	HVIO_5B_6	PIN_PERST_N_CVP_L1B_1	TXCLK6	Data_Ctrl6.BU61						
D25	HVIO	HVIO_5B_11	5B	BN67	HVIO_5B_11	SOURCE_SYNC_CLK1	TXCLK11	RXCLK3	Data_Ctrl11.BN67					
D26	HVIO	HVIO_5B_10	5B	BU65	HVIO_5B_10	PLLREFCLK2	TXCLK10	RXCLK2	Data_Ctrl10.BU65					
D27	HVIO	HVIO_5B_12	5B	BR67	HVIO_5B_12	SOURCE_SYNC_CLK2	TXCLK12	RXCLK4	Data_Ctrl12.BR67					
D28	POWER	GND	-	-										
D29	POWER	GND	-	-										
D30	HPS IO	GPIO0_IO3	HPS IOA	V64	GPIO0_3	SPIS0_MISO	UART0_RX	I2C1_SCL	NAND_RE_N	USB0_D0	EMAC1_PPSTRIG1	TRC_D7.V64		
D31	HPS IO	GPIO0_IO19	HPS IOA	K60	GPIO0_19	SPIM1_SS1_N	I3C0_SCL	NAND_ADQ11	USB1_D3	EMAC0_RXD1	TRC_CLK_K60			
D32	HPS IO	GPIO0_IO17	HPS IOA	H70	GPIO0_17	I3C1_SCL	NAND_ADQ9	USB1_NXT	EMAC0_TXD1	TRC_D5.H70				
D33	HPS IO	GPIO0_IO7	HPS IOA	K74	GPIO0_7	SPIM0_SS0_N	MDIO2_MDC	UART1_RX	I2C_EMAC2_SCL	NAND_CLE	SDMMC_CMD	USB0_D3	TRC_D15.K74	
D34	HPS IO	GPIO0_IO9	HPS IOA	F74	GPIO0_9	SPIM1_MOSI	SPIS1_MOSI	MDIO1_MDC	I2C_EMAC1_SCL	NAND_ADQ5	SDMMC_D5	USB0_D5	I3C1_SCL	TRC_D13.F74
D35	HPS IO	GPIO0_IO6	HPS IOA	G80	GPIO0_6	SPIM0_MISO	MDIO2_MDIO	UART1_TX	I2C_EMAC2_SDA	NAND_ADQ3	SDMMC_D3	USB0_D2	TRC_D4.G80	
D36	HPS IO	GPIO0_IO10	HPS IOA	H78	GPIO0_10	SPIM1_MISO	SPIS1_SS0_N	MDIO0_MDIO	I2C_EMAC0_SDA	NAND_ADQ6	SDMMC_D6	USB0_D6	I3C0_SDA	TRC_D12.H78
D37	HPS IO	GPIO0_IO0	HPS IOA	B80	GPIO0_0	SPIM0_SS1_N	SPIS0_CLK	UART0_CTS_N	NAND_ADQ0	SDMMC_D0	USB0_CLK	EMAC0_PPS0	TRC_D10.B80	
D38	HPS IO	GPIO0_IO16	HPS IOA	A76	GPIO0_16	I3C1_SDA	NAND_ADQ8	USB1_D1	EMAC0_TXD0	TRC_D6.A76				
D39	HPS IO	GPIO1_IO7	HPS IOB	K62	GPIO1_7	SPIS1_MISO	UART1_RX	I2C1_SCL	NAND_CLE	SDMMC_CMD	I3C0_SCL	EMAC1_RXD1	TRC_D15.K62	
D40	POWER	GND	-	-										
D41	HPS IO	GPIO1_IO19	HPS IOB	F67	GPIO1_19	SPIM0_SS0_N	MDIO1_MDC	I2C_EMAC1_SCL	NAND_ADQ11	EMAC2_RXD1	TRC_CLK_F67			
D42	HPS IO	GPIO1_IO10	HPS IOB	B61	GPIO1_10	JTAG_TDO	SPIS0_SS0_N	MDIO0_MDIO	I2C_EMAC0_SDA	NAND_ADQ6	SDMMC_D6	EMAC1_RXD2	TRC_D12.B61	
D43	HPS IO	GPIO1_IO0	HPS IOB	B68	GPIO1_0	SPIM1_CLK	UART0_CTS_N	EMAC0_PPS0	NAND_ADQ0	SDMMC_D0	EMAC1_TX_CLK	Trace_D10.B68		
D44	HPS IO	GPIO1_IO8	HPS IOB	A65	GPIO1_8	JTAG_TCK	SPIS0_CLK	MDIO2_MDIO	I2C_EMAC2_SDA	NAND_ADQ4	SDMMC_D4	EMAC1_TXD2	TRC_D14.A65	
D45	HPS IO	GPIO1_IO11	HPS IOB	A61	GPIO1_11	JTAG_TDI	SPIS0_MISO	MDIO0_MDC	I2C_EMAC0_SCL	NAND_ADQ7	SDMMC_D7	EMAC1_RXD3	TRC_D11.A61	
D46	HPS IO	GPIO1_IO16	HPS IOB	B54	GPIO1_16	UART1_CTS_N	NAND_ADQ8	I3C0_SDA	EMAC2_TXD0	TRC_D6.B54				
D47	HPS IO	GPIO1_IO23	HPS IOB	B47	GPIO1_23	SPIM0_SS0_N	SPIS1_MISO	MDIO0_MDC	I2C_EMAC0_SCL	NAND_ADQ15	EMAC2_RXD3	TRC_D3.B47		
D48	HPS IO	GPIO1_IO14	HPS IOB	A54	GPIO1_14	UART1_TX	NAND_CE_N	I3C1_SDA	EMAC2_RX_CLK	TRC_D8.A54				
D49	POWER	GND	-	-										
D50	OUTPUT	HPS_CLKIN	+1.8V	-										



Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10
E1	POWER	VCC_IN	-	-										
E2	POWER	VCC_IN	-	-										
E3	POWER	GND	-	-										
E4	HVIO	HVIO_6D_16	6D	F4	HVIO_6D_16	TXCLK16	Data_Ctrl16.F4							
E5	HVIO	HVIO_6D_12	6D	D4	HVIO_6D_12	SOURCE_SYNC_CLK2	TXCLK12	RXCLK4	Data_Ctrl12.D4					
E6	POWER	GND	-	-										
E7	POWER	GND	-	-										
E8	HVIO	HVIO_6D_13	6D	U7	HVIO_6D_13	TXCLK13	Data_Ctrl13.U7							
E9	HVIO	HVIO_6D_11	6D	AA2	HVIO_6D_11	SOURCE_SYNC_CLK1	TXCLK11	RXCLK3	Data_Ctrl11.AA2					
E10	POWER	GND	-	-										
E11	POWER	GND	-	-										
E12	HVIO	HVIO_6D_8	6D	AH2	HVIO_6D_8	TXCLK8	Data_Ctrl8.AH2							
E13	HVIO	HVIO_6D_5	6D	AL1	HVIO_6D_5	TXCLK5	Data_Ctrl5.AL1							
E14	HVIO	HVIO_6C_5	6C	AB14	HVIO_6C_5	TXCLK5	Data_Ctrl5.AB14							
E15	HVIO	HVIO_6C_8	6C	AC19	HVIO_6C_8	TXCLK8	Data_Ctrl8.AC19							
E16	HVIO	HVIO_6C_18	6C	AK10	HVIO_6C_18	TXCLK18	Data_Ctrl18.AK10							
E17	HVIO	HVIO_6C_7	6C	AF19	HVIO_6C_7	TXCLK7	Data_Ctrl7.AF19							
E18	HVIO	HVIO_6C_17	6C	AJ22	HVIO_6C_17	TXCLK17	Data_Ctrl17.AJ22							
E19	HVIO	HVIO_6C_16	6C	AM22	HVIO_6C_16	TXCLK16	Data_Ctrl16.AM22							
E20	HVIO	HVIO_6C_19	6C	AP19	HVIO_6C_19	TXCLK19	Data_Ctrl19.AP19							
E21	POWER	GND	-	-										
E22	HVIO	HVIO_6A_13	6A	BN4	HVIO_6A_13	TXCLK13	Data_Ctrl13.BN4							
E23	HVIO	HVIO_6A_18	6A	BF4	HVIO_6A_18	TXCLK18	Data_Ctrl18.BF4							
E24	HVIO	HVIO_6A_10	6A	BF11	HVIO_6A_10	PLLREFCLK2	TXCLK10	RXCLK2	Data_Ctrl10.BF11					
E25	HVIO	HVIO_6A_14	6A	BN11	HVIO_6A_14	TXCLK14	Data_Ctrl14.BN11							
E26	HVIO	HVIO_6A_20	6A	BC13	HVIO_6A_20	TXCLK20	Data_Ctrl20.BC13							
E27	HVIO	HVIO_6A_6	6A	BN15	HVIO_6A_6	PIN_PERST_N_R4B_0	TXCLK6	Data_Ctrl6.BN15						
E28	HVIO	HVIO_6A_9	6A	BH15	HVIO_6A_9	PLLREFCLK1	TXCLK9	RXCLK1	Data_Ctrl9.BH15					
E29	HVIO	HVIO_6A_7	6A	BR21	HVIO_6A_7	PIN_PERST_N_R4C_0	TXCLK7	Data_Ctrl7.BR21						
E30	HVIO	HVIO_6A_3	6A	BU25	HVIO_6A_3	SYSPLLREFCLK_R4B_0	TXCLK3	Data_Ctrl3.BU25						
E31	HVIO	HVIO_6A_5	6A	BJ19	HVIO_6A_5	PIN_PERST_N_R4A_0	TXCLK5	Data_Ctrl5.BJ19						
E32	POWER	GND	-	-										
E33	HPS IO	GPIO0_IO18	HPS IOA	B73	GPIO0_18	I3C0_SDA	NAND_ADQ10	USB1_D2	EMAC0_RXD0	TRC_D4.B73				
E34	HPS IO	GPIO0_IO12	HPS IOA	D74	GPIO0_12	NAND_ALE	SDMMC_PU_PD_D2	USB1_CLK	EMAC0_TX_CLK	TRC_D10.D74				
E35	HPS IO	GPIO0_IO4	HPS IOA	G81	GPIO0_4	SPIM0_CLK	UART1_CTS_N	I2C0_SDA	NAND_WP_N	SDMMC_WRITE_PROTECT	USB0_D1	EMAC2_PPS2	TRC_D6.G81	
E36	HPS IO	GPIO0_IO2	HPS IOA	E81	GPIO0_2	SPIS0_SS0_N	UART0_TX	I2C1_SDA	NAND_WE_N	SDMMC_CLK	USB0_DIR	EMAC1_PPS1	TRC_D8.E81	
E37	HPS IO	GPIO0_IO13	HPS IOA	B78	GPIO0_13	NAND_RB_N	SDMMC_PWR_ENA	USB1_STP	EMAC0_TX_CTL	Trace_D9.B78				
E38	HPS IO	GPIO0_IO20	HPS IOA	A73	GPIO0_20	SPIM1_CLK	SPIS0_CLK	UART0_CTS_N	I2C1_SDA	NAND_ADQ12	USB1_D4	EMAC0_TXD2	TRC_D0.A73	
E39	HPS IO	GPIO0_IO23	HPS IOA	A71	GPIO0_23	SPIM1_SS0_N	SPIS0_MISO	UART0_RX	I2C0_SCL	NAND_ADQ15	USB1_D7	EMAC0_RXD3	TRC_D3.A71	
	HPS IO	GPIO1_IO15	HPS IOB	F60	GPIO1_15	UART1_RX	NAND_DQS	SDMMC_D_STRO_BE	I3C1_SCL	EMAC2_RX_CTL	TRC_D7.F60			
E40	HPS IO	GPIO1_IO15	HPS IOB	F60	GPIO1_15	UART1_RX	NAND_DQS	SDMMC_D_STRO_BE	I3C1_SCL	EMAC2_RX_CTL	TRC_D7.F60			
E41	HPS IO	GPIO1_IO5	HPS IOB	F70	GPIO1_5	SPIS1_MOSI	UART1_RTS_N	EMAC2_PPSTRIG2	NAND_ADQ2	SDMMC_D2	I3C1_SCL	EMAC1_TXD1	TRC_D5.F70	
E42	HPS IO	GPIO1_IO6	HPS IOB	B65	GPIO1_6	SPIS1_SS0_N	UART1_TX	I2C1_SDA	NAND_ADQ3	SDMMC_D3	I3C0_SDA	EMAC1_RXD0	TRC_D4.B65	
E43	POWER	GND	-	-										
E44	HPS IO	GPIO1_IO1	HPS IOB	A63	GPIO1_1	SPIM1_MOSI	UART0_RTS_N	EMAC0_PPSTRIG0	NAND_ADQ1	SDMMC_D1	EMAC1_TX_CTL	Trace_D9.A63		
E45	HPS IO	GPIO1_IO20	HPS IOB	B49	GPIO1_20	SPIM0_CLK	SPIS1_CLK	I2C_EMAC2_SDA	NAND_ADQ12	EMAC2_TXD2	TRC_D0.B49			
	HPS IO	GPIO1_IO4	HPS IOB	B57	GPIO1_4	SPIM1_SS1_N	SPIS1_CLK	UART1_CTS_N	EMAC2_PPS2	NAND_WP_N	SDMMC_WRITE_PROTECT	I3C1_SDA	EMAC1_TXD0	TRC_D6.B57
E46	HPS IO	GPIO1_IO4	HPS IOB	B57	GPIO1_4	SPIM1_SS1_N	SPIS1_CLK	UART1_CTS_N	EMAC2_PPS2	NAND_WP_N	SDMMC_WRITE_PROTECT	I3C1_SDA	EMAC1_TXD0	TRC_D6.B57
E47	HPS IO	GPIO1_IO2	HPS IOB	A51	GPIO1_2	SPIM1_MISO	UART0_TX	I2C0_SDA	NAND_WE_N	SDMMC_CLK	EMAC1_RX_CLK	Trace_D8.A51		
E48	HPS IO	GPIO1_IO18	HPS IOB	A49	GPIO1_18	SPIM0_MISO	MDIO1_MDIO	I2C_EMAC1_SDA	NAND_ADQ10	EMAC2_RXD0	TRC_D4.A49			
E49	HPS IO	GPIO1_IO22	HPS IOB	A47	GPIO1_22	SPIM0_MISO	SPIS1_SS0_N	MDIO0_MDIO	I2C_EMAC0_SDA	NAND_ADQ14	EMAC2_RXD2	TRC_D2.A47		
E50	POWER	GND	-	-										



Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10
F1	POWER	VCC_IN	-	-										
F2	POWER	VCC_IN	-	-										
F3	POWER	GND	-	-										
F4	POWER	GND	-	-										
F5	POWER	GND	-	-										
F6	XCVR_RX	GTSR4C_RX_CH2_P	4C	AV1										
F7	XCVR_RX	GTSR4C_RX_CH2_N	4C	AV3										
F8	POWER	GND	-	-										
F9	POWER	GND	-	-										
F10	XCVR_RX	GTSR4C_RX_CH0_P	4C	BB1										
F11	XCVR_RX	GTSR4C_RX_CH0_N	4C	BB3										
F12	POWER	GND	-	-										
F13	HVIO	HVIO_6D_6	6D	AL2	HVIO_6D_6	TXCLK6		Data_Ctrl6.AL2						
F14	HVIO	HVIO_6D_2	6D	AN2	HVIO_6D_2	TXCLK2		Data_Ctrl2.AN2						
F15	HVIO	HVIO_6C_15	6C	AK7	HVIO_6C_15	TXCLK15		Data_Ctrl15.AK7						
F16	HVIO	HVIO_6C_4	6C	AC22	HVIO_6C_4	TXCLK4		Data_Ctrl4.AC22						
F17	HVIO	HVIO_6C_13	6C	AK14	HVIO_6C_13	TXCLK13		Data_Ctrl13.AK14						
F18	HVIO	HVIO_6C_6	6C	AF22	HVIO_6C_6	TXCLK6		Data_Ctrl6.AF22						
F19	HVIO	HVIO_6C_20	6C	AM19	HVIO_6C_20	TXCLK20		Data_Ctrl20.AM19						
F20	POWER	GND	-	-										
F21	HVIO	HVIO_6A_16	6A	BL4	HVIO_6A_16	TXCLK16		Data_Ctrl16.BL4						
F22	HVIO	HVIO_6A_17	6A	BH4	HVIO_6A_17	TXCLK17		Data_Ctrl17.BH4						
F23	HVIO	HVIO_6A_19	6A	BC9	HVIO_6A_19	SYSPLLREFCLK_R4C_0	TXCLK19	Data_Ctrl19.BC9						
F24	HVIO	HVIO_6A_12	6A	BH11	HVIO_6A_12	SOURCE_SYNC_CLK2	TXCLK12	RXCLK4		Data_Ctrl12.BH11				
F25	HVIO	HVIO_6A_15	6A	BR11	HVIO_6A_15	TXCLK15		Data_Ctrl15.BR11						
F26	HVIO	HVIO_6A_8	6A	BL15	HVIO_6A_8	TXCLK8		Data_Ctrl8.BL15						
F27	HVIO	HVIO_6A_11	6A	BF15	HVIO_6A_11	SOURCE_SYNC_CLK1	TXCLK11	RXCLK3		Data_Ctrl11.BF15				
F28	HVIO	HVIO_6A_2	6A	BN21	HVIO_6A_2	SYSPLLREFCLK_R4A_1	TXCLK2	Data_Ctrl2.BN21						
F29	HVIO	HVIO_6A_4	6A	BV25	HVIO_6A_4	SYSPLLREFCLK_R4B_1	TXCLK4	Data_Ctrl4.BV25						
F30	HVIO	HVIO_6A_1	6A	BN24	HVIO_6A_1	SYSPLLREFCLK_R4A_0	TXCLK1	Data_Ctrl1.BN24						
F31	POWER	GND	-	-										
F32	HPS IO	GPI00_IO21	HPS IOA	F62	GPI00_21	SPIM1_MOSI	SPIS0_MOSI	UART0_RTS_N	I2C1_SCL	NAND_ADQ13	USB1_D5	EMAC0_TXD3	TRC_D1.F62	
F33	HPS IO	GPI00_IO22	HPS IOA	B71	GPI00_22	SPIM1_MISO	SPIS0_SS0_N	UART0_TX	I2C0_SDA	NAND_ADQ14	USB1_D6	EMAC0_RXD2	TRC_D2.B71	
F34	POWER	GND	-	-										
F35	POWER	GND	-	-										
F36	HPS IO	GPI00_IO8	HPS IOA	E80	GPI00_8	SPIM1_CLK	SPIS1_CLK	MDIO1_MDIO	I2C_EMAC1_SDA	NAND_ADQ4	SDMMC_D4	USB0_D4	I3C1_SDA	TRC_D14.E80
F37	HPS IO	GPI00_IO14	HPS IOA	B76	GPI00_14	NAND_CE_N	USB1_DIR	EMAC0_RX_CLK	TRC_D8.B76					
F38	POWER	GND	-	-										
F39	POWER	GND	-	-										
F40	HPS IO	GPI01_IO9	HPS IOB	H62	GPI01_9	JTAG_TMS	SPIS0_MOSI	MDIO2_MDC	I2C_EMAC2_SCL	NAND_ADQ5	SDMMC_D5	EMAC1_TXD3	TRC_D13.H62	
F41	HPS IO	GPI01_IO3	HPS IOB	K67	GPI01_3	SPIM1_SS0_N	UART0_RX	I2C0_SCL	NAND_RE_N	EMAC1_RX_CTL	Trace_D7.K67			
F42	POWER	GND	-	-										
F43	POWER	GND	-	-										
F44	XCVR_REFCLK	REFCLK_GTSLIB_CH1_P	1B	AW69										
F45	XCVR_REFCLK	REFCLK_GTSLIB_CH1_N	1B	AW66										
F46	POWER	GND	-	-										
F47	POWER	GND	-	-										
F48	XCVR_REFCLK	REFCLK_GTSLIC_RX_P	1C	AU69										
F49	XCVR_REFCLK	REFCLK_GTSLIC_RX_N	1C	AU66										
F50	POWER	GND	-	-										



Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10
G1		CORE_EN												
G2	POWER	GND	-	-										
G3	POWER	GND	-	-										
G4	XCVR_RX	GTSR4C_RX_CH3_P	4C	AT1										
G5	XCVR_RX	GTSR4C_RX_CH3_N	4C	AT3										
G6	POWER	GND	-	-										
G7	POWER	GND	-	-										
G8	XCVR_RX	GTSR4C_RX_CH1_P	4C	AY1										
G9	XCVR_RX	GTSR4C_RX_CH1_N	4C	AY3										
G10	POWER	GND	-	-										
G11	POWER	GND	-	-										
G12	XCVR_REFCLK	REFCLK_GTSR4C_CH1_P	4C	AV19										
G13	XCVR_REFCLK	REFCLK_GTSR4C_CH1_N	4C	AV17										
G14	POWER	GND	-	-										
G15	POWER	GND	-	-										
G16	XCVR_RX	REFCLK_GTSR4C_RX_P	4C	AY17										
G17	XCVR_RX	REFCLK_GTSR4C_RX_N	4C	AY19										
G18	POWER	GND	-	-										
G19	POWER	VCC_BAT												
G20	HVIO	HVIO_6B_1	6B	BK1	HVIO_6B_1	TXCLK1	Data_Ctrl1.BK1							
G21	HVIO	HVIO_6B_3	6B	BK2	HVIO_6B_3	TXCLK3	Data_Ctrl3.BK2							
G22	HVIO	HVIO_6B_4	6B	BM1	HVIO_6B_4	TXCLK4	Data_Ctrl4.BM1							
G23	HVIO	HVIO_6B_5	6B	BP1	HVIO_6B_5	PIN_PERST_N_R4A_1	TXCLK5	Data_Ctrl5.BP1						
G24	HVIO	HVIO_6B_7	6B	BT2	HVIO_6B_7	PIN_PERST_N_R4C_1	TXCLK7	Data_Ctrl7.BT2						
G25	HVIO	HVIO_6B_9	6B	BU4	HVIO_6B_9	PLLREFCLK1	TXCLK9	RXCLK1	Data_Ctrl9.BU4					
G26	HVIO	HVIO_6B_11	6B	BU8	HVIO_6B_11	SOURCE_SYNC_CLK1	TXCLK11	RXCLK3	Data_Ctrl11.BU8					
G27	HVIO	HVIO_6B_18	6B	BU18	HVIO_6B_18	TXCLK18	Data_Ctrl18.BU18							
G28	HVIO	HVIO_6B_17	6B	BV20	HVIO_6B_17	TXCLK17	Data_Ctrl17.BV20							
G29	HVIO	HVIO_6B_19	6B	BU23	HVIO_6B_19	TXCLK19	Data_Ctrl19.BU23							
G30	HVIO	HVIO_ENABLE												
G31	POWER	VCCIO_5A5B	5A & 5B	-										
G32	POWER	VCCIO_5A5B	5A & 5B	-										
G33	POWER	GND	-	-										
G34	XCVR_TX	GTSL1C_TX_CH0_N	1C	AP72										
G35	XCVR_TX	GTSL1C_TX_CH0_P	1C	AP75										
G36	POWER	GND	-	-										
G37	POWER	GND	-	-										
G38	XCVR_RX	GTSL1B_RX_CH0_N	1B	BA79										
G39	XCVR_RX	GTSL1B_RX_CH0_P	1B	BA81										
G40	POWER	GND	-	-										
G41	POWER	GND	-	-										
G42	XCVR_RX	GTSL1B_RX_CH2_N	1B	AU79										
G43	XCVR_RX	GTSL1B_RX_CH2_P	1B	AU81										
G44	POWER	GND	-	-										
G45	POWER	GND	-	-										
G46	XCVR_RX	GTSL1C_RX_CH0_N	1C	AM79										
G47	XCVR_RX	GTSL1C_RX_CH0_P	1C	AM81										
G48	POWER	GND	-	-										
G49	POWER	GND	-	-										
G50	SDM I/O	CONF_DONE	SDM	BN46										



Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10
H1	POWER	GND	-	-										
H2	XCVR_TX	GTSR4C_TX_CH3_P	4C	AR9										
H3	XCVR_TX	GTSR4C_TX_CH3_N	4C	AR13										
H4	POWER	GND	-	-										
H5	POWER	GND	-	-										
H6	XCVR_TX	GTSR4C_TX_CH2_P	4C	AU9										
H7	XCVR_TX	GTSR4C_TX_CH2_N	4C	AU13										
H8	POWER	GND	-	-										
H9	POWER	GND	-	-										
H10	XCVR_TX	GTSR4C_TX_CH1_P	4C	AW9										
H11	XCVR_TX	GTSR4C_TX_CH1_N	4C	AW13										
H12	POWER	GND	-	-										
H13	POWER	GND	-	-										
H14	XCVR_TX	GTSR4C_TX_CH0_P	4C	BA9										
H15	XCVR_TX	GTSR4C_TX_CH0_N	4C	BA13										
H16	POWER	GND	-	-										
H17	POWER	GND	-	-										
H18	HVIO	HVIO_6B_2	6B	BG1	HVIO_6B_2	TXCLK2	Data_Ctrl2.BG1							
H19	HVIO	HVIO_6B_6	6B	BM2	HVIO_6B_6	PIN_PERST_N_R4B_1	TXCLK6	Data_Ctrl6.BM2						
H20	HVIO	HVIO_6B_8	6B	BF2	HVIO_6B_8	TXCLK8	Data_Ctrl8.BF2							
H21	HVIO	HVIO_6B_10	6B	BU2	HVIO_6B_10	PLLREFCLK2	TXCLK10	RXCLK2	Data_Ctrl10.BU2					
H22	HVIO	HVIO_6B_12	6B	BV8	HVIO_6B_12	SOURCE_SYNC_CLK2	TXCLK12	RXCLK4	Data_Ctrl12.BV8					
H23	HVIO	HVIO_6B_13	6B	BV12	HVIO_6B_13	TXCLK13	Data_Ctrl13.BV12							
H24	HVIO	HVIO_6B_16	6B	BV16	HVIO_6B_16	TXCLK16	Data_Ctrl16.BV16							
H25	HVIO	HVIO_6B_14	6B	BU12	HVIO_6B_14	TXCLK14	Data_Ctrl14.BU12							
H26	HVIO	HVIO_6B_15	6B	BV18	HVIO_6B_15	TXCLK15	Data_Ctrl15.BV18							
H27	HVIO	HVIO_6B_20	6B	BU20	HVIO_6B_20	TXCLK20	Data_Ctrl20.BU20							
H28	POWER	GND	-	-										
H29	SDM I/O	TCK	SDM	BJ58										
H30	SDM I/O	TDO	SDM	BN55										
H31	SDM I/O	TMS	SDM	BJ56										
H32	SDM I/O	TDI	SDM	BJ53										
H33	SDM I/O	nSTATUS	SDM	BV32										
H34	SDM I/O	nCONFIG	SDM	BU32										
H35	POWER	GND	-	-										
H36	XCVR_TX	GTSLIB_TX_CH0_N	1B	BB72										
H37	XCVR_TX	GTSLIB_TX_CH0_P	1B	BB75										
H38	POWER	GND	-	-										
H39	POWER	GND	-	-										
H40	XCVR_TX	GTSLIB_TX_CH1_N	1B	AY72										
H41	XCVR_TX	GTSLIB_TX_CH1_P	1B	AY75										
H42	POWER	GND	-	-										
H43	POWER	GND	-	-										
H44	XCVR_TX	GTSLIB_TX_CH2_N	1B	AV72										
H45	XCVR_TX	GTSLIB_TX_CH2_P	1B	AV75										
H46	POWER	GND	-	-										
H47	POWER	GND	-	-										
H48	XCVR_TX	GTSLIB_TX_CH3_N	1B	AT72										
H49	XCVR_TX	GTSLIB_TX_CH3_P	1B	AT75										
H50	POWER	GND	-	-										



ELECTRICAL CHARACTERISTICS

Table 7: Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VCC_IN	Voltage supply, +5V to +12V input		5	12.0	13.2	Volts
I _{12.0}	Quiescent Current draw	12.0 volt input, 1333 MHz LPDDR4, no FPGA fabric, Linux prompt	TBD	TBS	TBS	mA
I _{12.0-max}	Max current draw	12.0 volt input		TBS	5	A
	1. Power utilization of the MitySOM-A5E is heavily dependent on end-user application. Major factors include: ARM CPU PLL configuration, CPU Utilization, and external DDR4 RAM utilization. See section Power Interfaces for more info.					

ORDERING INFORMATION

The following table lists the standard module configurations. For availability, price, and minimum order quantity of these configurations, or to inquire about a development kit for these products, contact Critical Link via email at info@criticallink.com.

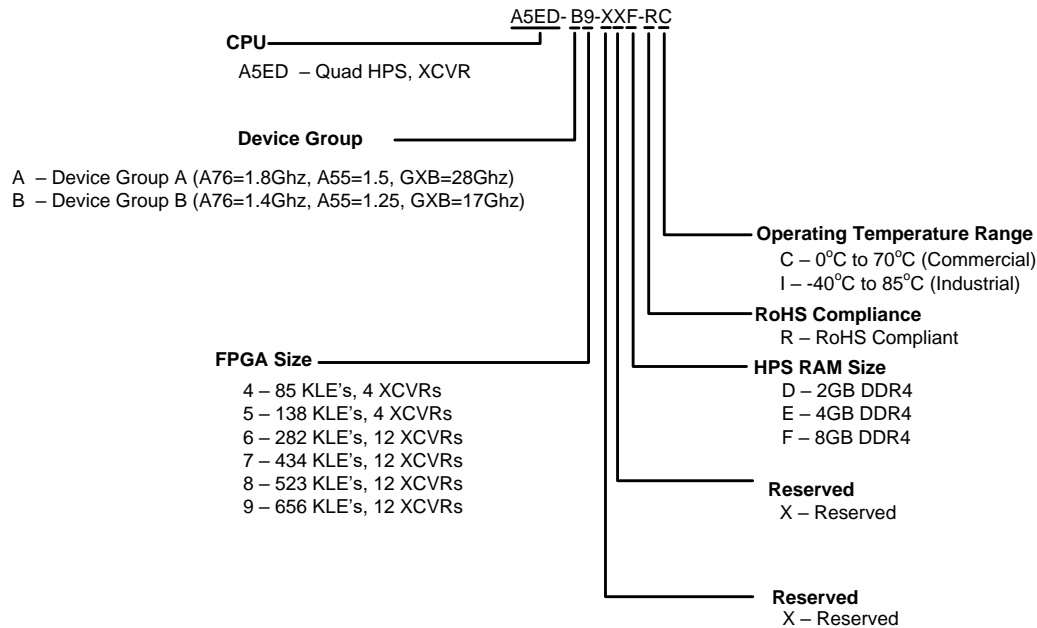
Table 8: Standard Model Numbers

Model / Part Number	FPGA KLE	CPU Speed Grade	HPS RAM (32-bit)	On-board Flash	Component Temperature Ratings
A5ED-B9-XXF-RI-X*	656	1.4GHz	8GB	256 MBit	-40°C to 85°C

- -X suffixes are preproduction silicon

MitySOM-A5E Module Family Model Number Guide

If a module suitable for your specific application is not found in **Error! Reference source not found.** please reference the following MitySOM-A5E model number decoder for configuring a custom module. Please contact your Critical Link representative to determine pricing, lead-time and availability of a custom module.



MECHANICAL INTERFACE

A bottom view mechanical outline of the MitySOM-A5E is illustrated in **Error! Reference source not found.**, below. All dimensions are in mils (0.001”). The alignment holes for the board to board interfaces are shown.

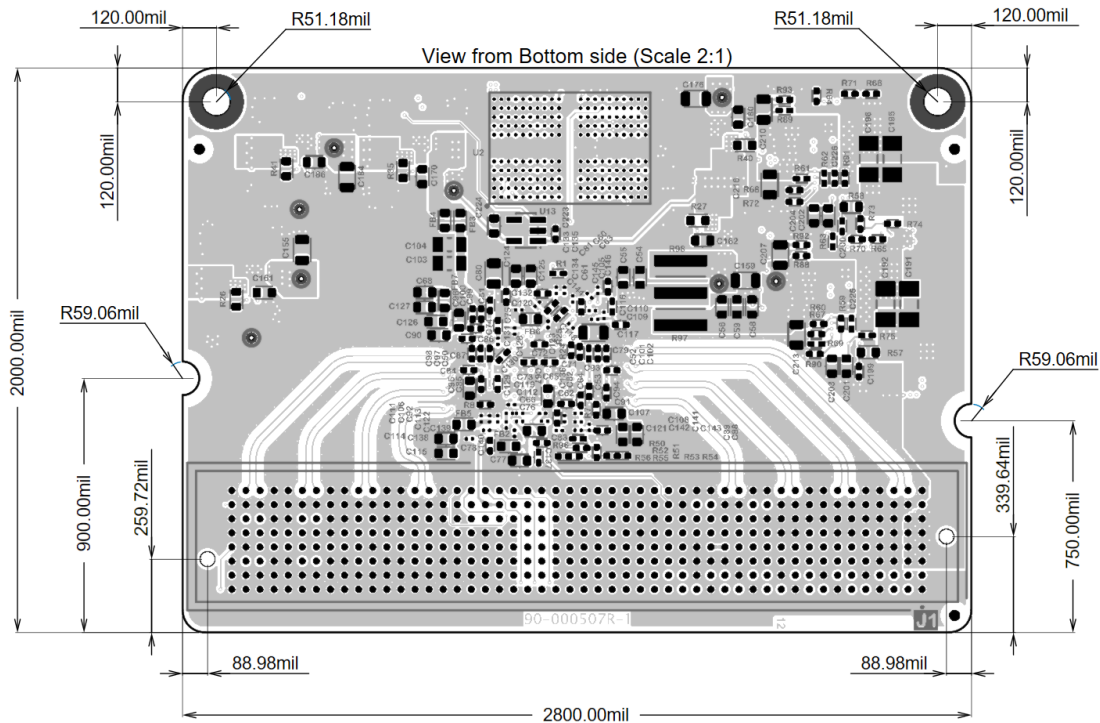


Figure 3 MitySOM-A5E Mechanical Outline, View From Bottom

REVISION HISTORY

Revision	Date	Change Description
A	March 21, 2024	Preliminary Release for early adopters

FOOTNOTES