MitySOM™ Document

Document: MitySOM-A5E Standard / Mini Carrier Board Design Guide

Revision: 1.0

Date: Nov 5, 2025

1 Overview

1.1 Fast Facts for Getting Started

Facts	MitySOM-A5E / MitySOM-A5E Mini
Required socket connector(s)	Samtec SEAM-50-02.0-L-08-2-A-K-TR, 7mm stacked height (or taller) 2 connectors needed for MitySOM-A5E, 1 connector needed for MitySOM-A5E mini
Voltage required	5-12V Main Input, 1.1-1.3V for HSIO banks, 1.8/2.5/3.3V for HVIO Banks, 1.8V for HPS
I/O Bank Voltages	HPS IO: 1.8V HSIO: 1.1-1.3V depending on desired IO standard HVIO: 1.8V, 2.5V, or 3.3V depending on desired IO standard
HPS Peripherals*	Up to 2 USB 2.0 ULPI Up to 1 USB 3.1 Gen 1 Super Speed Controller Up to 2 I3C Ports Up to 5 I2C Ports (note: I2C1 is required for configuration to support on-SOM devices) Up to 2 SPI Ports Up to 2 UARTS (note one UART should be configured for console IO) Up to 3 Ethernet MACs (10/100/1000/2500 Mbps) with TSN Support
Supported HSIO Standards**	LVDS / True Differential MIPI CSI D-PHY MIPI DSI D-PHY +1.0 -> +1.3V LVTTL (for LPDDR4 / LPDDR5) +1.1 -> +1.3V LVCMOS Single Ended IO
Supported HVIO Standards**	1.8V LVCMOS Single Ended IO 2.5V LVCMOS Single Ended IO 3.3V LVCMOS Single Ended IO
Multi-gigabit Transceivers***	MitySOM-A5E: up to 24 pairs RX/TX 6 pair CLK MitySOM-A5E Mini: up to 12 pairs RX/TX 4 pair CLK
Memory Options	MitySOM-A5E: up to 8 GB LPDDR4 @ 1333 MHz HPS (shared with FPGA), up to 8 GB LPDDR4 @ 1333 MHz FPGA MItySOM-A5E Mini: up to 8 GB LPDDR4 @ 1333 MHz HPS (shared with FPGA)
*Peripherals share pins, see SOM and Agilex 5 datasheet and HPS Technical Reference Manual for specific pin-multiplexing options ** For complete information on HPS, HSIO, HVIO supported standards, refer to the Agilex 5 datasheet. *** Number of available lanes vary with FPGA density option. See Datasheet for more information.	

1.2 Introduction

The MitySOM-A5E Family consists of 2 System on Module (SOM) designs: The MitySOM-A5E (referred to as the MitySOM-A5E Standard in this document), and the MitySOM-A5E Mini. These modules are designed to be easy to integrate into end-user embedded systems. Figure 1 and Figure 2 show the top and bottom views of the MitySOM-A5E Standard and MitySOM-A5E Mini modules, respectively. The modules integrate many crucial elements of an embedded system and do so with an established design framework utilizing a common set of core libraries. End-user design of the application PCB is also intended to be as simple as possible, allowing the PCB designer to concentrate on the custom I/O interfaces – especially analog & mixed-signal – instead of getting distracted with the learning curve of designing a brand new embedded digital system from scratch.

Developers are encouraged to review the MitySOM-A5E Standard and MitySOM-A5E Mini Development Kit design schematics, available on the Critical Link support site. The Development Kits have been qualified and there is a full software support package already available for the interfaces on the board. Customers interested in the Altium CAD design files for either kit should contact Critical Link for access.

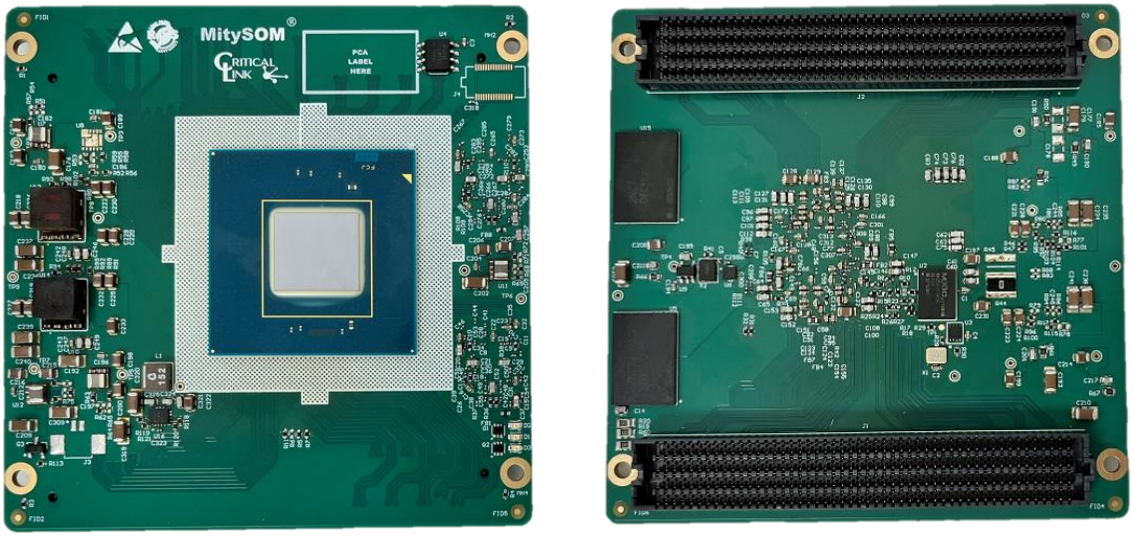

Figure 1 MitySOM-A5E Standard SOM, top and bottom view, 82x82mm

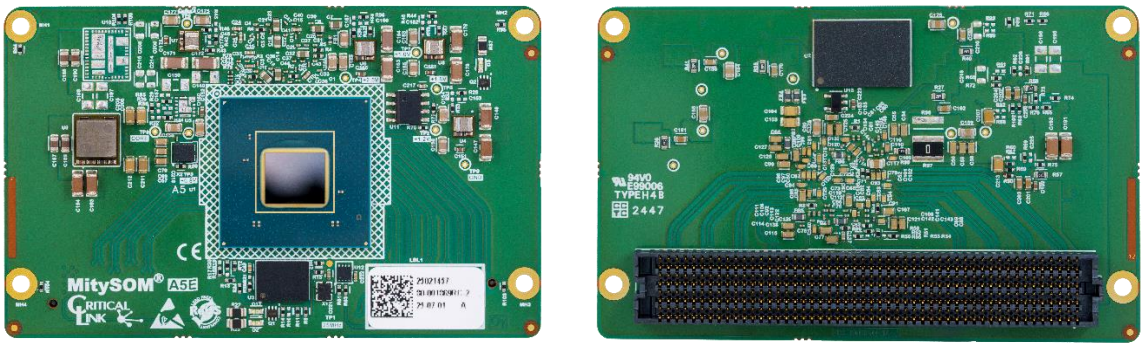

Figure 2 MitySOM-A5E Mini SOM, top and bottom view, 50.8x82mm

Links to Important Documents and Information

There are many useful documents and resources available that can be referenced when designing a system with the MitySOM-A5E Family modules which are listed below. It is recommended that the information on the Altera webpages be reviewed often for updates.

Document	Link
MitySOM-A5E Standard Data Sheet	https://www.criticallink.com/wp-content/uploads/MitySOM-A5E-Standard-Processor-Datasheet.pdf
MitySOM-A5E Mini Data Sheet	https://www.criticallink.com/wp-content/uploads/60-000087-MitySOM-A5E-Mini-Processor-Datasheet.pdf
MitySOM-A5E Family Support Site	https://support.criticallink.com/redmine/projects/mitysom_a5/wiki
Agilex 5 Data sheet	https://www.intel.com/content/www/us/en/docs/programmable/813918/current.html
Agilex 5 Family Overview	https://www.intel.com/content/www/us/en/docs/programmable/762191/current/overview-of-the-fpgas-and-socs.html
Agilex 5 HPS Technical Reference Manual	https://cdrdv2.intel.com/v1/dl/getContent/864050?fileName=mnl-814346-864050.pdf
Agilex 5 Device Configuration User Guide	https://www.intel.com/content/www/us/en/docs/programmable/813773/25-1/device-configuration-user-guide-fpgas.html
Agilex 5 General Purpose I/O Overview	https://www.intel.com/content/www/us/en/docs/programmable/813934/25-1-1/general-purpose-i-o-overview.html
Agilex 5 LVDS SERDES User Guide	https://www.intel.com/content/www/us/en/docs/programmable/813929/25-1-1/lvds-serdes-overview.html

2 Connectors

The MitySOM-A5E Standard utilizes two 400 pin board-to-board stacking Samtec SEARAY™ series connectors, SEAF-50-05.0-L-08-2-A-K-TR, for connectivity with the end user application PCB. These connectors were chosen for its high density, high performance, compact size, and ease of procurement. The stacking height of the board-to-board interface can range from 7 to 16 mm are based on the selected mating connectors for the carrier card. For 7mm stacking height, the Samtec SEAM-50-02.0-L-08-2-A-K-TR connector is recommended.

The MitySOM-A5E Mini uses only 1 of the board-to-board stacking connectors.

The MitySOM-A5E Standard uses one of the two connectors for power input, HPS IO connectivity, HVIO Banks 5A/5B/6A/6B/6C/6D, 24 pins of HSIO on Bank 3A, JTAG and miscellaneous SOM management signals, and up to 12 Transceiver TX/RX Pairs. This connector is electrically compatible with the MitySOM-A5E Mini connector (i.e., it should be safe to plug a MitySOM-A5E Mini into the J1 slot of a MitySOM-A5E Standard carrier card interface).

The MitySOM-A5E Standard second connector is used to provide access to HSIO Banks 2B (96 pins) and 2A (96 pins), their reference voltage input pins (to allow selection by the carrier card), and up to 12 additional transceiver TX/RX pairs.

The MitySOM-A5E Standard also includes a top side 30 pin connector, Samtec SS4-15-3.00-L-D-K-TR, for 232 KLE and smaller density devices, that provides additional access to 28 additional HVIO pins on Banks 6E and 6F.

Table 1 MitySOM-A5E Standard Interface Hardware Needed for Carrier Card / Interface Design

Manufacturer Part Number	Manufacturer	Quantity	Notes / Description
SEAM-50-02.0-L-08-2-A-K-TR	Samtec	2	400 Pin Interface Connector, mates with SOM J1 and J2
9774070151R	Würth Elektronik	4	Surface mount m2.5 7mm standoffs
94209A347	McMaster-Carr	4	Zinc-plated M2.5 Pan head Screw, 6mm
ST4-15-1.00-L-D-P-TR	Samtec	1	Optional top side connector for SOMs with 232 KLE or less. Requires separate interface board for mating.

Table 2 MitySOM-A5E Mini Interface Hardware Needed for Carrier Card / Interface Design

Manufacturer Part Number	Manufacturer	Quantity	Notes / Description
SEAM-50-02.0-L-08-2-A-K-TR	Samtec	1	400 Pin Interface Connector, mates with SOM J1
9774070151R	Würth Elektronik	4	Surface mount m2.5 7mm standoffs
94209A347	McMaster-Carr	4	Zinc-plated M2.5 Pan head Screw, 6mm

2.1 Connector compatibility

The MitySOM-A5E Standard and MitySOM-A5E Mini are designed to be electrically compatible. It should be possible to design a carrier card to support both the Standard and the Mini (with limited HSIO and transceiver availability). The electrical pinout for the SOMs is unique to the SOM design, other off-the-shelf circuit cards using the same connector should not be considered compatible.

There is some difference in the logical pin mapping on connector 1 between the MitySOM-A5E Standard and the MitySOM-A5E Mini. HVIO Bank 6A and Bank 6C positions were swapped, and HVIO Bank 6B and Bank 6D positions were swapped. The following tables highlight the differences between the two connectors.

Pin	Class	MitySOM-A5E Standard	MitySOM-A5E Mini		Pin	Class	MitySOM-A5E Standard	MitySOM-A5E Mini
A01	POWER	GND	GND		B01	POWER OUT	+1.8V	+1.8V
A02	HSIO	DIFF_IO_3A_T16_N	DIFF_IO_3A_T16_N		B02	POWER OUT	+1.8V	+1.8V
A03	HSIO	DIFF_IO_3A_T16_P	DIFF_IO_3A_T16_P		B03	HSIO	DIFF_IO_3A_T13_P	DIFF_IO_3A_T13_P
A04	POWER	GND	GND		B04	HSIO	DIFF_IO_3A_T13_N	DIFF_IO_3A_T13_N
A05	HSIO	DIFF_IO_3A_T14_P	DIFF_IO_3A_T14_P		B05	POWER	GND	GND
A06	HSIO	DIFF_IO_3A_T14_N	DIFF_IO_3A_T14_N		B06	HSIO	DIFF_IO_3A_T15_N	DIFF_IO_3A_T15_N
A07	POWER	GND	GND		B07	HSIO	DIFF_IO_3A_T15_P	DIFF_IO_3A_T15_P
A08	HSIO	DIFF_IO_3A_T17_P	DIFF_IO_3A_T17_P		B08	POWER	GND	GND
A09	HSIO	DIFF_IO_3A_T17_N	DIFF_IO_3A_T17_N		B09	HSIO	DIFF_IO_3A_T18_P	DIFF_IO_3A_T18_P
A10	POWER	GND	GND		B10	HSIO	DIFF_IO_3A_T18_N	DIFF_IO_3A_T18_N
A11	HSIO	DIFF_IO_3A_T24_N	DIFF_IO_3A_T24_N		B11	POWER	GND	GND
A12	HSIO	DIFF_IO_3A_T24_P	DIFF_IO_3A_T24_P		B12	HSIO	DIFF_IO_3A_T23_N	DIFF_IO_3A_T23_N
A13	POWER	GND	GND		B13	HSIO	DIFF_IO_3A_T23_P	DIFF_IO_3A_T23_P
A14	HSIO	DIFF_IO_3A_T22_P	DIFF_IO_3A_T22_P		B14	POWER	GND	GND
A15	HSIO	DIFF_IO_3A_T22_N	DIFF_IO_3A_T22_N		B15	HSIO	DIFF_IO_3A_T21_P	DIFF_IO_3A_T21_P
A16	POWER	GND	GND		B16	HSIO	DIFF_IO_3A_T21_N	DIFF_IO_3A_T21_N
A17	HSIO	DIFF_IO_3A_T20_P	DIFF_IO_3A_T20_P		B17	POWER	GND	GND
A18	HSIO	DIFF_IO_3A_T20_N	DIFF_IO_3A_T20_N		B18	HSIO	DIFF_IO_3A_T19_P	DIFF_IO_3A_T19_P
A19	POWER	VCCIO_6C6D	VCCIO_6A6B		B19	HSIO	DIFF_IO_3A_T19_N	DIFF_IO_3A_T19_N
A20	POWER	VCCIO_6C6D	VCCIO_6A6B		B20	POWER OUT	+1.1V	+1.1V
A21	HVIO	HVIO_5A_1	HVIO_5A_1		B21	POWER OUT	+1.1V	+1.1V
A22	HVIO	HVIO_5A_3	HVIO_5A_3		B22	HVIO	HVIO_5A_19	HVIO_5A_19
A23	HVIO	HVIO_5A_6	HVIO_5A_6		B23	HVIO	HVIO_5A_20	HVIO_5A_20
A24	HVIO	HVIO_5A_5	HVIO_5A_5		B24	HVIO	HVIO_5A_8	HVIO_5A_8
A25	HVIO	HVIO_5A_11	HVIO_5A_11		B25	HVIO	HVIO_5A_7	HVIO_5A_7
A26	HVIO	HVIO_5A_10	HVIO_5A_10		B26	HVIO	HVIO_5A_4	HVIO_5A_4
A27	HVIO	HVIO_5A_12	HVIO_5A_12		B27	HVIO	HVIO_5A_18	HVIO_5A_18
A28	HVIO	HVIO_5A_16	HVIO_5A_16		B28	HVIO	HVIO_5A_17	HVIO_5A_17
A29	HVIO	HVIO_5A_2	HVIO_5A_2		B29	HVIO	HVIO_5A_9	HVIO_5A_9
A30	HVIO	HVIO_5A_15	HVIO_5A_15		B30	HVIO	HVIO_5A_14	HVIO_5A_14
A31	POWER	GND	GND		B31	HVIO	HVIO_5A_13	HVIO_5A_13
A32	HPS	I2C1_SDA	I2C1_SDA		B32	POWER	GND	GND
A33	HPS	I2C1_SCL	I2C1_SCL		B33	POWER	GND	GND
A34	POWER	GND	GND		B34	XCVR_TX	GTSL1C_TX_CH1_N	GTSL1C_TX_CH1_N
A35	POWER	GND	GND		B35	XCVR_TX	GTSL1C_TX_CH1_P	GTSL1C_TX_CH1_P
A36	XCVR_RX	GTSL1B_RX_CH1_N	GTSL1B_RX_CH1_N		B36	POWER	GND	GND
A37	XCVR_RX	GTSL1B_RX_CH1_P	GTSL1B_RX_CH1_P		B37	POWER	GND	GND
A38	POWER	GND	GND		B38	XCVR_TX	GTSL1C_TX_CH2_N	GTSL1C_TX_CH2_N
A39	POWER	GND	GND		B39	XCVR_TX	GTSL1C_TX_CH2_P	GTSL1C_TX_CH2_P
A40	XCVR_RX	GTSL1B_RX_CH3_N	GTSL1B_RX_CH3_N		B40	POWER	GND	GND
A41	XCVR_RX	GTSL1B_RX_CH3_P	GTSL1B_RX_CH3_P		B41	POWER	GND	GND
A42	POWER	GND	GND		B42	XCVR_TX	GTSL1C_TX_CH3_N	GTSL1C_TX_CH3_N
A43	POWER	GND	GND		B43	XCVR_TX	GTSL1C_TX_CH3_P	GTSL1C_TX_CH3_P
A44	XCVR_RX	GTSL1C_RX_CH1_N	GTSL1C_RX_CH1_N		B44	POWER	GND	GND
A45	XCVR_RX	GTSL1C_RX_CH1_P	GTSL1C_RX_CH1_P		B45	POWER	GND	GND
A46	POWER	GND	GND		B46	XCVR_TX	GTSL1C_RX_CH2_N	GTSL1C_RX_CH2_N
A47	POWER	GND	GND		B47	XCVR_TX	GTSL1C_RX_CH2_P	GTSL1C_RX_CH2_P
A48	XCVR_RX	GTSL1C_RX_CH3_N	GTSL1C_RX_CH3_N		B48	POWER	GND	GND
A49	XCVR_RX	GTSL1C_RX_CH3_P	GTSL1C_RX_CH3_P		B49	POWER	GND	GND
A50	POWER	GND	GND		B50		INIT_DONE	INIT_DONE

Pin	Class	MitySOM-A5E Standard	MitySOM-A5E Mini		Pin	Class	MitySOM-A5E Standard	MitySOM-A5E Mini
C01	POWER	VCC_IN	VCC_IN		D01	POWER	VCC_IN	VCC_IN
C02	POWER	VCC_IN	VCC_IN		D02	POWER	VCC_IN	VCC_IN
C03	POWER	GND	GND		D03	POWER	GND	GND
C04	POWER	GND	GND		D04	POWER	GND	GND
C05	HVIO	HVIO_6A_1	HVIO_6C_1		D05	HVIO	HVIO_6B_18	HVIO_6D_18
C06	HVIO	HVIO_6B_17	HVIO_6D_17		D06	HVIO	HVIO_6B_19	HVIO_6D_19
C07	HVIO	HVIO_6B_14	HVIO_6D_14		D07	HVIO	HVIO_6B_15	HVIO_6D_15
C08	HVIO	HVIO_6B_9	HVIO_6D_9		D08	HVIO	HVIO_6B_20	HVIO_6D_20
C09	HVIO	HVIO_6B_10	HVIO_6D_10		D09	HVIO	HVIO_6B_7	HVIO_6D_7
C10	HVIO	HVIO_6B_3	HVIO_6D_3		D10	HVIO	HVIO_6A_3	HVIO_6C_3
C11	HVIO	HVIO_6A_10	HVIO_6C_10		D11	HVIO	HVIO_6B_4	HVIO_6D_4
C12	HVIO	HVIO_6A_12	HVIO_6C_12		D12	HVIO	HVIO_6A_11	HVIO_6C_11
C13	HVIO	HVIO_6B_1	HVIO_6D_1		D13	HVIO	HVIO_6A_14	HVIO_6C_14
C14	HVIO	HVIO_6A_9	HVIO_6C_9		D14	HVIO	HVIO_6A_2	HVIO_6C_2
C15	POWER	GND	GND		D15	POWER	VCCIO_6A6B	VCCIO_6C6D
C16	POWER	GND	GND		D16	POWER	VCCIO_6A6B	VCCIO_6C6D
C17	POWER	GND	GND		D17	POWER	GND	GND
C18	HVIO	HVIO_5B_19	HVIO_5B_19		D18	HVIO	HVIO_5B_3	HVIO_5B_3
C19	HVIO	HVIO_5B_20	HVIO_5B_20		D19	HVIO	HVIO_5B_4	HVIO_5B_4
C20	HVIO	HVIO_5B_18	HVIO_5B_18		D20	HVIO	HVIO_5B_1	HVIO_5B_1
C21	HVIO	HVIO_5B_16	HVIO_5B_16		D21	HVIO	HVIO_5B_7	HVIO_5B_7
C22	HVIO	HVIO_5B_17	HVIO_5B_17		D22	HVIO	HVIO_5B_2	HVIO_5B_2
C23	HVIO	HVIO_5B_8	HVIO_5B_8		D23	HVIO	HVIO_5B_5	HVIO_5B_5
C24	HVIO	HVIO_5B_9	HVIO_5B_9		D24	HVIO	HVIO_5B_6	HVIO_5B_6
C25	HVIO	HVIO_5B_14	HVIO_5B_14		D25	HVIO	HVIO_5B_11	HVIO_5B_11
C26	HVIO	HVIO_5B_13	HVIO_5B_13		D26	HVIO	HVIO_5B_10	HVIO_5B_10
C27	HVIO	HVIO_5B_15	HVIO_5B_15		D27	HVIO	HVIO_5B_12	HVIO_5B_12
C28	POWER	GND	GND		D28	POWER	GND	GND
C29	SDM	HPS_COLD_nRESET	HPS_COLD_nRESET		D29	POWER	GND	GND
C30	SDM	SDM_IO13	SDM_IO13		D30	GPIO	GPIO0_IO3	GPIO0_IO3
C31	SDM	SDM_IO8	SDM_IO8		D31	GPIO	GPIO0_IO19	GPIO0_IO19
C32	HPS	GPIO0_IO5	GPIO0_IO5		D32	GPIO	GPIO0_IO17	GPIO0_IO17
C33	HPS	GPIO0_IO15	GPIO0_IO15		D33	GPIO	GPIO0_IO7	GPIO0_IO7
C34	POWER	GND	GND		D34	GPIO	GPIO0_IO9	GPIO0_IO9
C35	POWER	GND	GND		D35	GPIO	GPIO0_IO6	GPIO0_IO6
C36	HPS	GPIO0_IO11	GPIO0_IO11		D36	GPIO	GPIO0_IO10	GPIO0_IO10
C37	HPS	GPIO0_IO1	GPIO0_IO1		D37	GPIO	GPIO0_IO0	GPIO0_IO0
C38	POWER	GND	GND		D38	GPIO	GPIO0_IO16	GPIO0_IO16
C39	POWER	GND	GND		D39	GPIO	GPIO1_IO7	GPIO1_IO7
C40	HPS	GPIO1_IO17	GPIO1_IO17		D40	POWER	GND	GND
C41	HPS	GPIO1_IO21	GPIO1_IO21		D41	GPIO	GPIO1_IO19	GPIO1_IO19
C42	POWER	GND	GND		D42	GPIO	GPIO1_IO10	GPIO1_IO10
C43	POWER	GND	GND		D43	GPIO	GPIO1_IO0	GPIO1_IO0
C44	XCVR_REFCLK	REFCLK_GTSL1B_RX_N	REFCLK_GTSL1B_RX_N		D44	GPIO	GPIO1_IO8	GPIO1_IO8
C45	XCVR_REFCLK	REFCLK_GTSL1B_RX_P	REFCLK_GTSL1B_RX_P		D45	GPIO	GPIO1_IO11	GPIO1_IO11
C46	POWER	GND	GND		D46	GPIO	GPIO1_IO16	GPIO1_IO16
C47	POWER	GND	GND		D47	GPIO	GPIO1_IO23	GPIO1_IO23
C48	XCVR_REFCLK	REFCLK_GTSL1C_CH1_P	REFCLK_GTSL1C_CH1_P		D48	GPIO	GPIO1_IO14	GPIO1_IO14
C49	XCVR_REFCLK	REFCLK_GTSL1C_CH1_N	REFCLK_GTSL1C_CH1_N		D49	POWER	GND	GND
C50	POWER	GND	GND		D50	MISC	HPS_CLKIN	HPS_CLKIN

Pin	Class	MitySOM-A5E Standard	MitySOM-A5E Mini		Pin	Class	MitySOM-A5E Standard	MitySOM-A5E Mini
E01	POWER	VCC_IN	VCC_IN		F01	POWER	VCC_IN	VCC_IN
E02	POWER	VCC_IN	VCC_IN		F02	POWER	VCC_IN	VCC_IN
E03	POWER	GND	GND		F03	POWER	GND	GND
E04	HVIO	HVIO_6B_16	HVIO_6D_16		F04	POWER	GND	GND
E05	HVIO	HVIO_6B_12	HVIO_6D_12		F05	POWER	GND	GND
E06	POWER	GND	GND		F06	XCVR_RX	GTSL1A_RX_CH2_P	GTSL1A_RX_CH2_P
E07	POWER	GND	GND		F07	XCVR_RX	GTSL1A_RX_CH2_N	GTSL1A_RX_CH2_N
E08	HVIO	HVIO_6B_13	HVIO_6D_13		F08	POWER	GND	GND
E09	HVIO	HVIO_6B_11	HVIO_6D_11		F09	POWER	GND	GND
E10	POWER	GND	GND		F10	XCVR_RX	GTSL1A_RX_CH0_P	GTSL1A_RX_CH0_P
E11	POWER	GND	GND		F11	XCVR_RX	GTSL1A_RX_CH0_N	GTSL1A_RX_CH0_N
E12	HVIO	HVIO_6B_8	HVIO_6D_8		F12	POWER	GND	GND
E13	HVIO	HVIO_6B_5	HVIO_6D_5		F13	HVIO	HVIO_6B_6	HVIO_6D_6
E14	HVIO	HVIO_6A_5	HVIO_6C_5		F14	HVIO	HVIO_6B_2	HVIO_6D_2
E15	HVIO	HVIO_6A_8	HVIO_6C_8		F15	HVIO	HVIO_6A_15	HVIO_6C_15
E16	HVIO	HVIO_6A_18	HVIO_6C_18		F16	HVIO	HVIO_6A_4	HVIO_6C_4
E17	HVIO	HVIO_6A_7	HVIO_6C_7		F17	HVIO	HVIO_6A_13	HVIO_6C_13
E18	HVIO	HVIO_6A_17	HVIO_6C_17		F18	HVIO	HVIO_6A_6	HVIO_6C_6
E19	HVIO	HVIO_6A_16	HVIO_6C_16		F19	HVIO	HVIO_6A_20	HVIO_6C_20
E20	HVIO	HVIO_6A_19	HVIO_6C_19		F20	POWER	GND	GND
E21	POWER	GND	GND		F21	HVIO	HVIO_6C_16	HVIO_6A_16
E22	HVIO	HVIO_6C_13	HVIO_6A_13		F22	HVIO	HVIO_6C_17	HVIO_6A_17
E23	HVIO	HVIO_6C_18	HVIO_6A_18		F23	HVIO	HVIO_6C_19	HVIO_6A_19
E24	HVIO	HVIO_6C_10	HVIO_6A_10		F24	HVIO	HVIO_6C_12	HVIO_6A_12
E25	HVIO	HVIO_6C_14	HVIO_6A_14		F25	HVIO	HVIO_6C_15	HVIO_6A_15
E26	HVIO	HVIO_6C_20	HVIO_6A_20		F26	HVIO	HVIO_6C_8	HVIO_6A_8
E27	HVIO	HVIO_6C_6	HVIO_6A_6		F27	HVIO	HVIO_6C_11	HVIO_6A_11
E28	HVIO	HVIO_6C_9	HVIO_6A_9		F28	HVIO	HVIO_6C_2	HVIO_6A_2
E29	HVIO	HVIO_6C_7	HVIO_6A_7		F29	HVIO	HVIO_6C_4	HVIO_6A_4
E30	HVIO	HVIO_6C_3	HVIO_6A_3		F30	HVIO	HVIO_6C_1	HVIO_6A_1
E31	HVIO	HVIO_6C_5	HVIO_6A_5		F31	POWER	GND	GND
E32	POWER	GND	GND		F32	HPS	GPIO0_IO21	GPIO0_IO21
E33	HPS	GPIO0_IO18	GPIO0_IO18		F33	HPS	GPIO0_IO22	GPIO0_IO22
E34	HPS	GPIO0_IO12	GPIO0_IO12		F34	POWER	GND	GND
E35	HPS	GPIO0_IO4	GPIO0_IO4		F35	POWER	GND	GND
E36	HPS	GPIO0_IO2	GPIO0_IO2		F36	HPS	GPIO0_IO8	GPIO0_IO8
E37	HPS	GPIO0_IO13	GPIO0_IO13		F37	HPS	GPIO0_IO14	GPIO0_IO14
E38	HPS	GPIO0_IO20	GPIO0_IO20		F38	POWER	GND	GND
E39	HPS	GPIO0_IO23	GPIO0_IO23		F39	POWER	GND	GND
E40	HPS	GPIO1_IO15	GPIO1_IO15		F40	HPS	GPIO1_IO9	GPIO1_IO9
E41	HPS	GPIO1_IO5	GPIO1_IO5		F41	HPS	GPIO1_IO3	GPIO1_IO3
E42	HPS	GPIO1_IO6	GPIO1_IO6		F42	POWER	GND	GND
E43	POWER	GND	GND		F43	POWER	GND	GND
E44	HPS	GPIO1_IO1	GPIO1_IO1		F44	XCVR_REFCLK	REFCLK_GTSL1B_CH1_P	REFCLK_GTSL1B_CH1_P
E45	HPS	GPIO1_IO20	GPIO1_IO20		F45	XCVR_REFCLK	REFCLK_GTSL1B_CH1_N	REFCLK_GTSL1B_CH1_N
E46	HPS	GPIO1_IO4	GPIO1_IO4		F46	POWER	GND	GND
E47	HPS	GPIO1_IO2	GPIO1_IO2		F47	POWER	GND	GND
E48	HPS	GPIO1_IO18	GPIO1_IO18		F48	XCVR_REFCLK	REFCLK_GTSL1C_RX_P	REFCLK_GTSL1C_RX_P
E49	HPS	GPIO1_IO22	GPIO1_IO22		F49	XCVR_REFCLK	REFCLK_GTSL1C_RX_N	REFCLK_GTSL1C_RX_N
E50	POWER	GND	GND		F50	POWER	GND	GND

Pin	Class	MitySOM-A5E Standard	MitySOM-A5E Mini		Pin	Class	MitySOM-A5E Standard	MitySOM-A5E Mini
G01	MISC	CORE_EN	CORE_EN		H01	POWER	GND	GND
G02	POWER	GND	GND		H02	XCVR_TX	GTSL1A_TX_CH3_P	GTSL1A_TX_CH3_P
G03	POWER	GND	GND		H03	XCVR_TX	GTSL1A_TX_CH3_N	GTSL1A_TX_CH3_N
G04	XCVR_RX	GTSL1A_RX_CH3_P	GTSL1A_RX_CH3_P		H04	POWER	GND	GND
G05	XCVR_RX	GTSL1A_RX_CH3_N	GTSL1A_RX_CH3_N		H05	POWER	GND	GND
G06	POWER	GND	GND		H06	XCVR_TX	GTSL1A_TX_CH2_P	GTSL1A_TX_CH2_P
G07	POWER	GND	GND		H07	XCVR_TX	GTSL1A_TX_CH2_N	GTSL1A_TX_CH2_N
G08	XCVR_RX	GTSL1A_RX_CH1_P	GTSL1A_RX_CH1_P		H08	POWER	GND	GND
G09	XCVR_RX	GTSL1A_RX_CH1_N	GTSL1A_RX_CH1_N		H09	POWER	GND	GND
G10	POWER	GND	GND		H10	XCVR_TX	GTSL1A_TX_CH1_P	GTSL1A_TX_CH1_P
G11	POWER	GND	GND		H11	XCVR_TX	GTSL1A_TX_CH1_N	GTSL1A_TX_CH1_N
G12	XCVR_REFCLK	REFCLK_GTSL1A_CH1_P	REFCLK_GTSL1A_CH1_P		H12	POWER	GND	GND
G13	XCVR_REFCLK	REFCLK_GTSL1A_CH1_N	REFCLK_GTSL1A_CH1_N		H13	POWER	GND	GND
G14	POWER	GND	GND		H14	XCVR_TX	GTSL1A_TX_CH0_P	GTSL1A_TX_CH0_P
G15	POWER	GND	GND		H15	XCVR_TX	GTSL1A_TX_CH0_N	GTSL1A_TX_CH0_N
G16	XCVR_REFCLK	REFCLK_GTSL1A_RX_P	REFCLK_GTSL1A_RX_P		H16	POWER	GND	GND
G17	XCVR_REFCLK	REFCLK_GTSL1A_RX_N	REFCLK_GTSL1A_RX_N		H17	POWER	GND	GND
G18	POWER	GND	GND		H18	HVIO	HVIO_6D_2	HVIO_6B_2
G19	POWER	VCC_BAT	VCC_BAT		H19	HVIO	HVIO_6D_6	HVIO_6B_6
G20	HVIO	HVIO_6D_1	HVIO_6B_1		H20	HVIO	HVIO_6D_8	HVIO_6B_8
G21	HVIO	HVIO_6D_3	HVIO_6B_3		H21	HVIO	HVIO_6D_10	HVIO_6B_10
G22	HVIO	HVIO_6D_4	HVIO_6B_4		H22	HVIO	HVIO_6D_12	HVIO_6B_12
G23	HVIO	HVIO_6D_5	HVIO_6B_5		H23	HVIO	HVIO_6D_13	HVIO_6B_13
G24	HVIO	HVIO_6D_7	HVIO_6B_7		H24	HVIO	HVIO_6D_16	HVIO_6B_16
G25	HVIO	HVIO_6D_9	HVIO_6B_9		H25	HVIO	HVIO_6D_14	HVIO_6B_14
G26	HVIO	HVIO_6D_11	HVIO_6B_11		H26	HVIO	HVIO_6D_15	HVIO_6B_15
G27	HVIO	HVIO_6D_18	HVIO_6B_18		H27	HVIO	HVIO_6D_20	HVIO_6B_20
G28	HVIO	HVIO_6D_17	HVIO_6B_17		H28	POWER	GND	GND
G29	HVIO	HVIO_6D_19	HVIO_6B_19		H29	SDM	TCK	TCK
G30	MISC	HVIO_ENABLE	HVIO_ENABLE		H30	SDM	TDO	TDO
G31	POWER	VCCIO_5A5B	VCCIO_5A5B		H31	SDM	TMS	TMS
G32	POWER	VCCIO_5A5B	VCCIO_5A5B		H32	SDM	TDI	TDI
G33	POWER	GND	GND		H33	SDM	nSTATUS	nSTATUS
G34	XCVR_TX	GTSL1C_TX_CH0_N	GTSL1C_TX_CH0_N		H34	SDM	nCONFIG	nCONFIG
G35	XCVR_TX	GTSL1C_TX_CH0_P	GTSL1C_TX_CH0_P		H35	POWER	GND	GND
G36	POWER	GND	GND		H36	XCVR_TX	GTSL1B_TX_CH0_N	GTSL1B_TX_CH0_N
G37	POWER	GND	GND		H37	XCVR_TX	GTSL1B_TX_CH0_P	GTSL1B_TX_CH0_P
G38	XCVR_RX	GTSL1B_RX_CH0_N	GTSL1B_RX_CH0_N		H38	POWER	GND	GND
G39	XCVR_RX	GTSL1B_RX_CH0_P	GTSL1B_RX_CH0_P		H39	POWER	GND	GND
G40	POWER	GND	GND		H40	XCVR_TX	GTSL1B_TX_CH1_N	GTSL1B_TX_CH1_N
G41	POWER	GND	GND		H41	XCVR_TX	GTSL1B_TX_CH1_P	GTSL1B_TX_CH1_P
G42	XCVR_RX	GTSL1B_RX_CH2_N	GTSL1B_RX_CH2_N		H42	POWER	GND	GND
G43	XCVR_RX	GTSL1B_RX_CH2_P	GTSL1B_RX_CH2_P		H43	POWER	GND	GND
G44	POWER	GND	GND		H44	XCVR_TX	GTSL1B_TX_CH2_N	GTSL1B_TX_CH2_N
G45	POWER	GND	GND		H45	XCVR_TX	GTSL1B_TX_CH2_P	GTSL1B_TX_CH2_P
G46	XCVR_RX	GTSL1C_RX_CH0_N	GTSL1C_RX_CH0_N		H46	POWER	GND	GND
G47	XCVR_RX	GTSL1C_RX_CH0_P	GTSL1C_RX_CH0_P		H47	POWER	GND	GND
G48	POWER	GND	GND		H48	XCVR_TX	GTSL1B_TX_CH3_N	GTSL1B_TX_CH3_N
G49	POWER	GND	GND		H49	XCVR_TX	GTSL1B_TX_CH3_P	GTSL1B_TX_CH3_P
G50	SDM	CONF_DONE	CONF_DONE		H50	POWER	GND	GND

3 Electrical Requirements

The following sections describe the various electrical requirements for the MitySOM-A5E Standard and MItySOM-A5E Mini modules.

3.1 Power Supplies

Figure 5 provides an overview of the MitySOM-A5E power scheme.

The MitySOM-A5E Standard and Mini are powered by an input voltage in the range of 5-12 Volts. Critical Link recommends using 12 Volts for applications requiring more than 10 Watts for operation. The SOM provides a CORE_EN signal which can be used to turn on (or off) the SOM power system from the carrier card. This pin is connected to a resistor divider network on the SOM as shown in the picture below and may be left disconnected if no SOM power-on control is needed. The enable threshold hysteresis is 1.2V (ramp up) and 1.0V (ramp down).

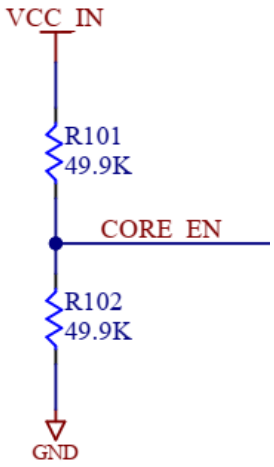

Figure 3 CORE_EN resistor divider network on SOM

The MitySOM-A5E Standard and Mini expose the Agilex 5 HVIO Bank 5A/5B (combined), 6A/6B (combined), and 6C/6D (combined) VCCIO pins. The MitySOM-A5E Standard also exposes the HSIO Bank 2A and 2B pins to the edge connector to support powering from the carrier card. HVIO Banks must use 1.8V, 2.5V, or 3.3V. HSIO Banks must use 1.0V, 1.05V, 1.1V, 1.2V, or 1.3V. Note that Bank 2A and 2B and their supply pins are not available on the MitySOM-A5E Mini. The Bank IO supplies should not be energized until the HVIO_ENABLE signal is asserted by the SOM.

In addition, the 1.8V supply used for the HPS IO and the 1.1V supply used for HSIO Bank 3A are also made available as outputs to the carrier card for powering interface circuitry. The bank assignment for each IO pin can be determined from Table 1 of the MitySOM-A5E Standard and Mini datasheet and additional information about the HSIO and HVIO Bank voltages can be found in the Altera Agilex 5 datasheet.

For secure key storage in onboard RAM, a 1.8V supply is required on the VBAT pin of interface. This supply must be continuously maintained to preserve loaded keys in the volatile RAM storage. This pin may be grounded if there is no need to store secure keys in the volatile RAM on the Agilex 5. Note: keys may also be stored in non-volatile fuses, but once this is done the keys are permanently programmed.

Figure 6 illustrates a typical carrier card power block diagram.

3.1.1 Power Supply Sequencing

The MitySOM-A5E Standard and Mini power inputs should be sequenced when powered on. There are three power groups for sequencing: the main VCC_IN input, the HPS IO pins to be run at 1.8V, and the FPGA HVIO and HSIO bank inputs and IO pins. The enabling of the FPGA HVIO and HSIO bank inputs can be accomplished using the HVIO_ENABLE (as a control pin to a load switch, supply enable, or MOSFET gate input) as shown in Figure 5. Note that the VCCIO 2A and 2B power rails are only valid for the MitySOM-A5E Standard.

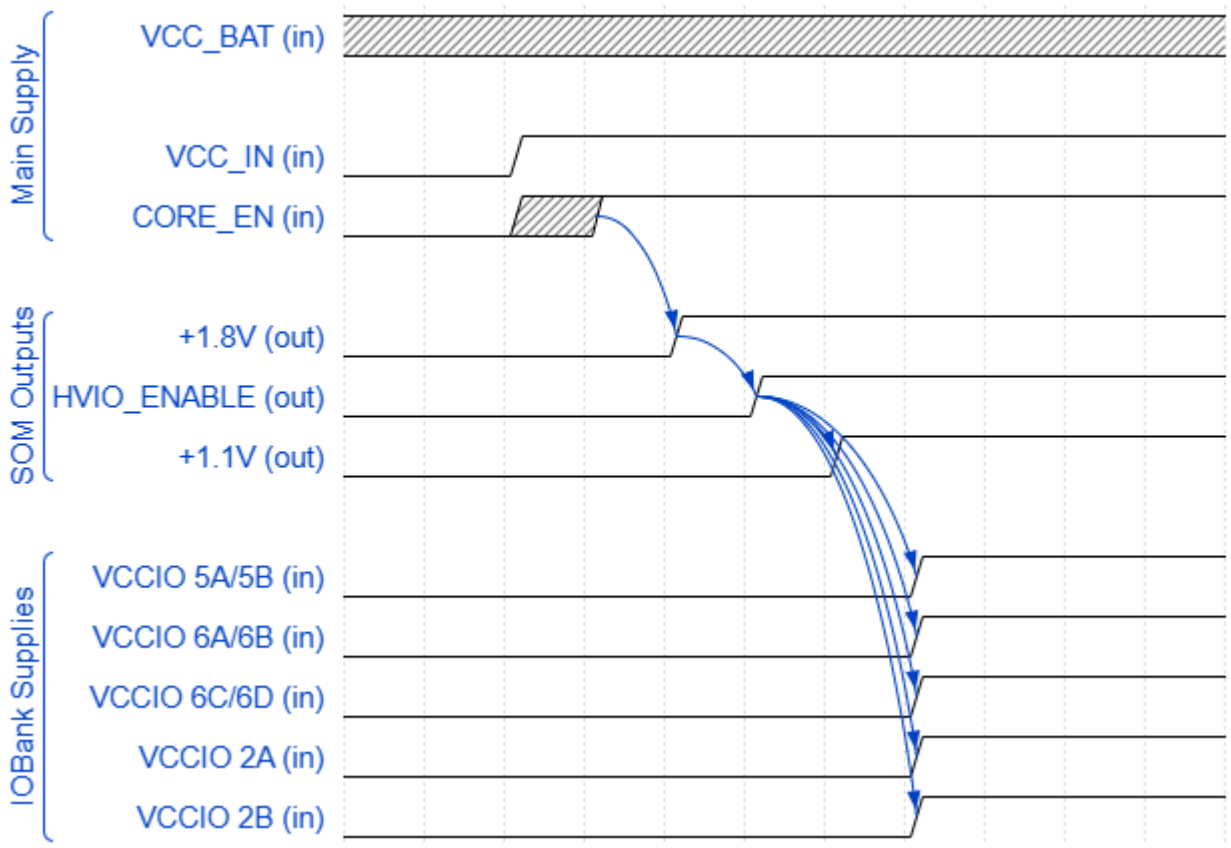

Figure 4: Example MitySOM-A5E Standard and Mini Power Up Sequence Requirements

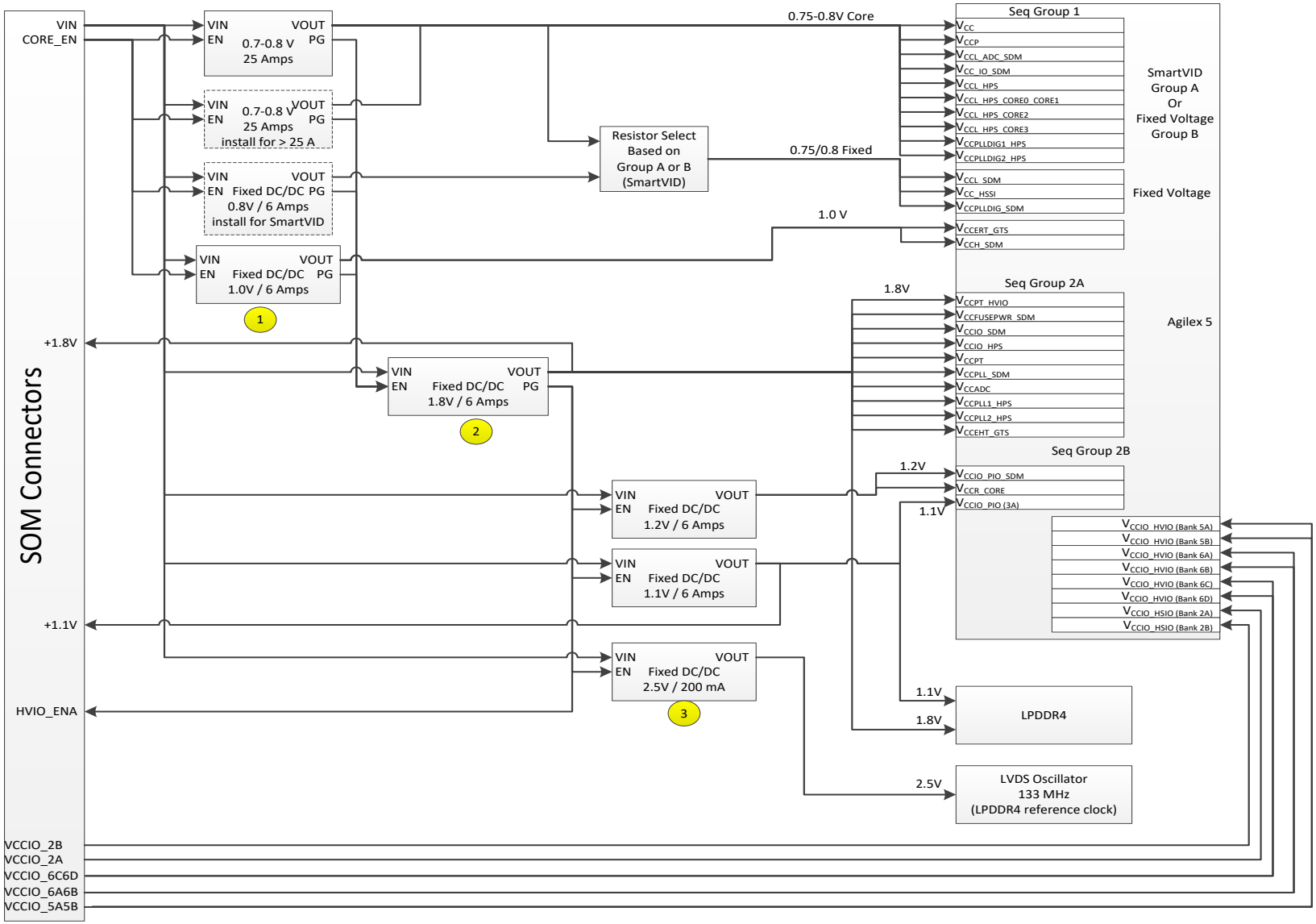

Figure 5 MitySOM-A5E Standard and Mini Power Interface Overview

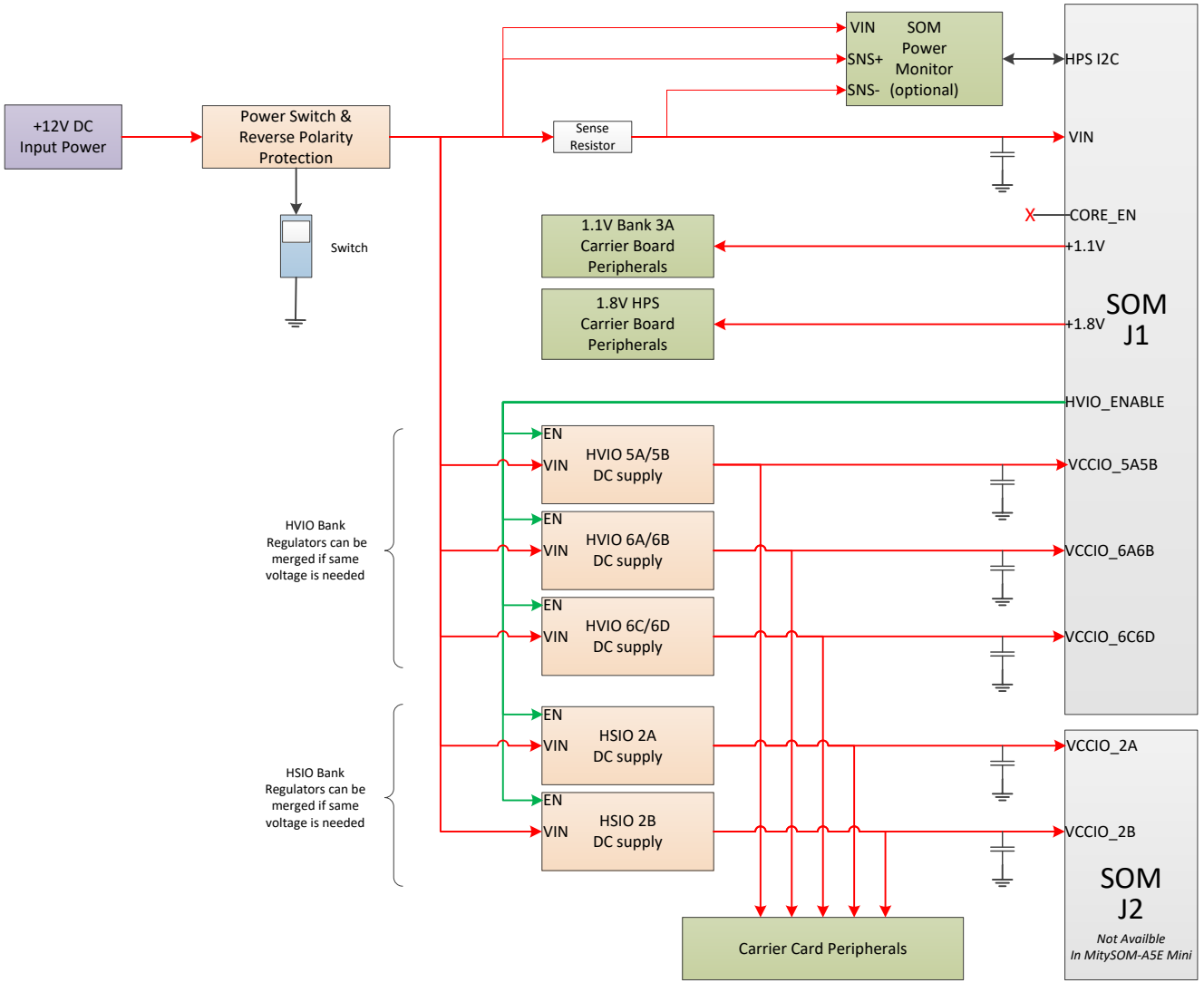

Figure 6 Typical MitySOM-A5E Standard and Mini Carrier Card Power Block Diagram

3.2 Clocking

The MitySOM-A5E SOMs provides 2 on-board clock sources: A 133.3333 MHz LVDS clock routed to clock input pins on HSIO Bank 3A and HSIO Bank 3B to support clocking the LPDDR4 memory banks at 800, 1066, or 1333 MHz. A second 25 MHz 1.8V CMOS clock is provided to drive the Agilex 5 Secure Data Management processing. This clock is also made available on the board-to-board interface connector and ***must be routed back into one of the HPS IO pins to properly clock the HPS subsystem.***

The MitySOM-A5E SOMs expose several transceiver clock pins directly to the board-to-board interface to support various transceiver protocols. Additionally, the HVIO Bank pins for banks 5 and 6 are all routed to the board-to-board interface. Many of these pins can act as FPGA fabric clock input pins for system PLL clocking.

Figure 7 illustrates the MitySOM-A5E Standard and Mini clock interfaces.

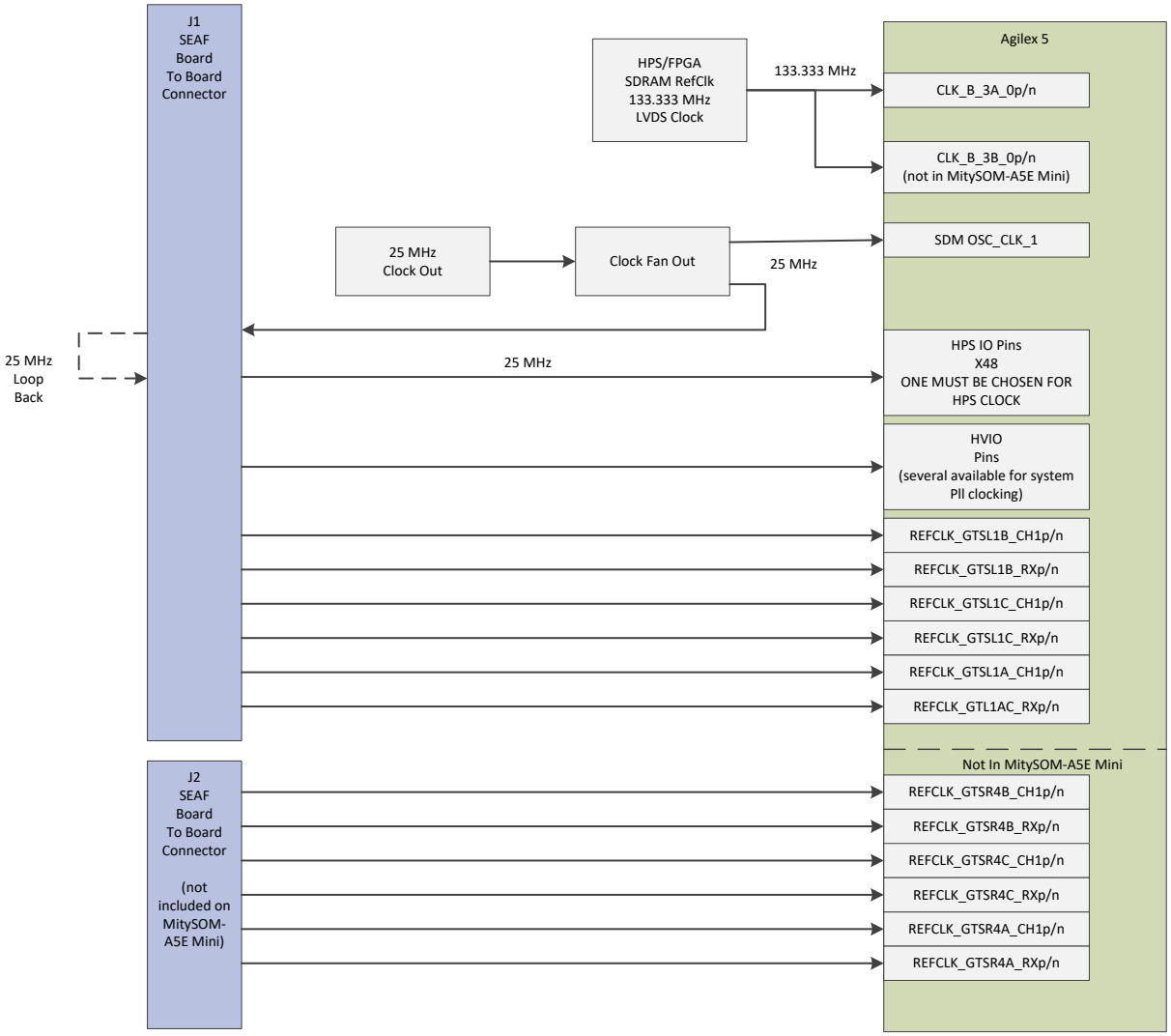

Figure 7 MitySOM-A5E Standard and Mini Clock Topology

3.3 Module Configuration and HPS Reset

After detecting a successful power on sequence, the MitySOM-A5E SOMs are designed to load the Agilex 5 Secure Device Manager (SDM) firmware from a programmed bitstream on an onboard QSPI serial NOR FLASH device. Specifically, the FPGA MSEL is configured as a "011", selected Active Serial, Normal Mode configuration. The following signals, mapped to the MitySOM-A5E Standard and Mini J1 Connector, are involved in SDM startup, FPGA configuration, and HPS reset:

Signal	J1 Pin	Direction	Description
nCONFIG	H34	Input	Active low signal to force (re)configuration. If this is held low during startup, the SDM will wait for this signal to go high to start the HPS/FPGA configuration sequence. When this signal is asserted low after a successful configuration, causes the SDM to clear FPGA and HPS and restart configuration sequence. This is pulled high on the SOM to 1.8V via 10K resistor.
nSTATUS	B50	Output	Open drain status that tracks nCONFIG. Pulled high on the SOM to 1.8V via 10K resistor. A rising edge on this signal indicates the SDM has initiated configuration.
CONF_DONE	G50	Output	Active high driver (routed to SDM_IO16) that indicates the SDM has received a valid bitstream from the QSPI NOR FLASH device. When CONF_DONE is high, LED D2 on the SOM will be illuminated.
INIT_DONE	B50	Output	Indicates when the FPGA has entered the user mode and the FPGA fabric has been fully programmed. In FPGA first mode, this will be set after the initialization of the FPGA fabric. In HPS first mode, this will be set after the HPS software initiates a complete FPGA configuration. When INIT_DONE is high, LED D1 on the SOM will be illuminated.
HPS_COLD_nRESET	C29	Input	Active low 1.8V CMOS signal to SDM_IO10, which should be configured as an HPS_COLD_nRESET function. This will issue a reset to the HPS subsystem. This signal must be held high on the Carrier Card for the HPS to operate normally.

The nSTATUS, CONF_DONE, and INIT_DONE signals may be monitored by a local processor / state machine on the carrier board to determine configuration success or simply ignored / left as a no connection.

The Agilex 5 SDM supports two main configuration orders, defined in the Quartus Project used to develop the FLASH bitstream / SDM firmware image.

FPGA First: The SDM fully configures the FPGA, then configures the HPS SDRAM pins, loads the HPS first stage boot loader and takes the HPS out of reset. FPGA first order requires the full bitstream for the FPGA to be included in the QSPI NOR FLASH. Generally, this will take a longer time to get to a working HPS boot prompt, etc., in this mode. Figure 8 illustrates a high-level configuration flow of the FPGA first mode.

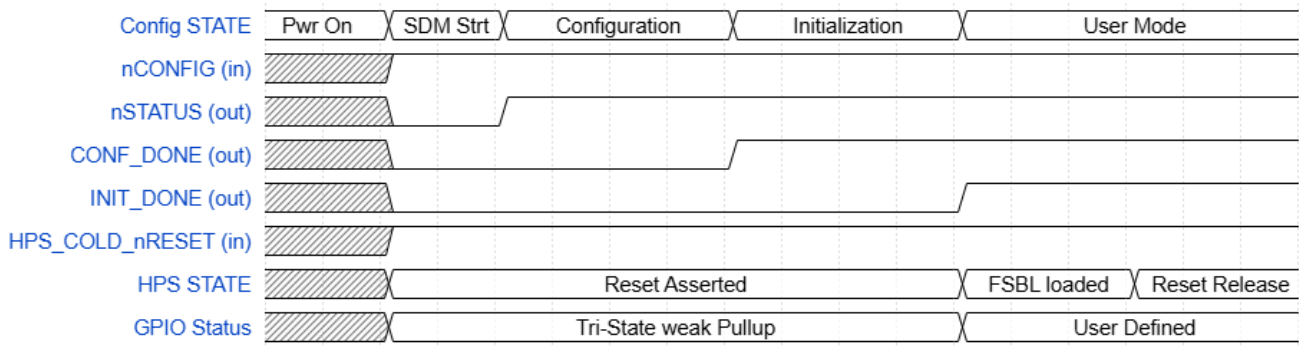

Figure 8 Configuration State Flow, FPGA first order

HPS First: The SDM first configures the HPS SDRAM pins, loads the HPS first stage boot loaders and takes the HPS out of reset. HPS first order requires only enough of the bitstream to be included on the QSPI NOR FLASH to define the HPS SDRAM configuration. After the HPS is loaded, follow on bitstream(s) can be loaded from any media the HPS boot software has access to via HPS IO pins, e.g. an MMC / MicroSD card, ethernet, NAND memory, UART, etc. Figure 9 illustrates a high-level configuration flow of HPS first mode.

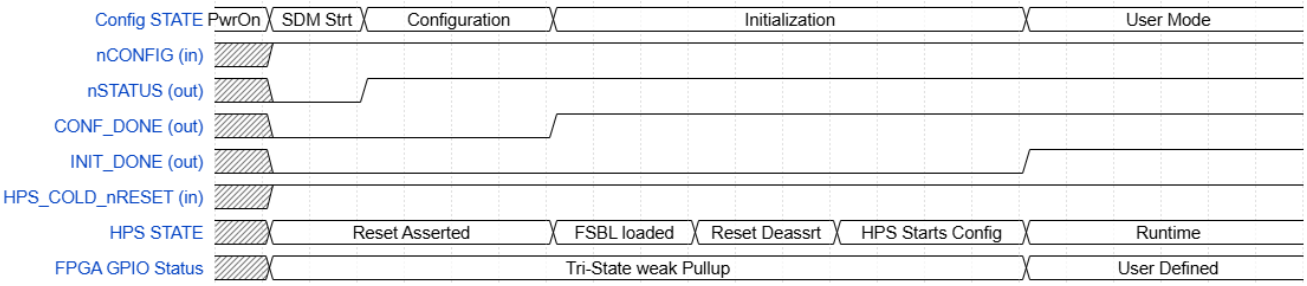

Figure 9 Configuration State Flow, HPS First Order

Typically, a carrier card design will include a momentary push-button to ground closure on the nCONFIG pin if forced reconfiguration is desired after power on. nCONFIG will reset the SDM state machine to the initial SDM Start state as shown in the above figures.

A carrier card design must pull the HPS_COLD_nRESET pin high to 1.8V or disable it in the quartus project. Typically, a carrier card design will include a momentary push-button to ground closure on the HPS_COLD_nRESET to force the HPS to reset while leaving the FPGA fabric programmed. Issuing an HPS_COLD_nRESET will cause the SDM to reload the first stage boot loader into the HPS memory and reset the HPS while leaving the FPGA fabric in its current state.

For more information about the SDM, HPS booting and FPGA configuration, please refer to the Agilex 5 Device Configuration User Guide from Altera.

3.4 Recommended Capacitance

The MitySOM-A5E modules include some power supply rail bypass capacitors on-board, however additional capacitance is recommended on the carrier board to minimize the ripple effect caused by changing load currents. It is recommended to place at least 20 µF in bulk capacitors nearby the main VCC_IN pins in addition to whatever bulk capacitance is recommended for your main rail supply design. For each of the HVIO and HSIO bank inputs, at least 10 µF in bulk capacitors is recommended. Please note that this is the minimum recommended amount of additional capacitance, and more is typically better.

3.5 I/O Interfaces

The I/O pins directly connected to the Agilex-5 FPGA can be grouped into the following functional domains. Designers are strongly encouraged to build a reference FPGA project and perform pin-planning to ensure final IO selection meets the Agilex 5 pin connection requirements.

- HPS IO Clock Pin – The HPS on the Agilex 5 uses a 25 MHz clock from one of the HPS 1.8V IO pins to drive its main PLL for generating the processor CPU clock and hard peripheral IO clock domains. The exact pin that is used can be programmed in the Quartus project settings. Carrier card designers must select / reserve an HPS IO pin for the HPS reference clock and loop the 25 MHz reference clock supplied by the SOM to this pin.

- HPS I2C1 Pins (J1 Pins A32 and A33) – The SOM HPS GPIO1_IO12 and GPIO1_IO13 pins are reserved for the I2C1 pin function. They are used on the SOM to access an on-board EEPROM as well as local power supplies and are pulled up with a 4.7K Ohm resistor to the HPS 1.8V rail. The I2C1 bus may be used on the carrier card, but designers should check that the desired addresses of the devices connected do not conflict with the addresses of devices on the SOM. See the SOM datasheet for the list of reserved I2C addresses.

- Remaining HPS IO interfaces – All of the remaining HPS IO interface pins operate at 1.8V CMOS level using the supplied +1.8V output power rail. The carrier card should use this rail for energizing circuitry interfacing with the HPS IO. The HPS IO pin functions are multiplexed. All pins can be used as a GPIO pin, the remaining functions (USB 2.0 ULPI, UART, I2C, I3C, SPI, NAND, EMAC, MMC, TRACE) are mapped to one or more pins and are configured using the Quartus Project / HPS Platform settings. Additional notes for some of the HPS IO interfaces are included in the following sections of this document.

- HSIO as MIPI D-PHY / CPI pins - These interfaces utilize low voltage differential signaling in accordance with the MIPI D-PHY / CSI standard. Data and clock lines should be routed using 100-ohm differential impedance and be matched in length. Note: MIPI/D-PHY clock and data lanes support data polarity inversion. Data lanes are in fixed order (data lanes may not be shuffled). A 240 ohm resistor must be connected to an RZQ pin within the HSIO bank for proper operation. Refer to the Agilex 5 HSIO MIPI user guide for more information. MIPI interface protocols require 1.1V or 1.2V HSIO Bank operation.

- HSIO as True Differential Signaling (TDS) Receivers – Users should carefully review the HSIO section of the Agilex 5 General Purpose I/O Overview and select an appropriate HSIO Bank voltage as the common mode and maximum input voltage levels for TDS are generally lower than nominal LVDS specifications. For integrating with standard LVDS signals with 1.25V common mode, the HSIO Bank voltage must be 1.3V and a 240 Ohm resistor should be connected to an RZQ pin for internal termination. Otherwise, external circuitry may be needed to lower the common mode voltage. Data and clock lines should be routed using 100-ohm differential impedance. Critical Link recommends matching the length of common function data and clock lanes, however the LVDS SERDES receiver block in the Agilex 5 does support Dynamic Phase Alignment (DPA) to correct for board skew. The lanes within an HSIO bank on the SOM are length matched between the Agilex 5 and the connector interface. Refer to the Agilex 5 LVDS SERDES User Guide, the Agilex 5 Datasheet (for common mode specifications), and the Agilex 5 General Purpose I/O Overview (HSIO section, for termination guidance) for more information.

- HSIO as True Differential Signaling Transmitters (supporting LVDS) – HSIO pins configured for TDS transmitters must use an HSIO Bank Voltage of 1.3V. Designers should be aware that the output common mode level for Agilex 5 TDS is typically 1.0V, which is slightly lower than the LVDS specification. Generally, most interface devices can support lower common modes. Designers should check the specifications for the devices they are integrating with and adjust common mode on the carrier board if it is required. Data and clock lines should be routed using 100-ohm differential impedance. The lanes within an HSIO bank on the SOM are length matched between the Agilex 5 and the connector interface. Refer to the Agilex 5 LVDS SERDES User Guide, the Agilex 5 Datasheet (for common mode specifications), and the Agilex 5 General Purpose I/O Overview (HSIO section, for termination guidance) for more information.

- HSIO as single ended interface – HSIO pins may be used as single ended IO ports using low voltage CMOS levels consistent with the provided Bank voltage. All pins within an HSIO bank are routed to the board-to-board connector with matched lengths.

- HVIO as single ended interface – HVIO pins may be used as single ended IO ports using low voltage CMOS levels consistent with the provided Bank Voltage. All pins within an HVIO bank are routed to the board-to-board connector with matched lengths.

- Multi-Gigabit Transceivers – The multi-gigabit transceiver lanes are routed differentially at 100 Ohms impedance and are directly connected to the board-to-board connector. No AC coupling capacitors are included on either the transmit or receive pairs on the SOM and should be included, where necessary,

on the carrier card. Users should refer to the Agilex 5 Datasheet for specific details on the transceiver electrical standards.

- Multi-Gigabit Transceiver Reference Clock inputs - The multi-gigabit transceiver reference clock lanes are routed differentially at 100 Ohms impedance and are directly connected to the board-to-board connector. No AC coupling capacitors are included on the SOM and should be included, where necessary, on the carrier card. Users should refer to the Agilex 5 Datasheet for specific details on the transceiver reference clock electrical standards.

3.5.1 I/O Protection

Any I/O interfaces that are external to the MitySOM-A5E module must be protected to ensure that no out-of-range voltage conditions occur as all I/O pins are directly connected to the Agilex 5 FPGA. The host board should contain the necessary protection/isolation circuits as required to protect the processor. Please refer to the Agilex 5 Datasheet for details about maximum voltage ranges for both HSIO and HVIO domains as the maximum ranges are different.

3.6 Debugger Interface (JTAG, TRACE)

The MitySOM-A5E Family JTAG interface is available on the J1 board-to-board connector, and it is strongly recommended that this interface be wired up to a header so a debugger can be attached to the design. This JTAG interface is daisy chained via the secure data manager (SDM) on the Agilex 5. The Critical Link devkit uses a TE Connectivity AMP 5103308-1 vertical 10-pin 2.54mm header to support standard USB Blaster II pods as shown in Figure 10. Note: The MitySOM-A5E modules include 10K ohm pullup resistors to +1.8V on TDI, and TMS and a 1K ohm pulldown resistor on TCK such that these pins may be left unconnected on the carrier card if no JTAG interface is desired.

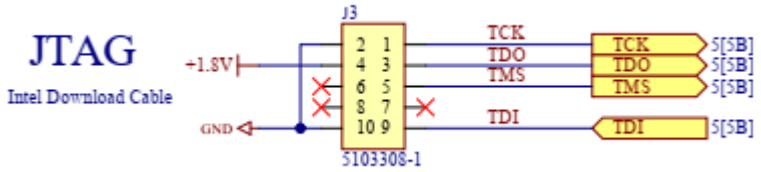

Figure 10: Typical Carrier Card JTAG Interface

It is also possible to route a JTAG interface to HPS multiplexed I/O or FPGA I/O pins that is not daisy chained with the SDM. However, these pins would then not be available for normal use.

For trace, the Agilex 5 includes Coresight SoC-400 capability. Up to 16 bits of trace width can be gathered using the (pin-multiplexed) HPS IO pins. Up to 32 bits of trace width can be gathered using FPGA I/O. For more information, refer to the Debug and Trace section of the Agilex 5 HPS Technical Reference Manual.

3.7 HPS IO RS232 Monitor Interface

It is strongly recommended that HPS IO UART0 on SOM J1 Connector Pins D48 and E40 be used as a general-purpose monitor port. All the u-Boot console and kernel console IO data is routed to UART0 (with no HW flow control) by default in the reference software development images. Using UART0 pins for other functions will require modification of low-level boot software (e.g., U-Boot) and the kernel configuration to disable kernel logging to this port. Modern board designs typically use a USB to UART bridge chip to support standard USB style serial ports (COM ports for windows, ttyUSBX ports for Linux). The Critical Link reference design utilizes a FT230XS UART to USB bridge chip to interface UART0 for the ARM console.

3.8 HPS IO RGMII / Ethernet Interface

RGMII traces to the HPS IO pins should be routed as 50 ohm. The transmitter groups should be matched in length. The receiver groups should be matched in length. It is recommended that series resistors be included on the PHY transmit lines (close to the source) and close to the SOM interface board for the HPS driver side to support impedance matching if required.

3.9 USB Interface(s)

3.9.1 HPS IO USB 2.0 ULPI Considerations

To support USB 2.0 connections (which are also required for USB 3.1 and USB-C interfaces), an external ULPI PHY is required. The MitySOM-A5E Standard and Mini development kits utilize a Microchip USB3320 series PHY for USB 2.0 support utilizing a 24 MHz external reference clock. The ULPI bus signals should be routed as 50 Ohm traces and the bus should be matched in length to board-to-board connector signals.

If you are connecting to a USB 2.0 port and would like to support dual role operation, you will need to handle detection of the USB_VBUS presence as well as controlling the +5V USB Bus enable switch. Some PHYs support manipulating this via ULPI PHY register access. In some cases, it may be easier to bring these signals back to the HPS via HPS GPIO or HVIO (mapped as PIO) pins. Users are encouraged to review the development kit schematics for PHY interface.

3.9.2 USB 3.1 Super Speed

The Agilex 5 HPS IO does provide USB 3.1 superspeed (SS) capability. The super speed connections require use of either CH2 or CH1 in the transceiver bank adjacent to the HPS. For the MitySOM-A5E Family the transceiver pins that are recommended for the USB 3.1 SS interface are on pins B34/B35/A44/A45 or pins B38/B39/B46/B47 of the J1 connector interface. Both the MitySOM-A5E Standard and Mini development kits include support for USB 3.1 super speed connections via the USB-C connector.

3.9.3 USB-C Connector

The USB-C connector interface introduces some complexities because the connector is reversable, and the power-delivery / data-facing direction negotiation is more complex.

For connector reversal detection, power negotiation and USB 3.1 super speed signal management, an external multiplexer chip and control chip is recommended. Users are encouraged to review the USB-C interface specifications for a better definition of the additional requirements beyond a simple USB 2.0 or USB 3.1 Type B connector. Both the MitySOM-A5E Standard and Mini development kit carrier cards utilize the TI HD3SS3220IRNHR to manage the super speed signal multiplexing, CC control line management, data-role, and power delivery negotiation related to the USB-C interface. Design files are available upon request.

4 Mechanical Requirements

The following sections describe some of the mechanical requirements of incorporating a MitySOM-A5E Standard or MitySOM-A5E Mini module into a board design.

4.1 Module Connectors and Mounting Holes

The MitySOM-A5E Standard makes use of two Samtec Female SEAF 400 pin board-to-board mating connectors. The carrier card connectors required to interface with the MitySOM-A5E Standard are the Samtec SEAM-50-02.0-L-08-2-A-K-TR. In addition to the Samtec connectors, provisions for 4 mounting holes on the MitySOM-A5E Standard allow fastening to the carrier card using M2.5 7mm tall standoffs. Depending on your operating environment, the screw-down mounting holes may not be necessary. The development kit carrier card design uses a Würth Elektronik 9774070151R surface mount round standoff to support the fasteners. Figure 11 provides a top-down view of the connector and standoff placement, which should be used to mate with the MitySOM-A5E Standard SOM.

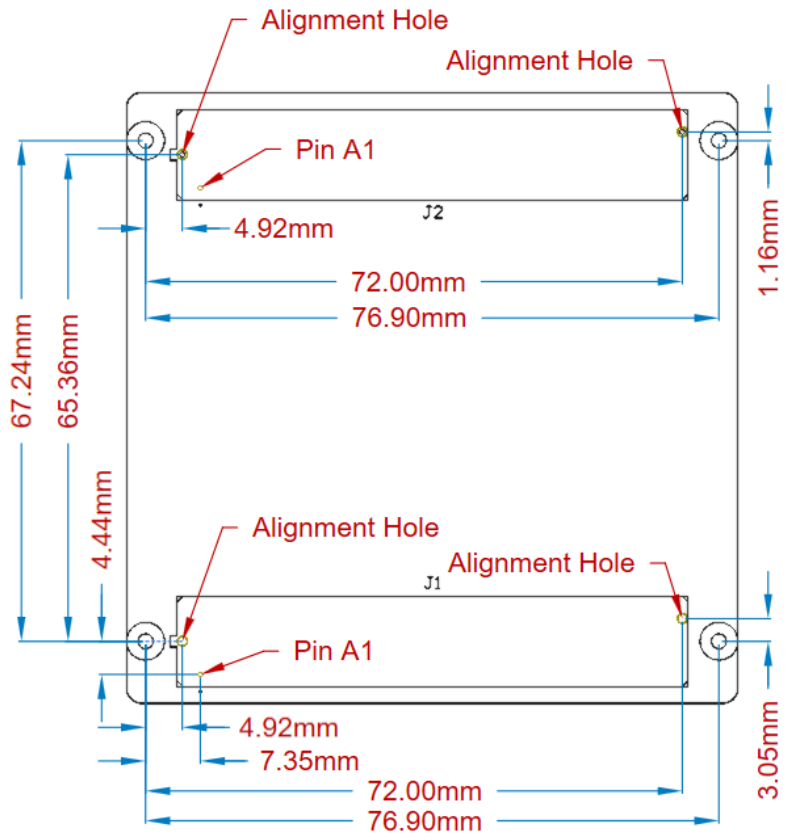

Figure 11 MitySOM-A5E Standard Carrier Card Connector and Standoff Placement

Note: customers may use alternative stacking height options, but in doing so will require different standoff mounts if the mounting holes are utilized.

A similar illustration for the MitySOM-A5E Mini is shown in Figure 12.

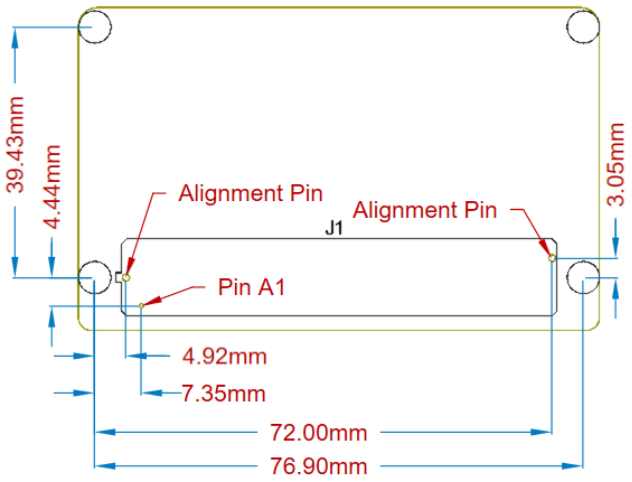

Figure 12 MitySOM-A5E Mini Carrier Card Connector and Standoff Placement

4.2 Module Clearance – Horizontal Mount

The MitySOM-A5E Standard and Mini modules use board-to-board insertion style main interface connectors for electrical and mechanical attachment to the carrier board. This style of connector positions the MitySOM-A5E modules in parallel with the carrier board, and as such there is limited clearance between the module and the carrier board. Therefore, it is not possible to place high-profile carrier board components underneath the MitySOM-A5E modules. However, it is possible to utilize most of this space for lower-profile components. Please refer to the following diagrams and tables for module-specific clearances. Note that this configuration is based on using a Samtec SEAM-50-02.0-L-08-2-A-K-TR connector (7 mm stacking height). Additional clearance may be gained using taller stacking SEAM connector options. As shown a keep-out height of 4mm from the top of the module is recommended. On the bottom of the module, the region between the two Samtec connectors has a keep-out of 2.5mm. With a 7mm stacking height, this leaves 4.5mm for component clearance on the carrier card. The STEP models for both the MitySOM-A5E Standard and Mini are available from the Critical Link support site, and users are encouraged to verify clearance if making use of the space under the module.

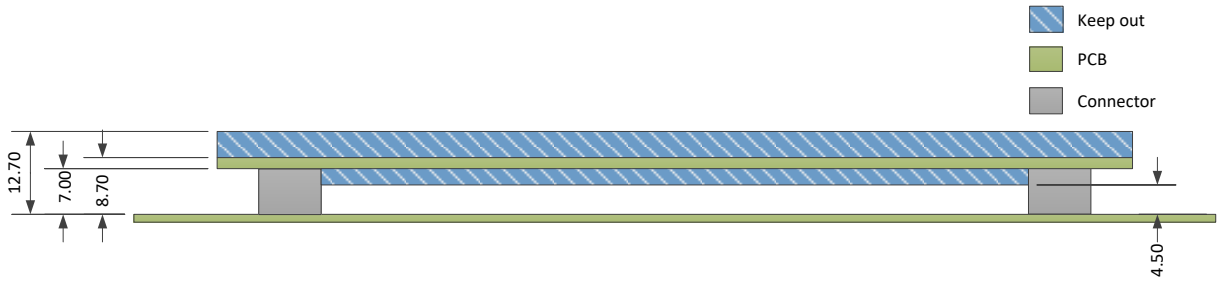

Figure 13: MitySOM-A5E Standard Module Clearance - Side View, all dimensions in mm

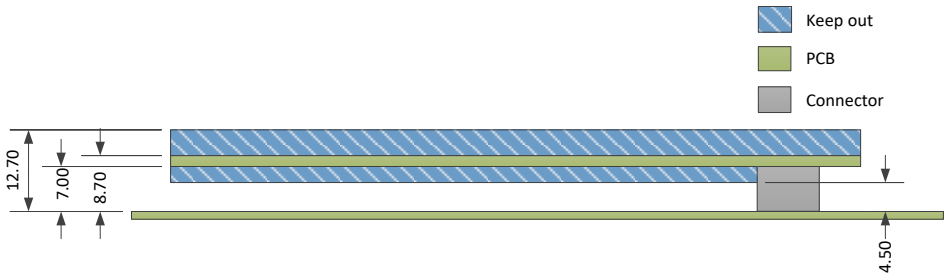

Figure 14 MitySOM-A5E Mini Module Clearance - Side View, all dimensions in mm

4.3 Thermal Management

The power consumption for both the MitySOM-A5E Standard and the MitySOM-A5E Mini devices are heavily dependent on the end-user application. Factors driving power consumption include FPGA device density (static power consumption), use of high-speed transceiver interfaces, total FPGA utilization, FPGA clock rates, and operating speed of the HPS complex (dynamic power). Applications requiring wide operational temperature will likely require some form of thermal management. Customers are strongly encouraged to review the power consumption reports made available via Altera's Power and Thermal Calculator tools during the development of the FPGA bitstream and model the thermal dissipation required for the SOM. On the Critical Link support site for the MitySOM-A5E Family, users can find typical consumption numbers for both SOMs under different usage situations. This information is provided for reference only.

The MitySOM-A5E Standard utilizes a 32x32 mm package device for the Agilex 5 FPGA. The layout of the SOM is such that it will support installation of an Advanced Technical Solutions (ATS) 32x32 maxiGRIP BGA heat sink device, such as the ATS-61325W-C2-R0. If more aggressive cooling is needed, it may be necessary to develop a heat spreading solution for the module.

The MitySOM-A5E Mini utilizes a 23x23 mm package device for the Agilex 5 FPGA. The layout of the SOM is such that it will support installation of an Advanced Technical Solutions (ATS) 23x23mm superGRIP BGA heat sink device, such as the ATS-X51230D-C1-R0. If more aggressive cooling is needed, it may be necessary to develop a heat spreading solution for the module.

5 Board Layout Recommendations

The following sections discuss topics for successful board layouts incorporating MitySOM-A5E modules.

5.1 Placement

Placement of the module site is crucial to a successful carrier board layout. Because the module connector footprint is fine-pitch and multi-row, it is generally best to place the connector fairly centered in the overall board layout. This placement allows traces to be routed out from both sides of the connector. The use of fewer signal layers, and therefore fewer vias, generally results in a more compact design with better signal integrity than a board using many layers and vias. Of course, ideally central placement is not always possible because of other mechanical constraints.

5.2 Pin-out and Routing

Care must be taken when routing the high speed interfaces – specifically the multi-gigabit transceiver lanes, the HSIO pins for DPHY/LVDS/SSTL (high speed) signaling, and the Gigabit Ethernet RGMII interface bus. Please refer to the specific device specification for guidance related to these pins.

5.3 Access Issues

Given that it is possible and often desirable to make best use of available space by placing components underneath the MitySOM-A5E modules (refer to section 4.2), hardware and software engineers who will be debugging code on the platform could find themselves in a tough situation if the component they need to access is blocked by the installed SOM. Because of these situations it is advisable to either not use the space under the SOM for active components that might need live probing with the MitySOM-A5E in-circuit, or only place circuits there that are already tried and tested by engineers on other platforms. If an obscured circuit does need to be probed, it may be necessary to solder temporary wires onto probe points. An even better solution would be to design the board with bottom-side test points, at least in the MitySOM-A5E region, if this is possible with a given design.

5.4 PCB/PCA Technology

The MitySOM-A5E modules do not have any specific requirements regarding the PCB technology used for its carrier board. The required socket connectors are available as RoHS compliant and may be used in both leaded and lead-free assembly processes. The board technology required will be primarily driven using the multi-gigabit high speed transceivers, as the performance of these traces may require materials having a lower loss factor and/or tighter impedance control at higher frequencies than standard FR-4 materials.

Developers should fabricate the carrier board thick enough to rigidly support the MitySOM-A5E socket connector. In practice, FR-4 with a common finished thickness of 0.062 inches is enough for all types of MitySOM-A5E modules.

5.5 PCB Footprints

Detailed information for the SEAM-50-02.0-I-08-2-A-K-TR is available on the Samtec Product Page. The CAD Files and Information Page on the Critical Link support site includes Altium integrated libraries and STEP models for both the MitySOM-A5E Standard and the MitySOM-A5E Mini. The integrated libraries include a schematic symbol as well as reference footprints including the PCB land pattern for the Samtec connector as well as reference locations for the mounting holes and SOM outlines. If support for an alternate CAD package is needed, please contact Critical Link.

6 Revision History

Revision	Date	Description of Changes
1.0	5-November-2025	Initial Revision