FEATURES

MitySOM-A10S Development Board

MitySOM-A10S Module

Additional Hardware Included:

- UART to USB Cable
- Ethernet Cable
- AC to DC 12V Adapter

Integrated +3.3V/+5V Power Supplies

Digital Interfaces:

- 10/100/1000 MBit Ethernet Interface
- Debug UART to USB
- USB OTG Interface

Expansion

- 400 Pin FPGA Mezzanine Card High Pin Count (FMC HPC)

Software and Documentation

- Reference Quartus Project
- Reference SD card to boot to Linux
- Development Environment - Virtual Machine
- Development Board Schematics
- Development Board Gerber Files
- Development Board BOM

APPLICATIONS

- MitySOM-A10S Evaluation
- Test and Measurement
- Factory Automation
- Industrial Automation
- Embedded Instrumentation
- Test and Measurement
- Rapid Prototyping

DESCRIPTION

The MitySOM-A10S Development Kit provides all the hardware and software support for system designers and developers to evaluate the Critical Link MitySOM-A10S System on Module. The MitySOM-A10S Development Kit comes complete with a MitySOM-A10S module that meets your project's needs.

The MitySOM-A10S Development Kit includes on-board Debug UART to USB converter, 10/100/1000 Gb Ethernet, Universal Serial Bus (USB 2.0) On-The-Go (OTG) communication interfaces. FMC HPC connector that is compatible with a wide range of existing add-on cards. All powered from a single 12VDC input (adapter included) with onboard +3.3V/+5V power supplies.

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A block diagram of the MitySOM-A10S Development Kit is illustrated in Figure 1. Control of the on-board interface hardware and connected Expansion IO cards require proper configuration of the MitySOM-A10S Module. While not required, it is strongly recommended that the MitySOM software development kit and supplied API be used to manage these interfaces.

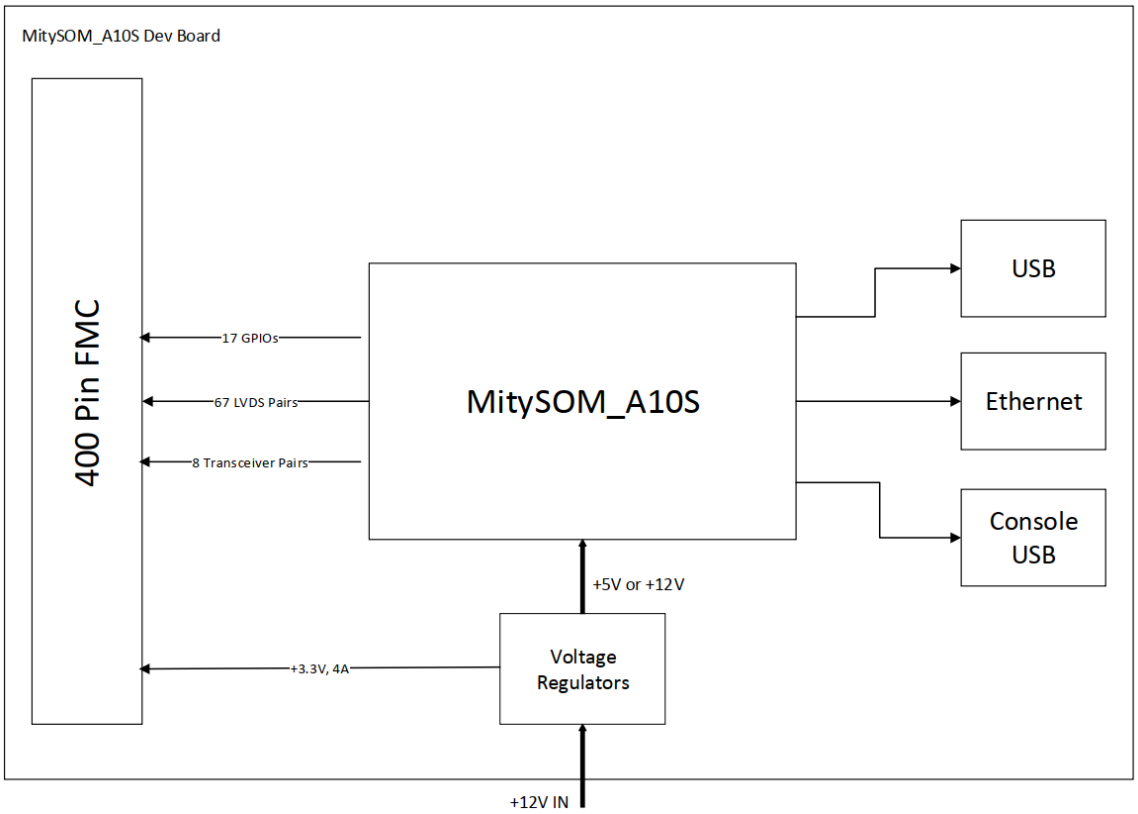

Figure 1: MitySOM-A10S Development Kit Block Diagram

Additional details about the Arria 10 SX SoC, available peripherals, their features and FPGA IO details are provided in the data sheet at the Intel website (https://www.intel.com/content/www/us/en/products/programmable/soc/arria-10.html).

Feature Descriptions

Electrical Interface Descriptions

Debug UART to USB Interface Description

The on-board UART to USB Bridge, FTDI FT230X, provides a serial interface at data rates up to 115,200 baud. The USB serial interface, J600 - Console, is routed to the primary MitySOM serial console port, UART0. It allows for general module debug and console interaction.

When connected to a Windows PC no drivers are required as Windows Update is used to obtain the drivers.

USB 2.0 Interface Description

The on-board USB OTG interface utilizes a micro B type connector J601 and interfaces with the USB phy on the MitySOM-A10S module. This phy is connected to the USB1 controller within the Arria 10 SoC HPS. Linux drivers are available. This interface allows for a connection to either a PC or a USB device through the use of a USB-OTG to USB A type adapter, not included.

Gigabit Ethernet Interface Description

The on-board Ethernet interface features a Micrel KSZ9031 Ethernet PHY capable of running at 10/100/1000Mbit including link auto-negotiation and RGMII/MDIO capability. An industry standard RJ-45 connector is provided for external connection.

FMC HPC Interface Description

The FPGA Mezzanine Card High Pin Count (FMC HPC) interface allows for the use of add-on cards that are designed for the Intel Arria 10 on the MitySOM-A10S module. A number of “off the shelf” boards/kits are available from third parties that are compatible with this interface.

Reset Switch Description

The A10S Development Kit has a cold reset button than can be used to reset the ARM processor of the Intel Arria 10. This reset button is located at S404.

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Parameter	Min	Max	Units
Supply Voltage	12	20	V
Operating Temperature for MitySOM-A10S/Baseboard	0	70	C
Operating Temperature for AC to DC Power Supply	0	50	C
Storage Temperature	-40	85	C
Humidity	0	95	% Non-condensing

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Typical	Limit	Units (Limits)
Maximum Power Supply Output					
I_{Max}	12V Supply (AC Adapter) all components			5.0	A
I_{Max}	12.0V Supply[1] for external components			1.0	A
I_{Max}	3.3V Supply[1] for external components			2.0	A
I_{Max}	1.8V Supply[1] for external components			4.0	A
Power Dissipation					
V_S	Supply Voltage		12±5%		V
I_S	Supply Current[2]		800		mA

Notes:

1. The maximum current supplied to external components should be limited to the specified maximum for all externally connected power supplies
2. FMC cards not attached, FPGA programmed, 100% ARM utilization, RS-232 and Ethernet are enabled and active.

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ELECTRICAL INTERFACE DESCRIPTIONS

Input Power – P700

The MitySOM-A10S Development Kit power interface, P700, requires a single +12Volt power supply. A recommended input supply rating of at least 3A is recommended and a 5A supply is included with each Development Kit.

Table 1: Input Power Interface Pin Description

Signal	J601 Position
+12V	1
GND	2

Main Power Switch – S700

An input power switch is present on the Development Kit, S700, which controls the power input, on or off, from P700.

Power Selection Switch – SW701

This switch is used to determine if +5V or +12V is going to be supplied to the MitySOM-A10S for the main power.

Debug/Boot UART - USB Interface – J600

Table 2: J600 Micro USB Connector Pin Assignments

Pin	Signal	Type	Standard	Notes
1	VBUS	Power	-	
2	D-	I/O	USB 2.0	USB data minus line
3	D+	I/O	USB 2.0	USB data plus line
4	GND	GND	-	
5	SHIELD	GND	-	

USB 2.0 Interface (OTG) – J601

Table 3: J601 Pin Assignments

Pin	Signal	Type	Standard	Notes
1	USB1_VBUS	POWER	-	
2	USB1_D_N	I/O	USB 2.0	USB data minus line
3	USB1_D_P	I/O	USB 2.0	USB data plus line
4	USB1_ID	I/O	-	
5	GND	POWER	-	

FMC Interface- J300

Table describes the pin-out of the FMC interface on the MitySOM-A10S development board. The I/O "type" is in reference to the signal direction from the SOM/development board.

Table 4.1: J300 Connector Pin A1-A40 Assignments

Pin	FMC Signal	Baseboard/SOM Signal	FPGA Ball	Type
A1	GND	GND	-	POWER
A2	DP1_M2C_P	GXBR_RX_0_P	T26	I
A3	DP1_M2C_N	GXBR_RX_0_N	T25	I
A4	GND	GND	-	POWER
A5	GND	GND	-	POWER
A6	DP2_M2C_P	GXBR_RX_2_P	P26	I
A7	DP2_M2C_N	GXBR_RX_2_N	P25	I
A8	GND	GND	-	POWER
A9	GND	GND	-	POWER
A10	DP3_M2C_P	GXBR_RX_3_P	M26	I
A11	DP3_M2C_N	GXBR_RX_3_N	M25	I
A12	GND	GND	-	POWER
A13	GND	GND	-	POWER
A14	DP4_M2C_P	GXBR_RX_5_P	H26	I
A15	DP4_M2C_N	GXBR_RX_5_N	H25	I
A16	GND	GND	-	POWER
A17	GND	GND	-	POWER
A18	DP5_M2C_P	GXBR_RX_7_P	D26	I
A19	DP5_M2C_N	GXBR_RX_7_N	D25	I
A20	GND	GND	-	POWER
A21	GND	GND	-	POWER
A22	DP1_C2M_P	GXBR_TX_0_P	W28	O
A23	DP1_C2M_N	GXBR_TX_0_N	W27	O
A24	GND	GND	-	POWER
A25	GND	GND	-	POWER
A26	DP2_C2M_P	GXBR_TX_2_P	R28	O
A27	DP2_C2M_N	GXBR_TX_2_N	R27	O
A28	GND	GND	-	POWER
A29	GND	GND	-	POWER
A30	DP3_C2M_P	GXBR_TX_3_P	N28	O
A31	DP3_C2M_N	GXBR_TX_3_N	N27	O
A32	GND	GND	-	POWER
A33	GND	GND	-	POWER
A34	DP4_C2M_P	GXBR_TX_5_P	J28	O
A35	DP4_C2M_N	GXBR_TX_5_N	J27	O
A36	GND	GND	-	POWER
A37	GND	GND	-	POWER
A38	DP5_C2M_P	GXBR_TX_7_P	E28	O
A39	DP5_C2M_N	GXBR_TX_7_N	E27	O
A40	GND	GND	-	POWER

Table 4.2: J300 Connector Pin B1-B40 Assignments

Pin	FMC Signal	Baseboard/SOM Signal	FPGA Ball	Type
B1	CLK_DIR	GND	-	-
B2	GND	GND	-	POWER
B3	GND	GND	-	POWER
B4	DP9_M2C_P	GND	-	-
B5	DP9_M2C_N	+1.8V_VADJ	-	-
B6	GND	GND	-	POWER
B7	GND	GND	-	POWER
B8	DP8_M2C_P	GND	-	-
B9	DP8_M2C_N	+1.8V_VADJ	-	-
B10	GND	GND	-	POWER
B11	GND	GND	-	POWER
B12	DP7_M2C_P	GXBR_RX_4_P	K26	I
B13	DP7_M2C_N	GXBR_RX_4_N	K25	I
B14	GND	GND	-	POWER
B15	GND	GND	-	POWER
B16	DP6_M2C_P	GXBR_RX_6_P	F26	I
B17	DP6_M2C_N	GXBR_RX_6_N	F25	I
B18	GND	GND	-	POWER
B19	GND	GND	-	POWER
B20	GBTCLK1_M2C_P	PLL_REFCLK_OUT_P	-	O
B21	GBTCLK1_M2C_N	PLL_REFCLK_OUT_N	-	O
B22	GND	GND	-	POWER
B23	GND	GND	-	POWER
B24	DP9_C2M_P	GND	-	-
B25	DP9_C2M_N	+1.8V_VADJ	-	-
B26	GND	GND	-	POWER
B27	GND	GND	-	POWER
B28	DP8_C2M_P	GND	-	-
B29	DP8_C2M_N	+1.8V_VADJ	-	-
B30	GND	GND	-	POWER
B31	GND	GND		POWER
B32	DP7_C2M_P	GXBR_TX_4_P	L28	O
B33	DP7_C2M_N	GXBR_TX_4_N	L27	O
B34	GND	GND	-	POWER
B35	GND	GND	-	POWER
B36	DP6_C2M_P	GXBR_TX_6_P	G28	O
B37	DP6_C2M_N	GXBR_TX_6_N	G27	O
B38	GND	GND	-	POWER
B39	GND	GND	-	POWER
B40	RES0	GND	-	-

Table 4.3: J300 Connector Pin C1-C40 Assignments

Pin	FMC Signal	Baseboard/SOM Signal	FPGA Ball	Type
C1	GND	GND	-	POWER
C2	DP0_C2M_P	GXBR_TX_1_P	U28	O
C3	DP0_C2M_N	GXBR_TX_1_N	U27	O
C4	GND	GND	-	POWER
C5	GND	GND	-	POWER
C6	DP0_M2C_P	GXBR_RX_1_P	P26	I
C7	DP0_M2C_N	GXBR_RX_1_N	P25	I
C8	GND	GND	-	POWER
C9	GND	GND	-	POWER
C10	LA06_P	B2A_LVDS_B5_P	AF12	IO
C11	LA06_N	B2A_LVDS_B5_N	AF11	IO
C12	GND	GND	-	POWER
C13	GND	GND	-	POWER
C14	LA10_P	B2A_LVDS_B22_P	AC13	IO
C15	LA10_N	B2A_LVDS_B22_N	AB13	IO
C16	GND	GND	-	POWER
C17	GND	GND	-	POWER
C18	LA14_P	B2A_LVDS_B2_P	AE15	IO
C19	LA14_N	B2A_LVDS_B2_N	AE14	IO
C20	GND	GND	-	POWER
C21	GND	GND	-	POWER
C22	LA18_P_CC	B2A_LVDS_B21_P	AC15	IO
C23	LA18_N_CC	B2A_LVDS_B21_N	AB15	IO
C24	GND	GND	-	POWER
C25	GND	GND	-	POWER
C26	LA27_P	B3B_LVDS_B19_P	U3	IO
C27	LA27_N	B3B_LVDS_B19_N	U4	IO
C28	GND	GND	-	POWER
C29	GND	GND	-	POWER
C30	SCL	I2C1_SCL	C16	O
C31	SDA	I2C1_SDA	C17	IO
C32	GND	GND	-	POWER
C33	GND	GND	-	POWER
C34	GA0	GND	-	-
C35	12P0V	+12V	-	POWER
C36	GND	GND	-	POWER
C37	12P0V	+12V	-	POWER
C38	GND	GND	-	POWER
C39	3P3V	+12V	-	POWER
C40	GND	GND	-	POWER

Table 4.4: J300 Connector Pin D1-D40 Assignments

Pin	FMC Signal	Baseboard/SOM Signal	FPGA Ball	Type
D1	PG_C2M	GPIO0_IO10	D19	IO
D2	GND	GND	-	POWER
D3	GND	GND	-	POWER
D4	GBTCLK0_M2C_P	GXBR_REFCLK_IN_P	N24	I
D5	GBTCLK0_M2C_N	GXBR_REFCLK_IN_N	N23	I
D6	GND	GND	-	POWER
D7	GND	GND	-	POWER
D8	LA01_P_CC	CLK3B_P	L2	IO
D9	LA01_N_CC	CLK3B_N	L3	IO
D10	GND	GND	-	POWER
D11	LA05_P	B2A_LVDS_B23_P	AA12	IO
D12	LA05_N	B2A_LVDS_B23_N	AA13	IO
D13	GND	GND	-	POWER
D14	LA09_P	B2A_LVDS_B6_P	AD13	IO
D15	LA09_N	B2A_LVDS_B6_N	AD14	IO
D16	GND	GND	-	POWER
D17	LA13_P	B2A_LVDS_B17_P	AE17	IO
D18	LA13_N	B2A_LVDS_B17_N	AD17	IO
D19	GND	GND	-	POWER
D20	LA17_P_CC	B2A_LVDS_B3_P	AE16	IO
D21	LA17_N_CC	B2A_LVDS_B3_N	AD15	IO
D22	GND	GND	-	POWER
D23	LA23_P	B3B_LVDS_B21_P	V7	IO
D24	LA23_N	B3B_LVDS_B21_N	U6	IO
D25	GND	GND	-	POWER
D26	LA26_P	B3B_LVDS_B20_P	V1	IO
D27	LA26_N	B3B_LVDS_B20_N	U1	IO
D28	GND	GND	-	POWER
D29	TCK	-	-	NC
D30	TDI	-	-	NC
D31	TDO	-	-	NC
D32	3P3VAUX	+3.3V	-	POWER
D33	TMS	-	-	NC
D34	TRST_L	-	-	NC
D35	GA1	GND	-	POWER
D36	3P3V	+3.3V	-	POWER
D37	GND	GND	-	POWER
D38	3P3V	+3.3V	-	POWER
D39	GND	GND	-	POWER
D40	3P3V	+3.3V	-	POWER

Table 4.5: J300 Connector Pin E1-E40 Assignments

Pin	FMC Signal	Baseboard/SOM Signal	FPGA Ball	Type
E1	GND	GND	-	POWER
E2	HA01_P_CC	B3A_LVDS_B9_P	AB6	IO
E3	HA01_N_CC	B3A_LVDS_B9_N	AB5	IO
E4	GND	GND	-	POWER
E5	GND	GND	-	POWER
E6	HA05_P	B3A_LVDS_B24_P	AE5	IO
E7	HA05_N	B3A_LVDS_B24_N	AD5	IO
E8	GND	GND	-	POWER
E9	HA09_P	B3A_LVDS_B20_P	AE4	IO
E10	HA09_N	B3A_LVDS_B20_N	AD4	IO
E11	GND	GND	-	POWER
E12	HA13_P	B3A_LVDS_B8_P	AB1	IO
E13	HA13_N	B3A_LVDS_B8_N	AA1	IO
E14	GND	GND	-	POWER
E15	HA16_P	B3A_LVDS_B19_P	AH2	IO
E16	HA16_N	B3A_LVDS_B19_N	AH3	IO
E17	GND	GND	-	POWER
E18	HA20_P	B3A_LVDS_B1_P	W4	IO
E19	HA20_N	B3A_LVDS_B1_N	Y4	IO
E20	GND	GND	-	POWER
E21	HB03_P	B3B_LVDS_B18_P	T1	IO
E22	HB03_N	B3B_LVDS_B18_N	R1	IO
E23	GND	GND	-	POWER
E24	HB05_P	B3B_LVDS_B8_P	K4	IO
E25	HB05_N	B3B_LVDS_B8_N	L4	IO
E26	GND	GND	-	POWER
E27	HB09_P	B3B_LVDS_B2_P	T8	IO
E28	HB09_N	B3B_LVDS_B2_N	T9	IO
E29	GND	GND	-	POWER
E30	HB13_P	GPIO1_IO15	H18	IO
E31	HB13_N	GPIO1_IO16	F17	IO
E32	GND	GND	-	POWER
E33	HB19_P	GND	-	-
E34	HB19_N	GND	-	-
E35	GND	GND	-	POWER
E36	HB21_P	GND	-	-
E37	HB21_N	GND	-	-
E38	GND	GND	-	POWER
E39	VADJ	+1.8V	-	POWER
E40	GND	GND	-	POWER

Table 4.6: J300 Connector Pin F1-F40 Assignments

Pin	FMC Signal	Baseboard/SOM Signal	FPGA Ball	Type
F1	PG_M2C	GPIO1_IO23	H16	IO
F2	GND	GND	-	POWER
F3	GND	GND	-	POWER
F4	HA00_P_CC	CLK3A_P	AA6	IO
F5	HA00_N_CC	CLK3A_N	AA7	IO
F6	GND	GND	-	POWER
F7	HA04_P	B3A_LVDS_B18_P	AG3	IO
F8	HA04_N	B3A_LVDS_B18_N	AF3	IO
F9	GND	GND	-	POWER
F10	HA08_P	B3A_LVDS_B7_P	AC5	IO
F11	HA08_N	B3A_LVDS_B7_N	AB4	IO
F12	GND	GND	-	POWER
F13	HA12_P	B3A_LVDS_B16_P	AE2	IO
F14	HA12_N	B3A_LVDS_B16_N	AD2	IO
F15	GND	GND	-	POWER
F16	HA15_P	B3A_LVDS_B21_P	AC6	IO
F17	HA15_N	B3A_LVDS_B21_N	AC7	IO
F18	GND	GND	-	POWER
F19	HA19_P	B3A_LVDS_B2_P	W8	IO
F20	HA19_N	B3A_LVDS_B2_N	W7	IO
F21	GND	GND	-	POWER
F22	HB02_P	B3B_LVDS_B23_P	W2	IO
F23	HB02_N	B3B_LVDS_B23_N	V2	IO
F24	GND	GND	-	POWER
F25	HB04_P	B3B_LVDS_B22_P	V5	IO
F26	HB04_N	B3B_LVDS_B22_N	V6	IO
F27	GND	GND	-	POWER
F28	HB08_P	B3B_LVDS_B15_P	R2	IO
F29	HB08_N	B3B_LVDS_B15_N	P2	IO
F30	GND	GND	-	POWER
F31	HB12_P	GPIO1_IO22	H17	IO
F32	HB12_N	GPIO1_IO17	F18	IO
F33	GND	GND	-	POWER
F34	HB16_P	GND	-	-
F35	HB16_N	GND	-	-
F36	GND	GND	-	POWER
F37	HB20_P	GND	-	-
F38	HB20_N	GND	-	-
F39	GND	GND	-	POWER
F40	VADJ	+1.8V	-	POWER

Table 4.7: J300 Connector Pin G1-G40 Assignments

Pin	FMC Signal	Baseboard/SOM Signal	FPGA Ball	Type
G1	GND	GND	-	POWER
G2	CLK1_M2C_P	GND	-	-
G3	CLK1_M2C_N	GND	-	-
G4	GND	GND	-	POWER
G5	GND	GND	-	POWER
G6	LA00_P_CC	CLK2A_P	AG14	IO
G7	LA00_N_CC	CLK2A_N	AG15	IO
G8	GND	GND	-	POWER
G9	LA03_P	B2A_LVDS_B1_P	AE11	IO
G10	LA03_N	B2A_LVDS_B1_N	AE10	IO
G11	GND	GND	-	POWER
G12	LA08_P	B2A_LVDS_B24_P	AC12	IO
G13	LA08_N	B2A_LVDS_B24_N	AC11	IO
G14	GND	GND	-	POWER
G15	LA12_P	B2A_LVDS_B15_P	AC16	IO
G16	LA12_N	B2A_LVDS_B15_N	AC17	IO
G17	GND	GND	-	POWER
G18	LA16_P	B2A_LVDS_B7_P	AG18	IO
G19	LA16_N	B2A_LVDS_B7_N	AF19	IO
G20	GND	GND	-	POWER
G21	LA20_P	B2A_LVDS_B16_P	AD18	IO
G22	LA20_N	B2A_LVDS_B16_N	AC18	IO
G23	GND	GND	-	POWER
G24	LA22_P	B3B_LVDS_B6_P	U8	IO
G25	LA22_N	B3B_LVDS_B6_N	V8	IO
G26	GND	GND	-	POWER
G27	LA25_P	B3B_LVDS_B14_P	H1	IO
G28	LA25_N	B3B_LVDS_B14_N	G1	IO
G29	GND	GND	-	POWER
G30	LA29_P	B3B_LVDS_B9_P	N2	IO
G31	LA29_N	B3B_LVDS_B9_N	N3	IO
G32	GND	GND	-	POWER
G33	LA31_P	B3B_LVDS_B24_P	W3	IO
G34	LA31_N	B3B_LVDS_B24_N	V3	IO
G35	GND	GND	-	POWER
G36	LA33_P	B3B_LVDS_B11_P	K2	IO
G37	LA33_N	B3B_LVDS_B11_N	J2	IO
G38	GND	GND	-	POWER
G39	VADJ	+1.8V	-	POWER
G40	GND	GND	-	POWER

Table 4.8: J300 Connector Pin H1-H40 Assignments

Pin	FMC Signal	Baseboard/SOM Signal	FPGA Ball	Type
H1	VREF_A_M2C	-	-	NC
H2	PRSNT_M2C_L	GPIO0_IO7	F19	IO
H3	GND	GND	-	POWER
H4	CLK0_M2C_P	-	-	NC
H5	CLK0_M2C_N	-	-	NC
H6	GND	GND	-	POWER
H7	LA02_P	B2A_LVDS_B20_P	AB14	IO
H8	LA02_N	B2A_LVDS_B20_N	AA14	IO
H9	GND	GND	-	POWER
H10	LA04_P	B2A_LVDS_B9_P	AF13	IO
H11	LA04_N	B2A_LVDS_B9_N	AF14	IO
H12	GND	GND	-	POWER
H13	LA07_P	B2A_LVDS_B4_P	AE12	IO
H14	LA07_N	B2A_LVDS_B4_N	AD12	IO
H15	GND	GND	-	POWER
H16	LA11_P	B2A_LVDS_B8_P	AF17	IO
H17	LA11_N	B2A_LVDS_B8_N	AF18	IO
H18	GND	GND	-	POWER
H19	LA15_P	B2A_LVDS_B11_P	AG16	IO
H20	LA15_N	B2A_LVDS_B11_N	AF16	IO
H21	GND	GND	-	POWER
H22	LA19_P	B2A_LVDS_B10_P	AE19	IO
H23	LA19_N	B2A_LVDS_B10_N	AE20	IO
H24	GND	GND	-	POWER
H25	LA21_P	B3B_LVDS_B1_P	P3	IO
H26	LA21_N	B3B_LVDS_B1_N	P4	IO
H27	GND	GND	-	POWER
H28	LA24_P	B3B_LVDS_B7_P	M3	IO
H29	LA24_N	B3B_LVDS_B7_N	M4	IO
H30	GND	GND	-	POWER
H31	LA28_P	B3B_LVDS_B4_P	R4	IO
H32	LA28_N	B3B_LVDS_B4_N	R5	IO
H33	GND	GND	-	POWER
H34	LA30_P	B3B_LVDS_B17_P	L1	IO
H35	LA30_N	B3B_LVDS_B17_N	K1	IO
H36	GND	GND	-	POWER
H37	LA32_P	B3B_LVDS_B3_P	T6	IO
H38	LA32_N	B3B_LVDS_B3_N	T7	IO
H39	GND	GND	-	POWER
H40	VADJ	+1.8V	-	POWER

Table 4.9: J300 Connector Pin J1-J40 Assignments

Pin	FMC Signal	Baseboard/SOM Signal	FPGA Ball	Type
J1	GND	GND	-	POWER
J2	CLK3_BIDIR_P	-	-	NC
J3	CLK3_BIDIR_N	-	-	NC
J4	GND	GND	-	POWER
J5	GND	GND	-	POWER
J6	HA03_P	B3A_LVDS_B22_P	AF6	IO
J7	HA03_N	B3A_LVDS_B22_N	AE6	IO
J8	GND	GND	-	POWER
J9	HA07_P	B3A_LVDS_B23_P	AG4	IO
J10	HA07_N	B3A_LVDS_B23_N	AF4	IO
J11	GND	GND	-	POWER
J12	HA11_P	B3A_LVDS_B17_P	AG1	IO
J13	HA11_N	B3A_LVDS_B17_N	AF1	IO
J14	GND	GND	-	POWER
J15	HA14_P	B3A_LVDS_B13_P	AD3	IO
J16	HA14_N	B3A_LVDS_B13_N	AC3	IO
J17	GND	GND	-	POWER
J18	HA18_P	B3A_LVDS_B5_N	Y2	IO
J19	HA18_N	B3A_LVDS_B5_P	Y1	IO
J20	GND	GND	-	POWER
J21	HA22_P	B3A_LVDS_B6_P	AA9	IO
J22	HA22_N	B3A_LVDS_B6_N	AA8	IO
J23	GND	GND	-	POWER
J24	HB01_P	B3B_LVDS_B16_P	T2	IO
J25	HB01_N	B3B_LVDS_B16_N	T3	IO
J26	GND	GND	-	POWER
J27	HB07_P	B3B_LVDS_B5_P	T4	IO
J28	HB07_N	B3B_LVDS_B5_N	U5	IO
J29	GND	GND	-	POWER
J30	HB11_P	GPIO1_IO19	K17	IO
J31	HB11_N	GPIO1_IO12	G20	IO
J32	GND	GND	-	POWER
J33	HB15_P	GND	-	-
J34	HB15_N	GND	-	-
J35	GND	GND	-	POWER
J36	HB18_P	GND	-	-
J37	HB18_N	GND	-	-
J38	GND	GND	-	POWER
J39	VIO_B_M2C	-	-	NC
J40	GND	GND	-	POWER

Table 4.10: J300 Connector Pin K1-K40 Assignments

Pin	FMC Signal	Baseboard/SOM Signal	FPGA Ball	Type
K1	VREF_B_M2C	-	-	NC
K2	GND	GND	-	POWER
K3	GND	GND	-	POWER
K4	CLK2_BIDIR_P	-	-	NC
K5	CLK2_BIDIR_N	-	-	NC
K6	GND	GND	-	POWER
K7	HA02_P	B3A_LVDS_B10_P	AA2	IO
K8	HA02_N	B3A_LVDS_B10_N	AB3	IO
K9	GND	GND	-	POWER
K10	HA06_P	B3A_LVDS_B15_P	AC1	IO
K11	HA06_N	B3A_LVDS_B15_N	AC2	IO
K12	GND	GND	-	POWER
K13	HA10_P	B3A_LVDS_B14_P	AE1	IO
K14	HA10_N	B3A_LVDS_B14_N	AF2	IO
K15	GND	GND	-	POWER
K16	HA17_P_CC	B3A_LVDS_B11_P	AA3	IO
K17	HA17_N_CC	B3A_LVDS_B11_N	AA4	IO
K18	GND	GND	-	POWER
K19	HA21_P	B3A_LVDS_B3_P	Y7	IO
K20	HA21_N	B3A_LVDS_B3_N	Y6	IO
K21	GND	GND	-	POWER
K22	HA23_P	B3A_LVDS_B4_P	W5	IO
K23	HA23_N	B3A_LVDS_B4_N	Y5	IO
K24	GND	GND	-	POWER
K25	HB00_P_CC	B3B_LVDS_B13_P	N1	IO
K26	HB00_N_CC	B3B_LVDS_B13_N	M1	IO
K27	GND	GND	-	POWER
K28	HB06_P_CC	B3B_LVDS_B10_P	H2	IO
K29	HB06_N_CC	B3B_LVDS_B10_N	J3	IO
K30	GND	GND	-	POWER
K31	HB10_P	GPIO1_IO18	J17	IO
K32	HB10_N	GPIO1_IO20	J18	IO
K33	GND	GND	-	POWER
K34	HB14_P	GPIO1_IO21	J19	IO
K35	HB14_N	B2A_LVDS_B19_N	AA11	IO
K36	GND	GND	-	POWER
K37	HB17_P_CC	GND	-	-
K38	HB17_N_CC	GND	-	-
K39	GND	GND	-	POWER
K40	VIO_B_M2C	-	-	NC

Notes:
1. The maximum total current supplied to external components from the +1.8V supply should be limited to less than 4.0A.
2. The maximum total current supplied to external components from the +12V supply should be limited to less than 1.0A.

Please see the following VITA documentation concerning the FMC specification (https://www.vita.com/fmc).

10/100/1000 Ethernet Interface – J400

The MitySOM-A10S Development Kit provides a RJ-45 connection for a Gigabit 10/100/1000 Ethernet connection. This connection follows standard TIA/EIA-568B pin-out as shown in Table below. The Ethernet PHY, Micrel KSZ9031, will auto negotiate to the speed of the device it is connected to.

Table 5: J500 Ethernet RJ45 Pin Assignments

Pin	Signal	Type
1	TXRXA_P	I/O
2	TXRXA_N	I/O
3	TXRXB_P	I/O
4	TXRXB_N	I/O
5	TXRXC_P	I/O
6	TXRXC_N	I/O
7	TXRXD_P	I/O
8	TXRXD_N	I/O

Included Components

The following table lists the components that are included with a MitySOM-A10S Development Kit. See Table for specific development kit ordering information.

Table 6: Included Items

Description	Interface Port	Qty. Included
MitySOM-A10S Development Kit Board	n/a	Qty. 1
MitySOM-A10S Module	J201, J202	Qty. 1
J202 Interposer	J202	Qty. 1
Micro USB Cable for Debug Console	J600	Qty. 1
12V 5A AC to DC Supply	P700	Qty. 1
Ethernet cable	J400	Qty. 1
USB Drive with Development Environment	n/a	Qty. 1
Development Kit Quick Start Guide	n/a	

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Syracuse, NY 13211
PHONE 315.425.4045
www.criticallink.com

MitySOM-A10S Development Kit Board with MitySOM-A10S Module

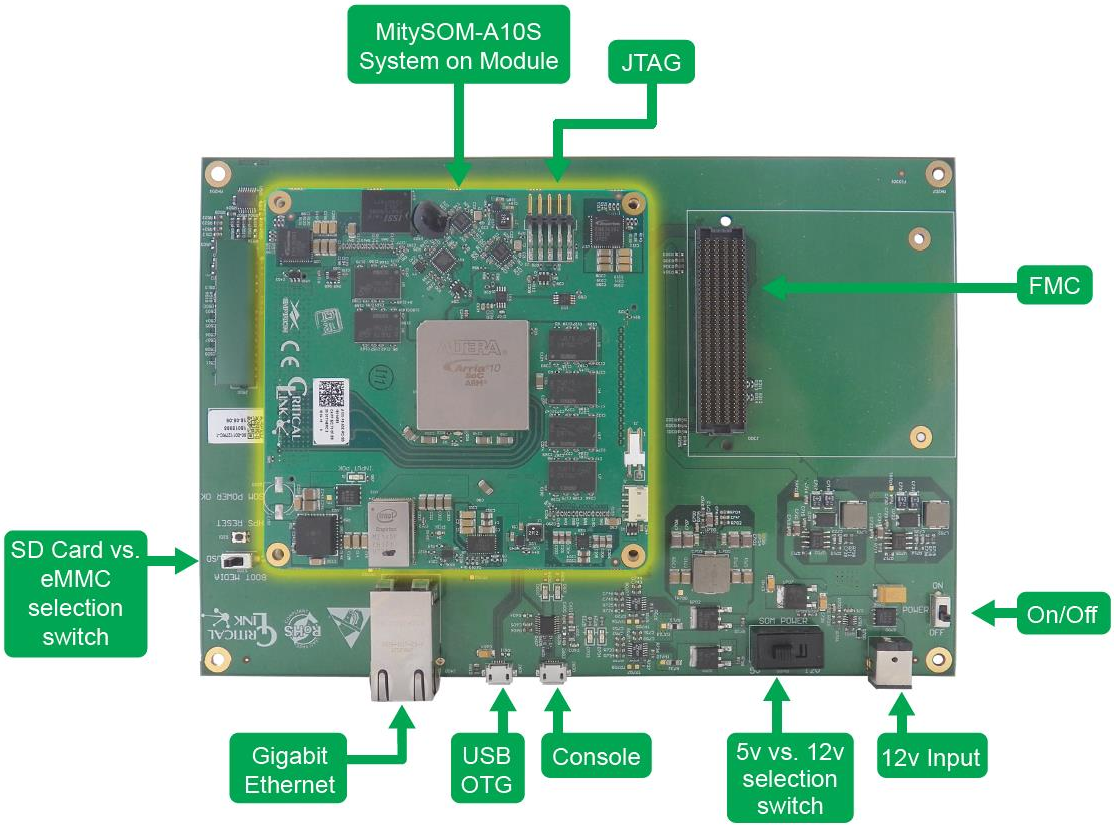

Figure 2: MitySOM-A10S Development Kit Interfaces

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ORDERING INFORMATION

Development Kits

The following table lists the standard MitySOM-A10S Development Kit configurations. For shipping status, availability, and lead time of these or other configurations please contact Critical Link at info@criticallink.com.

Table 7: Standard Model Numbers

Development Kit P/N	Module Included
80-001201	A10S-P8-X5E-RC-SA

MECHANICAL INTERFACE DESCRIPTION

Main Board Interface / Mounting

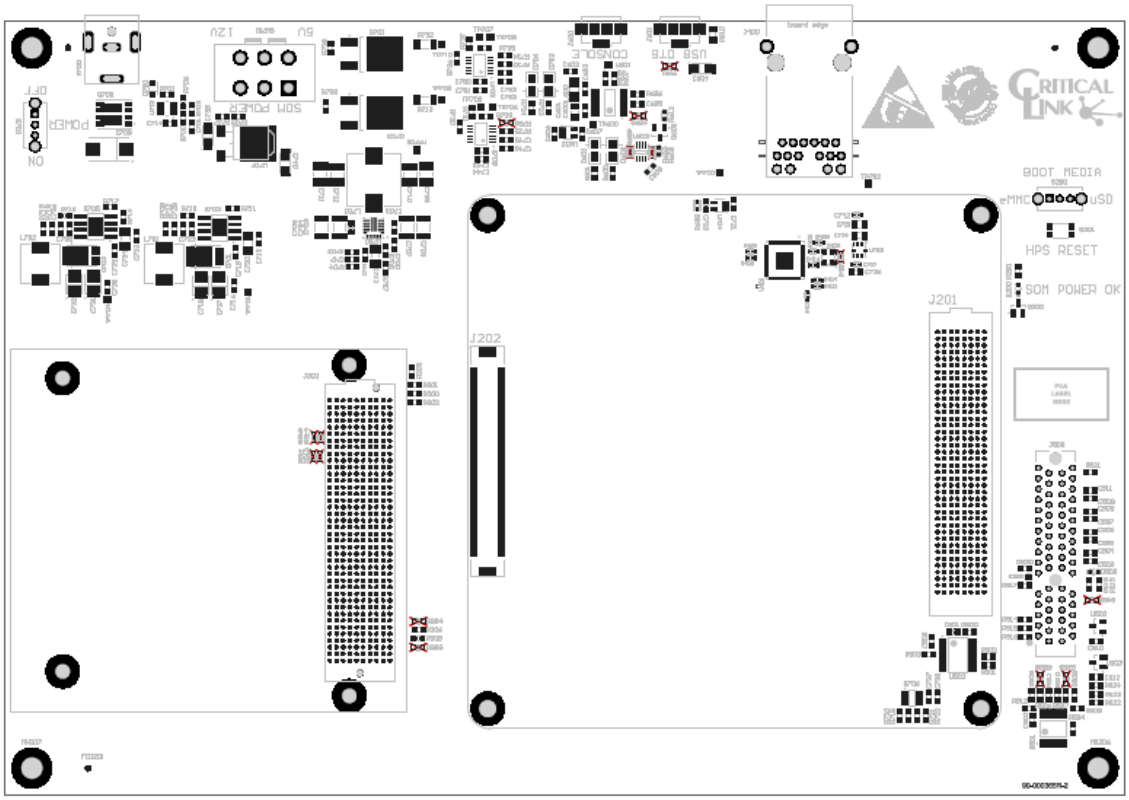

Figure 3: MitySOM-A10S Development Kit Outline, Mounting Hole Locations, (Top View)

REVISION HISTORY

Revision	Date	Change Description
1A	11/01/18	Initial Release
1B	12/12/18	Added table for max rating/operating conditions

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