FEATURES

- **Intel Arria 10 SX Processor**
  - Dual ARM Cortex- A9 MPU
  - Up to 1500 MHz Max clock speed
  - Dual NEON SIMD Coprocessors
  - 32 KB L1 Program Cache (per core)
  - 32 KB L1 Data Cache (per core)
  - 512 KB L2 Cache (shared)
  - 256 KB on-chip RAM
  - Up to 138 User FPGA I/O Pins
  - 12 Transceiver Pairs > 8 Gbps

- **Memory Interfaces**
  - Bank 1 : Up to 4 GB DDR4
    - 32 bits wide
    - 8.2 GB/sec burst transfer rate
    - Shared with HPS
  - Bank 2 : Up to 2 GB DDR4
    - 16 bits wide
    - 4.1 GB/sec burst transfer rate

- Integrated Power Management
- JTAG connector on-module
- On Board USB 2.0 PHY
- On Board MicroSD Card Interface
- Power, Reset and Clock Management

- **FPGA Fabric**
  - Up To 480K Logic Elements (LE)
  - 460Mhz Global Clock
  - Up To 28Mb M20K Memory
  - Up To 4.3Mb MLAB Memory
  - Up To 1368 Floating Point Multipliers
  - Up To 2736 Fixed Point Multipliers
  - 32 Global Clock Networks

- **Serial Transceivers**
  - 8 Gbps Transceivers
  - 1 x8 PCIe Hard IP Block (Up to Gen 3)
  - 1 x4 Bonded Set

- **Mechanical**
  - 101.5 x 101.5 mm (4x4")
  - Dual Samtec 120 pin board to board connectors on top and bottom for stacking form factor.
  - Additional Samtech 120 pin board to board connector for PCIe block populated bottom or on top at time of order.

- **Hard Processor System (HPS)**
  - Selection of boot sources
  - Up to 3 10/100/1000 Mbps Ethernet MACs
  - Up to 2 USB 2.0 OTG Ports
  - Up to 2 UARTs
  - 1 MMC/SD/SDIO
  - Up to 4 SPI controllers
  - Up to 5 I2C controllers

APPLICATIONS

- Machine Vision
- Life Science Vision applications
- Test and Measurement
- Embedded Instrumentation
- Industrial Automation and Control
- Industrial Instrumentation
- Medical Instrumentation

BENEFITS

- Rapid Development / Deployment
- Multiple Connectivity and I/O Options
- Rich User Interfaces
- High System Integration
- Supports OpenCL and HLS acceleration
- High Level OS Support
  - Embedded Linux

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Syracuse, NY 13211 FAX 315.425.4048
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DESCRIPTION

The MitySOM-A10S with Dual Side Connectors (MitySOM-A10S-DSC) is a highly configurable, medium form-factor System-on-Module (SOM) featuring an Intel Arria 10 System-on-Chip (SoC). In addition to the processor, the module includes on-board power supplies, two DDR4 RAM memory subsystems, micro SD card, a USB 2.0 on the go (OTG) port, and a temperature sensor. The MitySOM-A10S-DSC provides a complete and flexible CPU infrastructure for highly integrated embedded systems.

The MitySOM-A10S-DSC is available with a 270 K Logic Element (KLE) Arria 10 SX which provides Dual-core Cortex-A9 32-bit RISC processors with dual NEON SIMD coprocessors. Options for up to 480 KLE devices are available. This MPU can run a rich set of real-time operating systems containing software applications programming interfaces (APIs) expected by modern system designers. The ARM architecture supports several operating systems, including Linux.

Figure 1 illustrates a block diagram of the MitySOM-A10S-DSC. As shown in the figure, the primary interface to the MitySOM-A10S-DSC is through two 120-Pin vertical board-to-board mezzanine connectors, one on the top of the card and one on the bottom. An additional 120-pin board-to-board connector may be installed on either the top side or bottom side of the card to provide access to 8 additional transceiver pairs and clocks. The MitySOM-A10S-DSC is intended to fit into a stacked card system. Details of the board-to-board interfaces are included in the Interface Description section.

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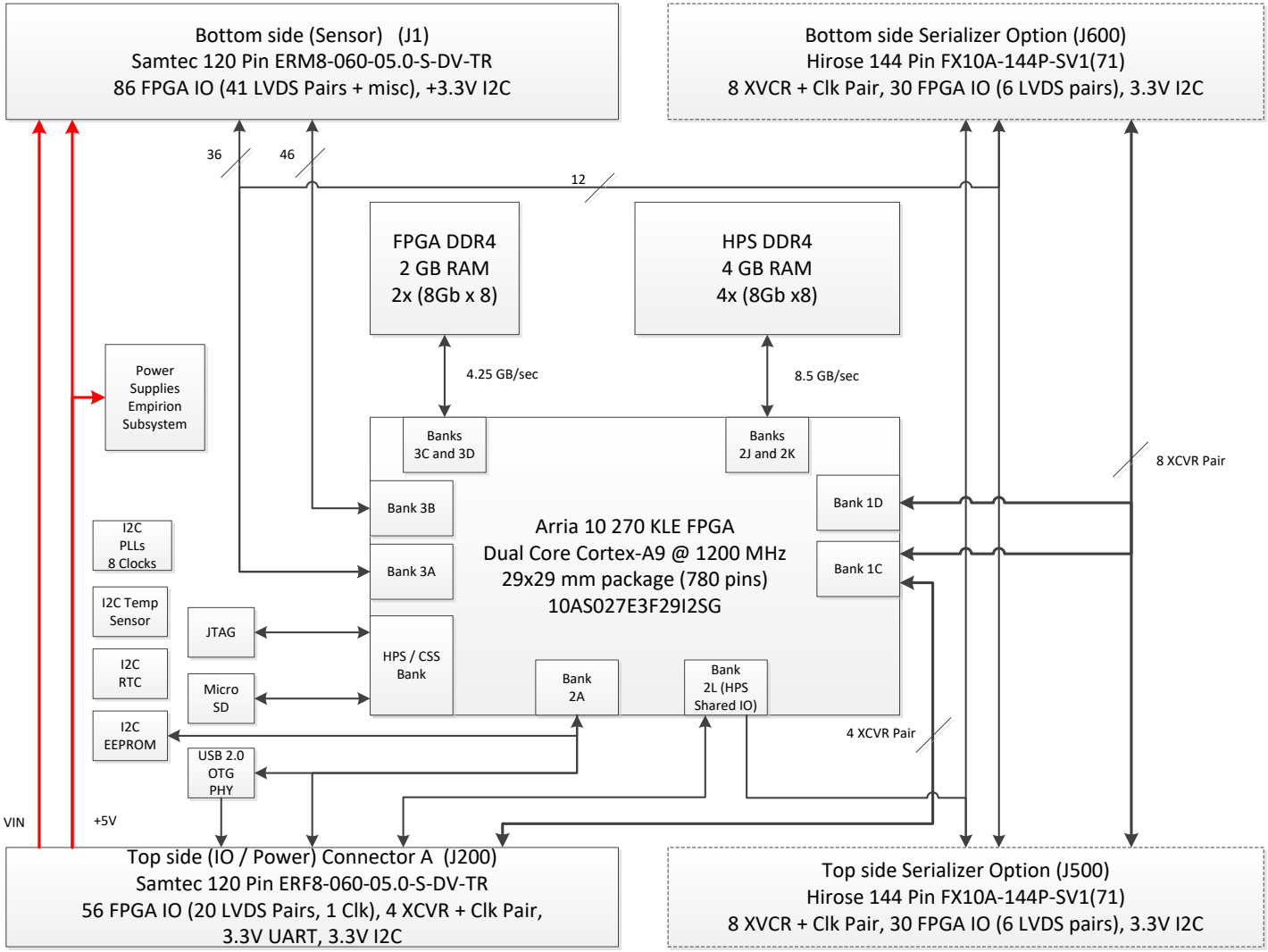

Figure 1 MitySOM-A10S-DSC Block Diagram

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DDR4 Memory – HPS Shared Memory

The MitySOM-A10S-DSC includes a dedicated 32-bit DDR4 memory interface that can address a maximum of 4GB of RAM. This DDR4 memory is available for both the HPS (Cortex-A9 ARM cores) as well as the FPGA fabric through either the AXI or Avalon high speed interfaces internal to the Arria 10.

The MitySOM-A10S-DSC family adheres to Intel's Arria 10 maximum memory speeds. The HPS memory clocked at 1033Mhz using a local on-board PLL as the maximum and a slower speed may be selected to reduce power consumption.

DDR4 Memory – FPGA Memory

The MitySOM-A10S-DSC includes a dedicated 16-bit DDR4 memory interface that can address a maximum of 2GB of RAM. This DDR4 memory is available for the FPGA fabric through either the AXI or Avalon high speed interfaces internal to the Arria 10. Using an appropriate arbiter is possible to allow HPS access to this memory region.

The MitySOM-A10S-DSC family adheres to Intel's Arria 10 maximum memory speeds. The HPS memory clocked at 1033Mhz using a local on-board PLL as the maximum and a slower speed may be selected to reduce power consumption.

HPS-FPGA AXI

The high bandwidth HPS-FPGA AXI bridges provided by Intel in the Arria 10 SoC allow masters in the FPGA fabric to communicate with slaves in the HPS logic and vice versa. These bridges can be configured for 32, 64, or 128 bit widths.

For example, designers can instantiate additional memories or peripherals in the FPGA fabric, and master interfaces belonging to components in the HPS logic can access them. Designers can also instantiate components such as a Nios® II processor in the FPGA fabric and their master interfaces can access memories or peripherals in the HPS logic, including DDR4 Memory – HPS Shared Memory.

Configuration EEPROM

MitySOM-A10S-DSC modules contain a 2048 x 8-bit EEPROM that is used to hold factory configuration data for the module. The EEPROM is connected to the Arria 10 using the I2C0 interface. This EEPROM contains information such as the module type, Serial Number, and MAC addresses for the Ethernet interface(s). This EEPROM is not available for customer use.

Dedicated HPS Interfaces

The following HPS interfaces have been dedicated as fixed function in order to support proper operation. The module was designed to allow as many HPS fixed and Shared IO pins to be user accessible as possible.

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Console Serial port

The console serial port (UART1) is supported on pins 17 (RX) and 16 (TX) of the 120-Pin Top Side Connector (J200) with 3.3V compatible asynchronouse UART I/O. By default, the flow control signals are not enabled but can be added to the console serial interface if desired.

Please reference the J200 Pin-Out for specific Arria 10 pin-connections.

I2C0 Interface

The I2C0 peripheral is consumed local to the module. It is used for the Real Time Clock, temperature sensors, and Configuration EEPROM.

Table 1: I2C0 Peripherals

Address	Device	Feature
1010XXX	FT24C16A	16Kbit EEPROM for factory config parameters
0110010	AB-RTCMK	Real Time Clock
1001000	AD7415ARTZ	Board / SDRAM temperature sensor
0011000	LM95235	Arria 10 core temperature sensor

I2C EMAC2 Interface

The I2C EMAC 2 peripheral is consumed local to the module. It is used for two quad programmable differential clock generators. The clock generators are used to provide stable clock sources (266 MHz) for the HPS EMIF DDR4 PLL as well as the FPGA EMIF DDR4 PLL.

Table 2: I2C EMAC 2 Peripherals

Address	Device	Feature
1110000	SI5338B	Quad Differential Clock Generator
1110001	SI5338B	Quad Differential Clock Generator

USB-2.0 OTG PHY

The USB1 interface of the Arria 10 processor is connected directly to a USB 2.0 OTG Physical Interface (PHY) on the PCA. The necessary USB ID, power and data pins are available on the Top Side board to board connector (J200) of the module. Please see Table 6 for the specific pin locations.

MicroSD / MMC Card

The HPS SD/MMC controller peripheral is connected via the HPS Bank to a micro-SD style connector (J103) on the PCA using a 1.8V (HPS side) to 3.3V level translator. The micro-SD media is the primary boot and filesystem media for the default configuration of the MitySOM-A10S-DSC PCA.

Debug JTAG

The JTAG interface signals for the Arria 10 FPGA fabric processor have been brought out to a 10 pin dual row 0.1” right angle header, J2. The connector is intended for use with a standard USB 2 Blaster JTAG adapter.

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External Interfaces

The Arria 10 makes extensive use of functional pin multiplexing to provide a highly configurable device that can be tailored to a multitude of applications.

HPS Interfaces

A list of the interfaces/functions that are available to the user from the HPS is provided below.

- 1 Universal Serial Bus (USB) 2.0 High-Speed On-The-Go (OTG) port
- Up to 3 Gigabit Ethernet MAC's (10/100/1000 Mbps)
- Up to 4 Serial Peripheral (SPI) ports
- 2 Universal Asynchronous Receive/Transmit (UART) ports
- 5 Inter-Integrated Circuit (I2C) ports
    - I2C0 is connected to the on-board EEPROM, Temperature Sensor, and RTC using 3.3V level translation
    - I2C EMAC2 is connected to two SI5338 PLLs and it not available on the external connector interface.
    - I2C1 is dedicated and is level translated to 3.3V for use on the Top and Bottom side Samtech connectors

Additionally, most of the pin multiplexed signals can be configured as general purpose I/O signals with interrupt capability.

FPGA Interfaces

GPIO

Up to 170 FPGA IO pins are available externally to the module. Of these pins, up to 67 LVDS pairs may be configured as transmitters or receivers.

The FPGA IO pins provided on the top side board to board connector (J200) are connected to Banks 2A and 2L of the Arria 10 FPGA. The FPGA IO pins on the Bottom side board to board connector are connected Banks 3A and 3B of the Arria 10 FPGA. All of the I/O banks are connected to 1.8V, and can support mixed standards including LVDS, 1.8V HSTL, and 1.8V single ended logic.

8 Gbps Transceivers

A total of twelve high speed transceiver pairs are available on the module for supporting high speed serial interfaces. 4 of the pairs are routed to top side J200 120 pin Samtech connector and may be bonded to support protocols such as HDMI, CoXpress, etc. The remaining 8 pairs, which may be bonded to a hard Gen 3 compliant PCIe controller core, are routed to a second 144 pin Hirose connector that may be placed either on the top side or bottom side of the card (determined at time of order). The module includes a local PLL clock circuit that may be used for a reference clock source for use with the transceiver logic, or a reference clock may be provided externally.

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Configuration and Boot Modes

The Arria 10 has two groups of pins, documented below, that are read during reset to determine which media to boot from for the HPS (BSEL pins) and one group of pins that is used to configure the FPGA (MSEL pins). On the MitySOM-A10S-DSC, the BSEL and MSEL pins are strapped to fixed settings on board as described below. There is also a set of user-programmable fuses stored in the HPS_fusesec register of the Arria 10. The HPS_fusesec fuses are not modified by Critical Link and will be at the default values outlined in the Intel Arria 10 Hard Processor System Technical Reference Manual. The MitySOM provides a local 50 MHz clock source to the HPS_CLK1 pin for HPS booting purposes.

HPS Configuration pins

The BSEL and MSEL pins determine which memory interface has the bootloader and how to clock the interface.

BSEL (HPS Boot Select at Reset)

The MitySOM-A10S-DSC standard option is to boot from an installed MicroSD card flash memory (at 3.0V, BSEL pin option 5). Note: the pins for BSEL0 and BSEL1 are exposed on the board to board connectors to allow use after power up. Care must be taken to ensure these pins are floating during power up.

FPGA Configuration Pins

The FPGA MSEL configuration input pins are all pulled down to ground with a 1.0K resistors on the MitySOM-A10S-DSC, selecting the Fast Passive Parallel (FPP) x16 mode. The FPGA should be configured using either the HPS internal FPGA manager or optionally using the JTAG interface.

General Status LED's

Power OK

D4 indicates the MitySOM-A10S-DSC on-module +3.3V supply is operating.

Configuration Debug

D2 is connected to the nSTATUS configuration pin of the FPGA. When lit, it indicates a programming error occurred during FPGA fabric configuration.

D3 indicates that FPGA configuration is not complete by lighting a yellow LED. It is connected to the CONF_DONE pin of the FPGA. This is only a warning rather than an error because the HPS can still boot and load the FPGA. This LED should turn on during initial power up until the FPGA is programmed.

Power Interfaces

The MitySOM-A10S-DSC is powered using the +5V DC (+5VIN) input and ground pins on the top side board to board connector. The MitySOM-A10S-DSC processor generates a +3.3V, +2.5V, +1.8V, +1.2V, +0.6V, 0.9V and +0.95V core voltages from the supplied +5V power supply for powering the local electronics. The MitySOM-A10S-DSC processor provides the +3.3V, +2.5V, and +1.8V supply voltages to both the top and bottom connectors to support

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powering external electronics and proper supply sequencing for interfaces to the FPGA bank IO.

In addition, the MitySOM-A10S-DSC allows several electrical pass-through connections between the top and bottom interfaces in order to allow providing custom power supplies and/ or signaling between the interface boards. These nets include the +12V, -5.0V, SPARE_V0, and SPARE_V1 signals present on both interfaces. The MitySOM-A10S-DSC does not reference these nets, it simply connects them between the two 120 pin Samtech connectors.

Software and Application Development Support

Users of the MitySOM-A10S-DSC are encouraged to develop applications using the MitySOM-A10S-DSC software development kit (SDK) provided by Critical Link LLC. The SDK is an expansion of the Intel platform support package for the Arria 10 and includes an implementation of a Yocto Project-compatible board support package providing a Linux root filesystem/distribution and compatible gcc compiler tool-chain with debugger.

Growth Options

The MitySOM-A10S-DSC has been designed to support several upgrade options. These options include a range of speed grades, FPGA density, HPS DDR memory configurations, and operating temperature specifications including commercial and industrial temperature ranges. The available options are listed in the section below containing ordering information. For additional ordering information and details regarding these options, or to inquire about a configuration not listed below, please contact a Critical Link sales representative.

Absolute Maximum Ratings

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office (info@criticallink.com) or unit Distributors for availability and specifications.

Table 3: Absolute Maximum Ratings

Maximum Supply Voltage (+5VIN)	5.2V
Storage Temperature Range	-55°C to 150°C

Operating Conditions

The following are the minimum temperature ratings for the components that are installed on a MitySOM-A10S-DSC. For specifications not contained in this table please contact a Critical Link sales representative. Please see the Thermal Management section below concerning ambient/operating temperature recommendations.

Table 4: Module Component Temperature Ratings (minimum)

Temperature Range	**Component Ratings**
Commercial (-RC)	0°C to 70°C
Industrial (-RI)	-40°C to 85°C

Thermal Management

The MitySOM-A10S-DSC module requires careful consideration of thermal management. Depending on load, different thermal management will be required for operation at room

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temperatures and above. The primary thermal concern is with the Arria 10 SoC device. Even when idle, case temperature on this device rises significantly. Additional processing activity will require more power consumption and more heat dissipation.

Thermal management is a system level issue that must be addressed in conjunction with the overall system design. Some systems may have available airflow with limited space for a heat sink; others may have room for a heat sink with or without the possibility for additional airflow. As a result, the approach taken for thermal management is a design consideration that must be addressed by the overall system designers when integrating the MitySOM-A10S-DSC.

Every end product is different and it is advisable to perform thorough testing to ensure that the product will meet desired performance and longevity specifications. Customers should use Intel's Early Power Estimator (EPE) for the Arria 10. This utility will assist in estimating the potential power usage of the processor for a given application. Details can be found on the PowerPlay EPE[1] page at Intel.com. To achieve reliable operation at the maximum specified operating temperatures it has been determined that some form of thermal management (e.g., forced air, heat sink, etc.) will be required.

J2 Interface Description

The connector for J2, is a TSM-105-01-L-DH-A, a 0.1" 5x2 dual row male header interface. The interface is designed to mate with a USB Blaster II JTAG interface pod according to Intel's UG-USB81204 specifications for USB-Blaster Download Cable. The interface is described in the table below.

Table 5 J2 Connector Pin Assignments

Pin	Name	I/O	Description
1	TCK	Input	Clock Signal (pulled to GND with 1.8K resistor)
2	GND	Input	Signal Ground
3	TDO	Output	Data From Device
4	+1V8	Output	Target Power Supply from Module.
5	TMD	Input	JTAG State Machine Control (pulled to 1.8V with 10Kresistor)
6	PROC_RST	Input	Active Low Signal for hard processor reset (pulled to 1.8V with 10K resistor)
7	NC	-	No Connect / Key
8	JTAG_TRST	Input	JTAG TRST Signal. Pulled to 1.8V via 1K resistor
9	TDI	Input	Data to Device. Pulled to 1.8V via 10K resistor
10	GND	Input	Signal Ground

J100, J200 and J500/J600 Connector Interfaces

The next sections outline the connector pin interfaces. The pin interfaces are grouped into the signal classes defined in the table below.

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Class	Applicable IO Standard	Description
POWER	N/A	These are module power input pins and corresponding return pins.
XCVR_TX	High Speed Differential I/O	These pins are directly connected to the Gigabit Transceiver Transmit lanes of the Arria 10. VCCT is set to 0.95V for all transceiver banks.
XCVR_RX	CML, Differential LVPECL, LVDS, HCSL	These pins are directly connected to the Gigabit Transceiver Receive lanes of the Arria 10. CML, Differential LVPECL, and LVDS must be AC Coupled. VCCR is set to 0.95V for all transceiver banks.
XCVR_REFCLK	CML Differential LVPECL, LVDS	These pins are directly connected to the Gigabit Transceiver Reference input clocks.
IO_1V8	1.8V CMOS	These pins are directly connected to FPGA Bank IO pins, but cannot be used for LVDS IO. The Bank voltage is 1.8 V.
LVDSIO_1V8	LVDS, 1.8V CMOS, SSTL-18, HSTL-18	These pins are directly connected to FPGA Bank IO pins that may be configured for LVDS IO. The bank voltage is 1.8 volts.
SHAREDIO_1V8	1.8V CMOS	These pins are connected to shared FPGA or HPS pins in one of the Arria 10 HPS shared bank quadrants. The bank voltage for these pins are 1.8 V.
FFIO_1V8	1.8V CMOS	These are fixed function pins using 1.8V CMOS Logic Levels.
FFIO_3V3	3.3V CMOS	These are fixed function pins using 3.3V CMOS logic levels.
FFIO	Various	These are fixed function pins. See the interface description for details.
HPSIO_1V8	1.8V CMOS	These pins are connected to the HPS bank IO pins. The bank voltage for these pins is 1.8V.
CLKOUT	LVDS or CML	These pins are directly connected to a local si5338B phase locked loop chip output driver and may be used for external clock generation.

Top Side Interface Description (J200)

One of two primary interface connectors for the MitySOM-A10S-DSC is the 120-pin board to board interface, J200. The connector used for J-200 is a Samtech ERF8-060-05.0-S-DV-TR, which mates with Samtech ERM8-060-05.0-S-DV-TR. The mating height may be taller if desired. The design of this interface was intended to support as much compatibility with the MitySOM-5CSx-DSC (a Cyclone V based processor platform) as possible. Table 6 contains a summary of the MitySOM-A10S-DSC Top Side Interface pin-mapping.

Table 6: MitySOM-A10S-DSC Top Side Connector Pin-Out (J200)

Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Notes / Alternate HPS Mux functions
1	POWER	GND	-	-	
2	POWER	GND	-	-	
3	POWER	+12V	-	-	
4	POWER	+3V3	-	-	
5	POWER	+5VIN	-	-	Main Supply Input
6	POWER	-5.0V	-	-	
7	POWER	+5VIN	-	-	Main Supply Input
8	POWER	+1V8	-	-	
9	POWER	+5VIN	-	-	Main Supply Input
10	POWER	SPARE_V0	-	-	Connected to J202 only
11	POWER	GND	-	-	
12	POWER	SPARE_V1	-	-	Connected to J202 only
13	FFIO_3V3	I2C1_SCL	2L	C16	+3.3V Level Translated
14	POWER	GND	-	-	
15	FFIO_3V3	I2C1_SDA	2L	C17	+3.3V Level Translated
16	FFIO_3V3	UART0_TX	HPS	K15	+3.3V Level Translated
17	FFIO_3V3	UART0_RX	HPS	F13	+3.3V Level Translated

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Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Notes / Alternate HPS Mux functions
18	POWER	GND	-	-	
19	POWER	GND	-	-	
20	IO_1V8	pRESTL0_LVDS2A_19p	2A	AB11	nPERSTL0/LVDS2A_19p
21	IO_1V8	B2A_LVDS_B10_N	2A	AE20	PLL_2A_CLKOUT1n/LVDS2A_10n
22	LVDSIO_1V8	B2A_LVDS_B19_N	2A	AA11	LVDS2A_19N
23	LVDSIO_1V8	B2A_LVDS_B10_P	2A	AE19	PLL_2A_CLKOUT1p/LVDS2A_10p
24	LVDSIO_1V8	B2A_LVDS_B16_N	2A	AC18	LVDS2A_16n
25	POWER	GND	-	-	
26	LVDSIO_1V8	B2A_LVDS_B16_P	2A	AD18	LVDS2A_16p
27	LVDSIO_1V8	B2A_LVDS_B8_N	2A	AF18	LVDS2A_8n
28	LVDSIO_1V8	B2A_LVDS_B7_N	2A	AF19	LVDS2A_7n
29	LVDSIO_1V8	B2A_LVDS_B8_P	2A	AF17	LVDS2A_8p
30	LVDSIO_1V8	B2A_LVDS_B7_P	2A	AG18	LVDS2A_7p
31	LVDSIO_1V8	B2A_LVDS_B3_P	2A	AE16	LVDS2A_3p
32	LVDSIO_1V8	B2A_LVDS_B5_P	2A	AF12	LVDS2A_5p
33	LVDSIO_1V8	B2A_LVDS_B3_N	2A	AD15	LVDS2A_3n
34	LVDSIO_1V8	B2A_LVDS_B5_N	2A	AF11	LVDS2A_5n
35	LVDSIO_1V8	B2A_LVDS_B2_P	2A	AE15	LVDS2A_2p
36	LVDSIO_1V8	B2A_LVDS_B17_N	2A	AD17	LVDS2A_17n
37	LVDSIO_1V8	B2A_LVDS_B2_N	2A	AE14	LVDS2A_2n
38	LVDSIO_1V8	B2A_LVDS_B17_P	2A	AE17	LVDS2A_17p
39	LVDSIO_1V8	B2A_LVDS_B9_N	2A	AF14	LVDS2A_9n
40	LVDSIO_1V8	CLK2A_N	2A	AG15	LVDS2A_12n/CLK_2A_1n
41	LVDSIO_1V8	B2A_LVDS_B9_P	2A	AF13	LVDS2A_9p
42	LVDSIO_1V8	CLK2A_P	2A	AG14	LVDS2A_12n/CLK_2A_1p
43	POWER	GND	-	-	
44	POWER	GND	-	-	
45	LVDSIO_1V8	B2A_LVDS_B6_N	2A	AD14	LVDS2A_6n
46	LVDSIO_1V8	B2A_LVDS_B11_N	2A	AF16	LVDS2A_11n
47	LVDSIO_1V8	B2A_LVDS_B6_P	2A	AD13	LVDS2A_6p
48	LVDSIO_1V8	B2A_LVDS_B11_P	2A	AG16	LVDS2A_11p
49	POWER	GND	-	-	
50	POWER	GND	-	-	
51	LVDSIO_1V8	B2A_LVDS_B1_P	2A	AE11	LVDS2A_1p
52	LVDSIO_1V8	B2A_LVDS_B21_P	2A	AC15	LVDS2A_21p
53	LVDSIO_1V8	B2A_LVDS_B1_N	2A	AE10	LVDS2A_1n
54	LVDSIO_1V8	B2A_LVDS_B21_N	2A	AB15	LVDS2A_21n
55	LVDSIO_1V8	B2A_LVDS_B20_P	2A	AB14	LVDS2A_20p
56	LVDSIO_1V8	B2A_LVDS_B4_N	2A	AD12	LVDS2A_4n
57	LVDSIO_1V8	B2A_LVDS_B20_N	2A	AA14	LVDS2A_20n
58	LVDSIO_1V8	B2A_LVDS_B4_P	2A	AE12	LVDS2A_4p
59	LVDSIO_1V8	B2A_LVDS_B23_P	2A	AA12	DEV_OE/LVDS2A_23p
60	LVDSIO_1V8	B2A_LVDS_B24_P	2A	AC12	DEV_CLRn/LVDS2A_24p
61	LVDSIO_1V8	B2A_LVDS_B23_N	2A	AA13	INIT_DONE/LVDS2A_23n
62	LVDSIO_1V8	B2A_LVDS_B24_N	2A	AC11	CRC_ERROR/LVDS2A_24n
63	LVDSIO_1V8	B2A_LVDS_B14_N	2A	AD19	LVDS2A_18n
64	LVDSIO_1V8	B2A_LVDS_B22_P	2A	AC13	LVDS2A_22p
65	LVDSIO_1V8	B2A_LVDS_B14_P	2A	AD20	LVDS2A_18p
66	LVDSIO_1V8	B2A_LVDS_B22_N	2A	AB13	LVDS2A_22n
67	POWER	GND	-	-	
68	POWER	GND	-	-	
69	SHAREDIO_1V8	RGMII1_TX_CTL	2L	G23	CLK_2L_1n,GPIO1_IO1,NAND_ADQ1,UART0_RTS_N,EMAC1_TX_CTL,SPIM1_MOSI
70	SHAREDIO_1V8	RGMII1_RX_CLK	2L	F21	RZQ_2L,GPIO1_IO2,NAND_WE_N,UART0_TX,EMAC1_RX_CLK,SPIM1_MISO,I2C0_SDA
71	SHAREDIO_1V8	RGMII1_TX_CLK	2L	F23	CLK_2L_1p,GPIO1_IO0,NAND_ADQ0,UART0_CTS_N,EMAC1_TX_CLK,SPIM1_CLK
72	SHAREDIO_1V8	RGMII1_RX_CTL	2L	G21	GPIO1_IO3,NAND_RE_N,UART0_RX,EMAC1_RX_CTL,SPIM1_SS0_N,I2C0_SCL
73	SHAREDIO_1V8	RGMII1_TXD3	2L	E23	GPIO1_IO9,NAND_ADQ5,EMAC1_TXD3,SPIS0_MOSI,EMAC2_MDC,I2

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Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Notes / Alternate HPS Mux functions
					C_EMAC2_SCL
74	SHAREDIO_1V8	RGMII1_RXD0	2L	E22	GPIO1_IO6,NAND_ADQ3,UART1_TX,EMAC1_RXD0,SPIS1_SS0_N,I2C1_SDA
75	SHAREDIO_1V8	RGMII1_TXD2	2L	D23	GPIO1_IO8,NAND_ADQ4,EMAC1_TXD2,SPIS0_CLK,EMAC2_MDIO,I2C_EMAC2_SDA
76	SHAREDIO_1V8	RGMII1_RXD1	2L	F22	GPIO1_IO7,NAND_CLE,UART1_RX,EMAC1_RXD1,SPIS1_MISO,I2C1_SCL
77	SHAREDIO_1V8	RGMII1_TXD1	2L	C22	PLL_2L_CLKOUT1n,GPIO1_IO5,NAND_ADQ2,UART1_RTS_N,EMAC1_TXD1,SPIS1_MOSI
78	SHAREDIO_1V8	RGMII1_RXD2	2L	D22	GPIO1_IO10,NAND_ADQ6,EMAC1_RXD2,SPIS0_SS0_N,EMAC0_MDIO,I2C_EMAC0_SDA
79	SHAREDIO_1V8	RGMII1_TXD0	2L	C23	PLL_2L_CLKOUT1p,PLL_2L_CLKOUT1,PLL_2L_FB1,GPIO1_IO4,NAND_WP_N,UART1_CTS_N,EMAC1_TXD0,SPIM1_SS1_N,SPIS1_CLK
80	SHAREDIO_1V8	RGMII1_RXD3	2L	E21	GPIO1_IO11,NAND_ADQ7,EMAC1_RXD3,SPIS0_MISO,EMAC0_MDC,I2C_EMAC0_SCL
81	POWER	GND	-	-	
82	FFIO	HPS_RST_N	HPS	K11	HPS_nPOR
83	HPSIO_1V8	RGMII1_MDC	HPS	F16	GPIO2_IO8,NAND_RB,UART1_TX,SDMMC_DATA4,SPIM0_MOSI,EMAC1_MDIO,I2C_EMAC1_SDA
84	HPSIO_1V8	RGMII1_MDIO	HPS	H15	GPIO2_IO9,NAND_CE_N,UART1_RTS_N,SDMMC_DATA5,SPIM0_MISO,EMAC1_MDC,I2C_EMAC1_SCL
85	FFIO_3V3	GPIO1_IO23_3V3	2L	H16	GPIO1_IO23,NAND_ADQ15,Trace_D3,EMAC2_RXD3,SPIM0_SS0_N,SPIS1_MISO,EMAC0_MDC,I2C_EMAC0_SCL
86	FFIO	USB1_VBUS	-	-	
87	POWER	+3VBAT	-	-	
88	FFIO	USB1_ID	-	-	
89	POWER	GND	-	-	
90	POWER	GND	-	-	
91	XCVR_RX	GXB_RX_3_P	1C	Y26	GXBL1C_RX_CH3p,GXBL1C_REFCLK3p
92	FFIO	USB1_D_N	-	-	
93	XCVR_RX	GXB_RX_3_N	1C	Y25	GXBL1C_RX_CH3n,GXBL1C_REFCLK3n
94	FFIO	USB1_D_P	-	-	
95	POWER	GND	-	-	
96	POWER	GND	-	-	
97	XCVR_RX	GXB_RX_2_P	1C	AB26	GXBL1C_RX_CH2p,GXBL1C_REFCLK2p
98	XCVR_TX	GXB_TX_3_N	1C	AA27	GXBL1C_TX_CH3n
99	XCVR_RX	GXB_RX_2_N	1C	AB25	GXBL1C_RX_CH2n,GXBL1C_REFCLK2n
100	XCVR_TX	GXB_TX_3_P	1C	AA28	GXBL1C_TX_CH3p
101	POWER	GND	-	-	
102	POWER	GND	-	-	
103	XCVR_RX	GXB_RX_1_P	1C	AD26	GXBL1C_RX_CH1p,GXBL1C_REFCLK1p
104	XCVR_TX	GXB_TX_2_N	1C	AC27	GXBL1C_TX_CH2n
105	XCVR_RX	GXB_RX_1_N	1C	AD25	GXBL1C_RX_CH1n,GXBL1C_REFCLK1n
106	XCVR_TX	GXB_TX_2_P	1C	AC28	GXBL1C_TX_CH2p
107	POWER	GND	-	-	
108	POWER	GND	-	-	
109	XCVR_RX	GXB_RX_0_P	1C	AF26	GXBL1C_RX_CH0p,GXBL1C_REFCLK0p
110	XCVR_TX	GXB_TX_1_N	1C	AE27	GXBL1C_TX_CH1n
111	XCVR_RX	GXB_RX_0_N	1C	AF25	GXBL1C_RX_CH0n,GXBL1C_REFCLK0n
112	XCVR_TX	GXB_TX_1_P	1C	AE28	GXBL1C_TX_CH1p
113	POWER	GND	-	-	
114	POWER	GND	-	-	
115	XCVR_REFCLK	GXB_REFCLK1_P	-	-	
116	XCVR_TX	GXB_TX_0_N	1C	AG27	GXBL1C_TX_CH0n
117	XCVR_REFCLK	GXB_REFCLK1_N	-	-	
118	XCVR_TX	GXB_TX_0_P	1C	AG28	GXBL1C_TX_CH0p
119	POWER	GND	-	-	
120	POWER	GND	-	-	

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Bottom Side Interface Description (J100)

One of two primary interface connectors for the MitySOM-A10S-DSC is the 120-pin board to board interface, J100. The connector used for J100 is a Samtech ERM8-060-05.0-S-DV-TR, which mates with Samtech ERF8-060-05.0-S-DV-TR (the mating height may be taller if desired). Table 7 contains a summary of the MitySOM-A10S-DSC Bottom Side Interface pin-mapping.

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Table 7: MitySOM-A10S-DSC Bottom Side Connector Pin-Out (J100)

Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Notes
1	-	NC	-	-	
2	POWER	GND	-	-	
3	IO_1V8	B2A_LVDS_B15_N	2A	AC17	LVDS2A_15n/PLL_2A_CLKOUT0n
4	LVDSIO_1V8	B3B_LVDS_B14_N	3B	G1	LVDS3B_14n
5	LVDSIO_1V8	B3B_LVDS_B10_P	3B	H2	PLL_3B_CLKOUT1P/LVDS3B_10p
6	LVDSIO_1V8	B3B_LVDS_B14_P	3B	H1	LVDS3B_14p
7	LVDSIO_1V8	B3B_LVDS_B10_N	3B	J3	PLL_3B_CLKOUT1n/LVDS3B_10n
8	POWER	GND	-	-	
9	LVDSIO_1V8	B3B_LVDS_B15_N	3B	P2	LVDS3B_15n/PLL_3B_ClkOUT0n
10	LVDSIO_1V8	B3B_LVDS_B9_N	3B	N3	LVDS3B_9n
11	LVDSIO_1V8	B3B_LVDS_B15_P	3B	R2	LVDS3B_15p/PLL_3B_ClkOUT0p
12	LVDSIO_1V8	B3B_LVDS_B9_P	3B	N2	LVDS3B_9p
13	POWER	GND	-	-	
14	POWER	GND	-	-	
15	LVDSIO_1V8	B3B_LVDS_B17_N	3B	K1	LVDS3B_17n
16	LVDSIO_1V8	B3B_LVDS_B11_N	3B	J2	LVDS3B_11n
17	LVDSIO_1V8	B3B_LVDS_B17_P	3B	L1	LVDS3B_17p
18	LVDSIO_1V8	B3B_LVDS_B11_P	3B	K2	LVDS3B_11p/RZQ_3B
19	LVDSIO_1V8	B3B_LVDS_B18_N	3B	R1	LVDS3B_18n
20	LVDSIO_1V8	B3B_LVDS_B7_P	3B	M3	LVDS3B_7p
21	LVDSIO_1V8	B3B_LVDS_B18_P	3B	T1	LVDS3B_18p
22	LVDSIO_1V8	B3B_LVDS_B7_N	3B	M4	LVDS3B_7n
23	LVDSIO_1V8	B3B_LVDS_B19_N	3B	U4	LVDS3B_19n
24	LVDSIO_1V8	B3B_LVDS_B16_P	3B	T2	LVDS3B_16p
25	LVDSIO_1V8	B3B_LVDS_B19_P	3B	U3	LVDS3B_19p
26	LVDSIO_1V8	B3B_LVDS_B16_N	3B	T3	LVDS3B_16n
27	LVDSIO_1V8	B3B_LVDS_B20_N	3B	U1	LVDS3B_20N
28	LVDSIO_1V8	B3B_LVDS_B5_P	3B	T4	LVDS3B_5p
29	LVDSIO_1V8	B3B_LVDS_B20_P	3B	V1	LVDS3B_20p
30	LVDSIO_1V8	B3B_LVDS_B5_N	3B	U5	LVDS3B_5n
31	POWER	GND	-	-	
32	POWER	GND	-	-	
33	LVDSIO_1V8	CLK3B_P	3B	L2	LVDS3B_12p/CLK_3B_1p
34	LVDSIO_1V8	B3B_LVDS_B4_P	3B	R5	LVDS3B_4n
35	LVDSIO_1V8	CLK3B_N	3B	L3	LVDS3B_12n/CLK_3B_1n
36	LVDSIO_1V8	B3B_LVDS_B4_N	3B	R4	LVDS3B_4p
37	POWER	GND	-	-	
38	LVDSIO_1V8	B3B_LVDS_B3_P	3B	T6	LVDS3B_3p
39	LVDSIO_1V8	B3B_LVDS_B21_N	3B	U6	LVDS3B_21p
40	LVDSIO_1V8	B3B_LVDS_B3_N	3B	T7	LVDS3B_3n
41	LVDSIO_1V8	B3B_LVDS_B21_P	3B	V7	LVDS3B_21n
42	LVDSIO_1V8	B3B_LVDS_B2_N	3B	T9	LVDS3B_2n
43	LVDSIO_1V8	B3B_LVDS_B22_P	3B	V5	LVDS3B_22p
44	LVDSIO_1V8	B3B_LVDS_B2_P	3B	T8	LVDS3B_2p
45	LVDSIO_1V8	B3B_LVDS_B22_N	3B	V6	LVDS3B_2n
46	LVDSIO_1V8	B3B_LVDS_B8_N	3B	L4	LVDS3B_8n
47	IO_1V8	B3B_LVDS_B1_P	3B	P3	LVDS3B_1p
48	LVDSIO_1V8	B3B_LVDS_B8_P	3B	K4	LVDS3B_8p
49	POWER	GND	-	-	
50	POWER	GND	-	-	
51	SHAREDIO_1V8	GPIO1_IO14	2L	G18	GPIO1_IO14,NAND_CE_N,UART1_TX,EMAC2_RX-CLK,SDMMC_CCLK
52	LVDSIO_1V8	B3B_LVDS_B23_N	3B	V2	LVDS3B_23n
53	POWER	GND	-	-	
54	LVDSIO_1V8	B3B_LVDS_B23_P	3B	W2	LVDS3B_23p
55	LVDSIO_1V8	B3B_LVDS_B6_P	3B	U8	LVDS3B_6p
56	LVDSIO_1V8	B3B_LVDS_B24_N	3B	V3	LVDS3B_24n
57	LVDSIO_1V8	B3B_LVDS_B6_N	3B	V8	LVDS3B_6n
58	LVDSIO_1V8	B3B_LVDS_B24_P	3B	W3	LVDS3B_24p

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Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Notes
59	POWER	GND	-	-	
60	LVDSIO_1V8	B3A_LVDS_B16_N	3A	AD2	LVDS3A_16n
61	FFIO_3V3	I2C1_SDA	2L	C17	+3.3V Level Translated
62	LVDSIO_1V8	B3A_LVDS_B16_P	3A	AE2	LVDS3A_16p
63	FFIO_3V3	I2C1_SCL	2L	C16	+3.3V Level Translated
64	LVDSIO_1V8	B3A_LVDS_B17_N	3A	AF1	LVDS3A_17n
65	POWER	GND	-	-	
66	LVDSIO_1V8	B3A_LVDS_B17_P	3A	AG1	LVDS3A_17p
67	LVDSIO_1V8	REF_CLK_N	3B	M1	LVDS3B_13n/CLK_3B_0n
68	LVDSIO_1V8	B3A_LVDS_B18_N	3A	AF3	LVDS3A_18n
69	LVDSIO_1V8	REF_CLK_P	3B	N1	LVDS3B_13p/CLK_3B_0p
70	LVDSIO_1V8	B3A_LVDS_B18_P	3A	AG3	LVDS3A_18p
71	POWER	GND	-	-	
72	POWER	GND	-	-	
73	IO_1V8	B3B_LVDS_B1_N	3B	P4	LVDS3B_1n
74	LVDSIO_1V8	B3A_LVDS_B1_P	3A	W4	LVDS3A_1p
75	LVDSIO_1V8	B3A_LVDS_B15_P	3A	AC1	PLL_3A_CLKOUT0p/LVDS3A_15p
76	LVDSIO_1V8	B3A_LVDS_B1_N	3A	Y4	LVDS3A_1n
77	LVDSIO_1V8	B3A_LVDS_B15_N	3A	AC2	PLL_3A_CLKOUT0n/LVDS3A_15n
78	LVDSIO_1V8	B3A_LVDS_B2_P	3A	W8	LVDS3A_2p
79	LVDSIO_1V8	B3A_LVDS_B14_P	3A	AE1	LVDS3A_14p
80	LVDSIO_1V8	B3A_LVDS_B2_N	3A	W7	LVDS3A_2n
81	LVDSIO_1V8	B3A_LVDS_B14_N	3A	AF2	LVDS3A_14n
82	LVDSIO_1V8	B3A_LVDS_B3_P	3A	Y7	LVDS3A_3p
83	POWER	GND	-	-	
84	LVDSIO_1V8	B3A_LVDS_B3_N	3A	Y6	LVDS3A_3n
85	LVDSIO_1V8	CLK3A_N	3A	AA7	LVDS3A_12n/CLK_3A_1n
86	LVDSIO_1V8	B3A_LVDS_B4_P	3A	W5	LVDS3A_4p
87	LVDSIO_1V8	CLK3A_P	3A	AA6	LVDS3A_12p/CLK_3A_1p
88	LVDSIO_1V8	B3A_LVDS_B4_N	3A	Y5	LVDS3A_4n
89	POWER	GND	-	-	
90	POWER	GND	-	-	
91	LVDSIO_1V8	B3A_LVDS_B7_N	3A	AB4	LVDS3A_7n
92	LVDSIO_1V8	B3A_LVDS_B5_N	3A	Y2	LVDS3A_5n
93	LVDSIO_1V8	B3A_LVDS_B7_P	3A	AC5	LVDS3A_7p
94	LVDSIO_1V8	B3A_LVDS_B5_P	3A	Y1	LVDS3A_5p
95	LVDSIO_1V8	B3A_LVDS_B20_N	3A	AD4	LVDS3A_20n
96	LVDSIO_1V8	B3A_LVDS_B6_P	3A	AA9	LVDS3A_6p
97	LVDSIO_1V8	B3A_LVDS_B20_P	3A	AE4	LVDS3A_20p
98	LVDSIO_1V8	B3A_LVDS_B6_N	3A	AA8	LVDS3A_6n
99	LVDSIO_1V8	B3A_LVDS_B24_N	3A	AD5	LVDS3A_24n
100	LVDSIO_1V8	B3A_LVDS_B8_N	3A	AA1	LVDS3A_8n
101	LVDSIO_1V8	B3A_LVDS_B24_P	3A	AE5	LVDS3A_24p
102	LVDSIO_1V8	B3A_LVDS_B8_P	3A	AB1	LVDS3A_8p
103	LVDSIO_1V8	B3A_LVDS_B22_N	3A	AE6	LVDS3A_22n
104	LVDSIO_1V8	B3A_LVDS_B10_P	3A	AA2	LVDS3A_10p
105	LVDSIO_1V8	B3A_LVDS_B22_P	3A	AF6	LVDS3A_22p
106	LVDSIO_1V8	B3A_LVDS_B10_N	3A	AB3	LVDS3A_10n
107	POWER	GND	-	-	
108	POWER	GND	-	-	
109	POWER	SPARE_V1	-	-	
110	POWER	+5VIN	-	-	
111	POWER	SPARE_V0	-	-	
112	POWER	+5VIN	-	-	
113	POWER	+1V8	-	-	
114	POWER	GND	-	-	
115	POWER	+5.0V	-	-	
116	POWER	+2V5	-	-	
117	POWER	+3V3	-	-	
118	POWER	+12V	-	-	

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Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Notes
119	POWER	GND	-	-	
120	POWER	GND	-	-	

Notes:
1) For more information about pin definitions and pin connection guidelines please refer to the Arria 10 Device Family Pin Connection Guidelines.

Top or Bottom Side Transceiver Expansion Interface (J500 or J600)
MitySOM-A10S-DSC includes a 60-pin board to board interface] that may be populated on the Top Side or the Bottom Side or not at all (determined at time of order). The connector for the Top Side Option, J500, is a Hirose FX10A-144P-SV1(71). The connector for the Bottom Side Option, J600, is a Hirose FX10A-144P-SV1(71). Table 7 contains a summary of the MitySOM-A10S-DSC Transceiver Expansion Interface mapping. Note: legacy versions of the MitySOM-A10S-DSC used a different connector for J500/J600. Customers requiring information for these boards should contact Critical Link for mechanical and pin out details.

Table 8: MitySOM-A10S-DSC Bottom Side Connector Pin-Out (J500 / J600)

J600	J500	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Notes
1	2	POWER	GND			
2	1	POWER	GND	-	-	
3	4	POWER	GND	-	-	
4	3	XCVR_REFCLK	REFCLK_PCIE_N	1D	N23	
5	6	POWER	GND	-	-	
6	5	XCVR_REFCLK	REFCLK_PCIE_P	1D	N24	
7	8	POWER	GND	-	-	
8	7	POWER	GND	-	-	
9	10	POWER	GND	-	-	
10	9	POWER	GND	-	-	
11	12	POWER	GND	-	-	
12	11	CLKOUT	GXBR_REFCLK1_N	-	-	CLK2 Output of U14 (PLL)
13	14	POWER	GND	-	-	
14	13	CLKOUT	GXBR_REFCLK1_P	-	-	CLK2 Output of U14 (PLL)
15	16	POWER	GND	-	-	
16	15	POWER	GND	-	-	
17	18	POWER	GND	-	-	
18	17	POWER	GND	-	-	
19	20	POWER	GND	-	-	
20	19	XCVR_RX	GXBR_RX_7_P	1D	D26	
21	22	POWER	GND	-	-	
22	21	XCVR_RX	GXBR_RX_7_N	1D	D25	
23	24	POWER	GND	-	-	
24	23	POWER	GND	-	-	
25	26	FFIO_3V3	I2C1_SDA	2L	C17	+3.3V Level Translated
26	25	POWER	GND	-	-	
27	28	FFIO_3V3	I2C1_SCL	2L	C16	+3.3V Level Translated
28	27	XCVR_TX	GXBR_TX_7_P	1D	E28	
29	30	POWER	GND	-	-	
30	29	XCVR_TX	GXBR_TX_7_N	1D	E27	
31	32	POWER	GND	-	-	

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J600	J500	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Notes
32	31	POWER	GND	-	-	
33	34	POWER	GND	-	-	
34	33	POWER	GND	-	-	
35	36	POWER	GND	-	-	
36	35	XCVR_RX	GXBR_RX_6_P	1D	F26	
37	38	POWER	GND	-	-	
38	37	XCVR_RX	GXBR_RX_6_N	1D	F25	
39	40	POWER	GND	-	-	
40	39	POWER	GND	-	-	
41	42	POWER	GND	-	-	
42	41	POWER	GND	-	-	
43	44	POWER	GND	-	-	
44	43	XCVR_TX	GXBR_TX_6_P	1D	G28	
45	46	POWER	GND	-	-	
46	45	XCVR_TX	GXBR_TX_6_N	1D	G27	
47	48	POWER	GND	-	-	
48	47	POWER	GND	-	-	
49	50	POWER	GND	-	-	
50	49	POWER	GND	-	-	
51	52	POWER	GND	-	-	
52	51	XCVR_RX	GXBR_RX_5_P	1D	H26	
53	54	POWER	GND	-	-	
54	53	XCVR_RX	GXBR_RX_5_N	1D	H25	
55	56	SHAREDIO_1V8	GPIO1_IO12	2L	G20	GPIO1_IO12,NAND_ALE,EMAC2_TX_CLK,SDMMC_DATA0,I2C1_SDA
56	55	POWER	GND	-	-	
57	58	SHAREDIO_1V8	GPIO1_IO19	2L	K17	GPIO1_IO19,NAND_ADQ11,Trace_CLK,EMAC2_RXD1,SDMMC_DATA5,SPIM0_SS0_N,EMAC1_MDC,I2C_EMAC1_SCL
58	57	POWER	GND	-	-	
59	60	SHAREDIO_1V8	GPIO1_IO21	2L	J19	GPIO1_IO21,NAND_ADQ13,Trace_D1,EMAC2_TXD3,SDMMC_DATA7,SPIM0_MOSI,SPIS1_MOSI,I2C_EMAC2_SCL
60	59	XCVR_TX	GXBR_TX_5_P	1D	J28	
61	62	SHAREDIO_1V8	GPIO1_IO18	2L	J17	GPIO1_IO18,NAND_ADQ10,EMAC2_RXD0,SDMMC_DATA4,SPIM0_MISO,EMAC1_MDIO,I2C_EMAC1_SDA
62	61	XCVR_TX	GXBR_TX_5_N	1D	J27	
63	64	SHAREDIO_1V8	GPIO1_IO20	2L	J18	GPIO1_IO20,NAND_ADQ12,Trace_D0,EMAC2_TXD2,SDMMC_DATA6,SPIM0_CLK,SPIS1_CLK,I2C_EMAC2_SDA
64	63	POWER	GND	-	-	
65	66	SHAREDIO_1V8	GPIO1_IO22	2L	H17	GPIO1_IO22,NAND_ADQ14,Trace_D2,EMAC2_RXD2,SPIM0_MISO,SPIS1_SS0_N,EMAC0_MDIO,I2C_EMAC0_SDA
66	65	POWER	GND	-	-	
67	68	POWER	GND	-	-	
68	67	XCVR_RX	GXBR_RX_4_P	1D	K26	
69	70	SHAREDIO_1V8	GPIO1_IO15	2L	H18	GPIO1_IO15,UART1_RX,Trace_CLK,EMAC2_RX_CTL,SDMMC_DATA1
70	69	XCVR_RX	GXBR_RX_4_N	1D	K25	
71	72	SHAREDIO_1V8	GPIO1_IO16	2L	F17	GPIO1_IO16,NAND_ADQ8,UART1_CTS_N,QSPI_SS2,EMAC2_TXD0,SDMMC_DATA2
72	71	POWER	GND	-	-	
73	74	SHAREDIO_1V8	GPIO1_IO17	2L	F18	GPIO1_IO17,NAND_ADQ9,UART1_RTS_N,QSPI_SS3,EMAC2_TXD1,SDMMC_DATA3,SPIM0_SS1_N
74	73	POWER	GND	-	-	
75	76	SHAREDIO_1V8	GPIO0_IO7	2L	F19	GPIO0_IO7,NAND_CLE,UART1_RX,USB0_DATA3,SDMMC_DATA5,SPIM0_SS0_N,EMAC2_MDC,I2C_EMAC2_SCL
76	75	XCVR_TX	GXBR_TX_4_P	1D	L28	
77	78	SHAREDIO_1V8	GPIO0_IO1	2L	D17	GPIO0_IO1,NAND_ADQ1,UART0_RTS_N,USB0_STP,SDMMC_CMD,SPIM1_SS1_N,SPIS0_MOSI
78	77	XCVR_TX	GXBR_TX_4_N	1D	L27	
79	80	POWER	GND	-	-	
80	79	POWER	GND	-	-	

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J600	J500	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Notes
81	82	SHAREDIO_1V8	GPIO0_IO0	2L	C18	GPIO0_IO0,NAND_ADQ0,UART0_CTS_N,USB0_CLK,SDMMC_DATA0,SPIM0_SS1_N,SPIS0_CLK
82	81	POWER	GND	-	-	
83	84	SHAREDIO_1V8	GPIO0_IO10	2L	D10	GPIO0_IO10,NAND_ADQ6,USB0_DATA6,SPIM1_MISO,SPIS1_SS0_N,EMAC0_MDIO,I2C_EMAC0_SDA
84	83	XCVR_RX	GXBR_RX_3_P	1D	M26	
85	86	SHAREDIO_1V8	GPIO0_IO11	2L	D18	GPIO0_IO11,NAND_ADQ7,USB0_DATA7,SPIM1_SS0_N,SPIS1_MISO,EMAC0_MDC,I2C_EMAC0_SCL
86	85	XCVR_RX	GXBR_RX_3_N	1D	M25	
87	88	SHAREDIO_1V8	GPIO0_IO6	2L	E19	GPIO0_IO6,NAND_ADQ3,UART1_TX,USB0_DATA2,SDMMC_DATA4,SPIM0_MISO,EMAC2_MDIO,I2C_EMAC2_SDA
88	87	POWER	GND	-	-	
89	90	SHAREDIO_1V8	GPIO1_IO13	2L	G19	GPIO1_IO13,NAND_RB,EMAC2_TX_CTL,SDMMC_CMD,I2C1_SCL
90	89	POWER	GND	-	-	
91	92	SHAREDIO_1V8	nPERSTL0_LVDS2A_19p	2A	AB11	nPERSTL0/LVDS2A_19p
92	91	XCVR_TX	GXBR_TX_3_P	1D	N28	
93	94	IO_1V8	B2A_LVDS_B15_P	2A	AC16	LVDS2A_15p/PLL_2A_CLKOUT0p
94	93	XCVR_TX	GXBR_TX_3_N	1D	N27	
95	96	POWER	GND	-	-	
96	95	POWER	GND	-	-	
97	98	POWER	GND	-	-	
98	97	POWER	GND	-	-	
99	100	LVDSIO_1V8	B3A_LVDS_B9_P	3A	AB6	LVDS3A_9p
100	99	XCVR_RX	GXBR_RX_2_P	1D	P26	
101	102	LVDSIO_1V8	B3A_LVDS_B9_N	3A	AB5	LVDS3A_9n
102	101	XCVR_RX	GXBR_RX_2_N	1D	P25	
103	104	POWER	GND	-	-	
104	103	POWER	GND	-	-	
105	106	POWER	GND	-	-	
106	105	POWER	GND	-	-	
107	108	LVDSIO_1V8	B3A_LVDS_B21_N	3A	AC7	LVDS3A_21n
108	107	XCVR_TX	GXBR_TX_2_P	1D	R28	
109	110	LVDSIO_1V8	B3A_LVDS_B21_P	3A	AC6	LVDS3A_21p
110	109	XCVR_TX	GXBR_TX_2_N	1D	R27	
111	112	POWER	GND	-	-	
112	111	POWER	GND	-	-	
113	114	POWER	GND	-	-	
114	113	POWER	GND	-	-	
115	116	LVDSIO_1V8	B3A_LVDS_B11_N	3A	AA4	LVDS3A_11n
116	115	XCVR_RX	GXBR_RX_1_P	1C	T26	
117	118	LVDSIO_1V8	B3A_LVDS_B11_P	3A	AA3	LVDS3A_11p/RZQ_3A
118	117	XCVR_RX	GXBR_RX_1_N	1C	T25	
119	120	POWER	GND	-	-	
120	119	POWER	GND	-	-	
121	122	POWER	GND	-	-	
122	121	POWER	GND	-	-	
123	124	LVDSIO_1V8	B3A_LVDS_B13_N	3A	AC3	LVDS3A_13n/CLK_3A_0n
124	123	XCVR_TX	GXBR_TX_1_P	1C	U28	
125	126	LVDSIO_1V8	B3A_LVDS_B13_P	3A	AD3	LVDS3A_13p/CLK_3A_0p
126	125	XCVR_TX	GXBR_TX_1_N	1C	U27	

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J600	J500	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Notes
127	128	POWER	GND	-	-	
128	127	POWER	GND	-	-	
129	130	POWER	GND	-	-	
130	129	POWER	GND	-	-	
131	132	LVDSIO_1V8	B3A_LVDS_B23_P	3A	AG4	LVDS3A_23p
132	131	XCVR_RX	GXBR_RX_0_P	1C	V26	
133	134	LVDSIO_1V8	B3A_LVDS_B23_N	3A	AF4	LVDS3A_23n
134	133	XCVR_RX	GXBR_RX_0_N	1C	V25	
135	136	POWER	GND	-	-	
136	135	POWER	GND	-	-	
137	138	POWER	GND	-	-	
138	137	POWER	GND	-	-	
139	140	LVDSIO_1V8	B3A_LVDS_19_N	3A	AH3	LVDS3A_19n
140	139	XCVR_TX	GXBR_TX_0_P	1C	W28	
141	142	LVDSIO_1V8	B3A_LVDS_B19_P	3A	AH2	LVDS3A_19p
142	141	XCVR_TX	GXBR_TX_0_N	1C	W27	
143	144	POWER	GND	-	-	
144	143	POWER	GND	-	-	

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ELECTRICAL CHARACTERISTICS

Table 9: Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
+5VIN	Voltage supply, volt input.		4.8	5.0	5.15	Volts
$\mathbf{I_{5.0}}$	Quiescent Current draw	5.0 volt input, 1033 MHz DDR4, no FPGA fabric, Linux prompt		2000		mA
$\mathbf{I_{5.0\text{-}max}}$	Max current draw[1]	5.0 volt input		3500	6000	mA
+3.3V	Voltage Supply, volt output.			3.3		Volts
$\mathbf{I_{3.3\text{-}max}}$	Max current draw	3.3 volt output			100	mA
+2.5V	Voltage Supply, volt output.			2.5		Volts
$\mathbf{I_{3.3\text{-}max}}$	Max current draw	2.5 volt output			TBS	mA
+1.8V	Voltage Supply, volt output.			1.8		Volts
$\mathbf{I_{3.3\text{-}max}}$	Max current draw	1.8 volt output			TBS	mA
Notes	1. Power utilization of the MitySOM-A10S-DSC is heavily dependent on end-user application. Major factors include: ARM CPU PLL configuration, CPU Utilization, and external DDR4 RAM utilization. Users should refer to Intel's power estimator tools for a given design to confirm device utilization.					

ORDERING INFORMATION

The following table lists the module configurations. Items shown in **bold** are standard configurations. For shipping status, availability, and lead time of these configurations, or to inquire about a development kit for these products, contact Critical Link via email at info@criticallink.com.

Table 10: Standard Model Numbers

Model / Part Number	FPGA KLE	X8 XCVR Connector Option	HPS RAM (32-bit)	FPGA RAM (16-bit)	Component Temperature Ratings
A10S-P7-A5E-RI-TA	160	None	1 GB	N / A	-40ºC to 85º C
A10S-P8-A5E-RC-TA	**270**	**None**	**4 GB**	**2 GB**	**0ºC to 70º C**
A10S-P8-A5E-RI-TA	270	Top J500	4 GB	2 GB	-40ºC to 85º C
A10S-P9-A5E-RC-TA	480	Top J500	4 GB	2 GB	0ºC to 70º C
A10S-P9-A5E-RI-TA	480	Top J500	4 GB	2 GB	-40ºC to 85º C

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MECHANICAL INTERFACE

A top view mechanical outline of the MitySOM-A10S-DSC is illustrated in Figure 2, which includes placement positions of the J200 and J500 interface connectors. A view of locations of the bottom side connectors is shown in Figure 3, showing the J100 and J600 connector positions. Note that the view in Figure 3 is from the top side, and the connectors are on the back side of the view. All dimensions are in mils.

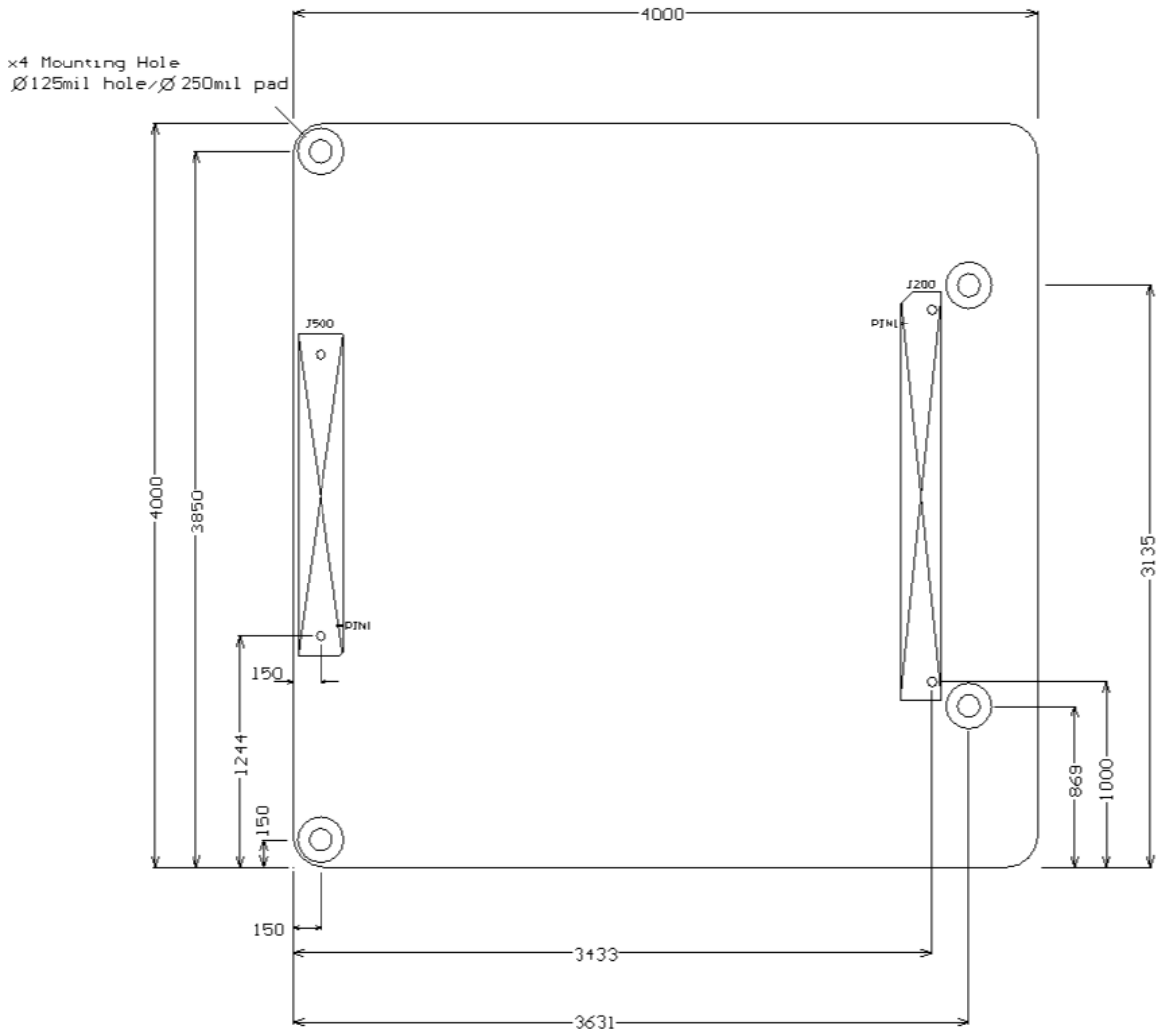

Figure 2 MitySOM-A10S-DSC Mechanical Outline, Top Side, View from top

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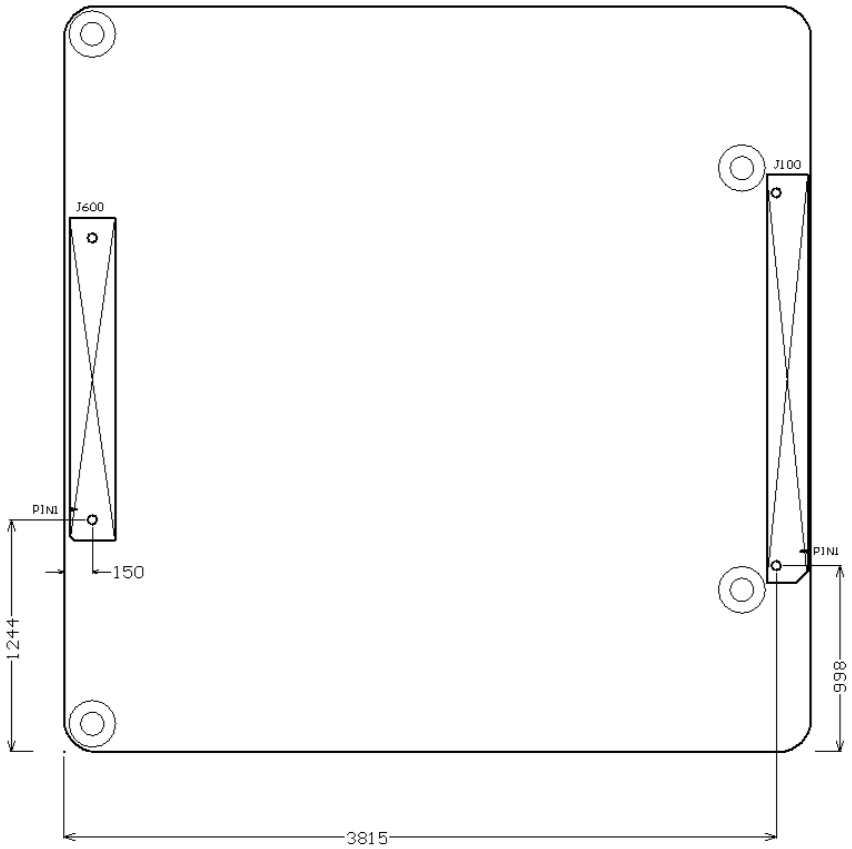

Figure 3 MitySOM-A10S-DSC Mechanical Outline, Bottom Side, View from Top

REVISION HISTORY

Revision	Date	Change Description
A	November 23, 2017	Preliminary Release for early adopters
B	February 5, 2018	Updated Block diagrams and connector tables.
C	June 4, 2018	Updated based on production release. Added description for JTAG headers, clarified connectors for J100, J200, and J500/J600. Corrected pin assignments errors. Made the A10S-P8-A5E-RC-TA the standard option.
D	July 17, 2023	Updated J500 and J600 connectors to floating Hirose FX10A-144P-SV1(71) style. Update pin tables and Figures 1, 2 and 3. Remove references to Altera, just Intel.

FOOTNOTES

[1] https://www.intel.com/content/www/us/en/support/programmable/support-resources/power/a10-power-estimator-download.html

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