FEATURES

- Intel/Altera Cyclone V SX Processor
  - Dual ARM Cortex- A9 MPU
  - 925MHz Max clock speed
  - Dual NEON SIMD Coprocessors
  - 32 KB L1 Program Cache (per core)
  - 32 KB L1 Data Cache (per core)
  - 512 KB L2 Cache (shared)
  - 64 KB on-chip RAM
  - ECC Support
  - Up to 112 User FPGA I/O Pins
  - 28 CPU I/O Pins
  - 4 High Speed 3.125 Gbps transceivers

- **Cyclone V Processor Choices**
  - Cyclone V SX (3.125 Gbps transceivers)

- **Memory**
  - Up To 2GB DDR3 CPU RAM x32 bits + ECC
  - Up To 32MB QPSI NOR FLASH

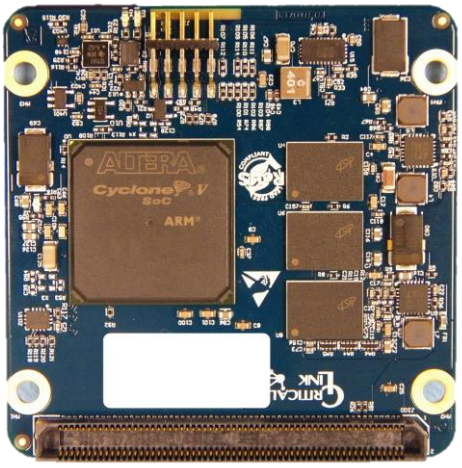
- Integrated Power Management
- JTAG connector on-module
- On Board USB 2.0 PHY
- On Board MicroSD Card Interface

- **FPGA Fabric**
  - Up To 110K Logic Elements (LE)
  - 460Mhz Global Clock
  - Up To 5.1Mb M10K Memory
  - Up To 621Kb MLAB Memory
  - Up To 112 DSP Blocks
  - Up To 6 FPGA PLLs
  - Fractional PLL Outputs on each PLL

- Low Power Serial Transceivers
  - 3.125Gbps Transceivers
  - PCIe Hard IP Block (Gen1.1 x1 or x4)

- Power, Reset and Clock Management

- **Mechanical**
  - 63.5mm (2.5") x 63.5mm (2.5") size
  - Dual Samtec 120 pin board to board connectors on top and bottom for stacking form factor.



- **Hard Processor System (HPS)**
  - Selection of boot sources
  - Up to 2 10/100/1000 Mbps Ethernet MACs
  - Up to 2 USB 2.0 OTG Ports
  - Up to 2 CAN Interfaces
  - Up to 2 UARTs
  - 1 MMC/SD/SDIO
  - Up to 4 I2C controllers
  - Up to 2 master/2 slave SPI
  - 3 HPS PLLs

APPLICATIONS

- Machine Vision
- Test and Measurement
- Embedded Instrumentation
- Industrial Automation and Control
- Industrial Instrumentation
- Medical Instrumentation
- Closed Loop Motor Control

BENEFITS

- Rapid Development / Deployment
- Multiple Connectivity and I/O Options
- Rich User Interfaces
- High System Integration
- High Level OS Support
  - Embedded Linux
  - Micrium uC/OS (via 3rd Party)
  - Android (via 3rd Party)
  - QNX (via 3rd Party)

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DESCRIPTION

The MitySOM-5CSx with Dual Side Connectors (MitySOM-5CSx-DSC) is a highly configurable, small form-factor System-on-Module (SOM) featuring an Intel/Altera Cyclone V System-on-Chip (SoC). In addition to the processor, the module includes on-board power supplies, NOR FLASH, a DDR3 RAM memory subsystem, a real time clock (RTC), micro SD card, a USB 2.0 on the go (OTG) port, and a temperature sensor. The MitySOM-5CSx-DSC provides a complete and flexible CPU infrastructure for highly integrated embedded systems.

The MitySOM-5CSx-DSC is available with a 110 KLE Cyclone V SX which provides Dual-core Cortex-A9 32-bit RISC processors with dual NEON SIMD coprocessors. This MPU can run a rich set of real-time operating systems containing software applications programming interfaces (APIs) expected by modern system designers. The ARM architecture supports several operating systems, including Linux, Micrium uC/OS, Android and QNX.

Figure 1 illustrates a block diagram of the MitySOM-5CSx-DSC. As shown in the figure, the primary interface to the MitySOM-5CSx-DSC is through two 120-Pin vertical board-to-board mezzanine connectors, one on the top of the card and one on the bottom. The MitySOM-5CSx-DSC is intended to fit into a stacked card system. Details of the top and bottom interfaces are included in the Interface Description section.

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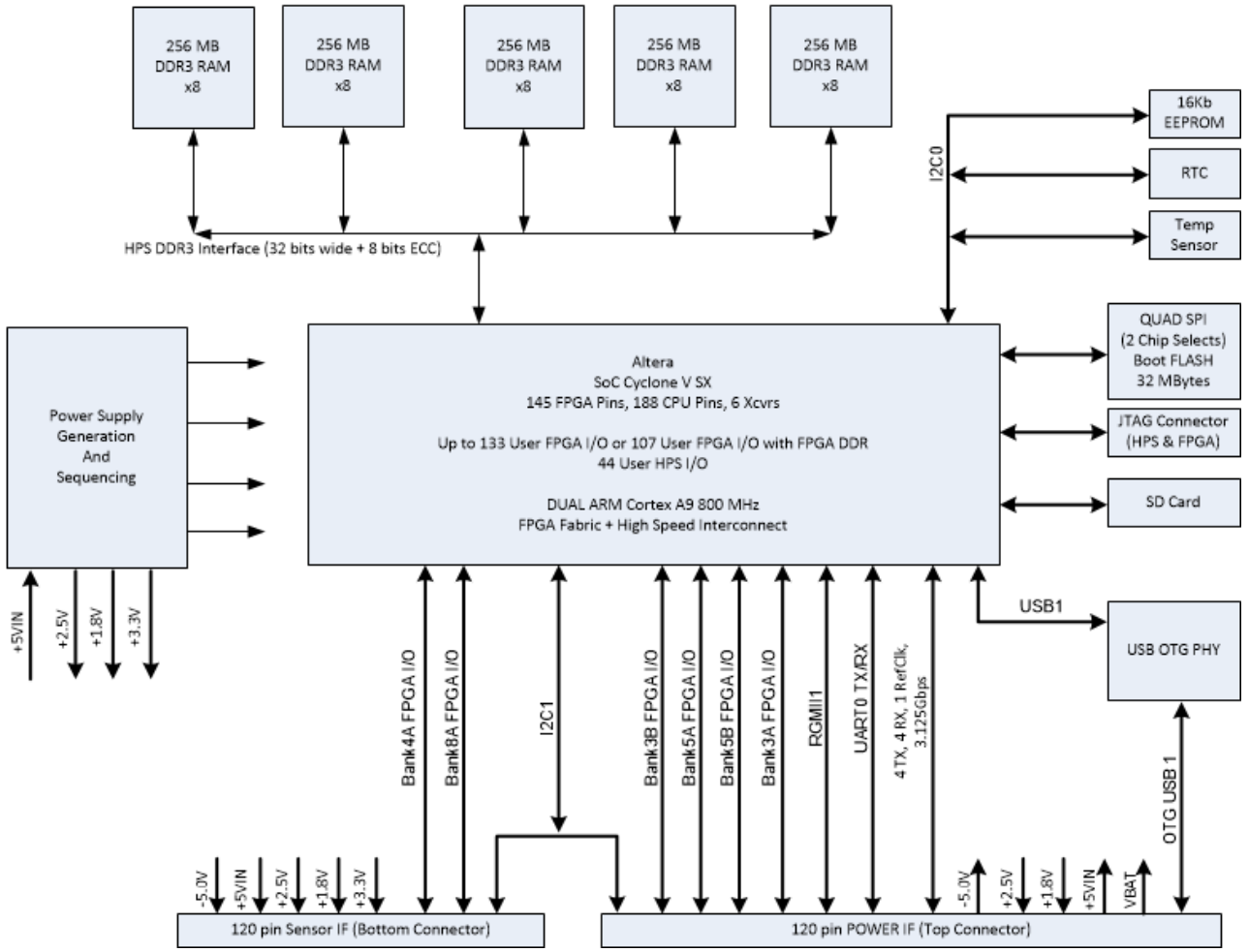

Figure 1 MitySOM-5CSx-DSC Block Diagram

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DDR3 Memory – HPS Memory

The MitySOM-5CSx-DSC includes one dedicated 40-bit DDR3 memory interface. The memory interface can be up-to 40-bits wide including 8-bits for ECC. A maximum of 2GB of DDR3 RAM with ECC is supported by the module.

The standard MitySOM-5CSx-DSC includes 1GB of DDR3 RAM with ECC (40-bits wide) integrated on the module.

This HPS DDR3 memory is available for both the HPS (Cortex-A9 ARM cores) as well as the FPGA fabric through either the AXI or Avalon high speed interfaces internal to the Cyclone V.

The MitySOM-5CSx-DSC family adheres to Intel/Altera's Cyclone V maximum memory speeds. The HPS memory clocked at 400Mhz as the maximum and a slower speed may be selected, if desired, down to 300MHz.

See Table 10: Standard Model Numbers for additional configuration details.

HPS-FPGA AXI

The high bandwidth HPS-FPGA AXI bridges provided by Intel/Altera in the Cyclone V SoC allow masters in the FPGA fabric to communicate with slaves in the HPS logic and vice versa. These bridges can be configured for 32, 64, or 128 bit widths.

For example, designers can instantiate additional memories or peripherals in the FPGA fabric, and master interfaces belonging to components in the HPS logic can access them. Designers can also instantiate components such as a Nios® II processor in the FPGA fabric and their master interfaces can access memories or peripherals in the HPS logic, including DDR3 Memory – HPS Memory.

NOR FLASH

A maximum of 32MB (2 16MB chips) of on-board NOR FLASH memory is connected to the Cyclone V using a Quad Serial Peripheral Interface (QSPI SS0 and SS1). This is a reliable flash memory that can be used as a boot media for the module.

Configuration EEPROM

MitySOM-5CSx-DSC modules contain a 2048 x 8-bit EEPROM that is used to hold factory configuration data for the module. The EEPROM is connected to the Cyclone V using the I2C0 interface. This EEPROM contains information such as the module type, Serial Number, and MAC addresses for the Ethernet interface(s).

On-board HPS Interfaces

The following on-board interfaces were chosen to provide the most flexibility for end user applications. As many HPS MUX options as possible were left available for the user. These interfaces should not be muxed external to the module on other pins.

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Console Serial port

The console serial port (UART0) is supported on pins 17 (RX) and 16 (TX) of the 120-Pin Top Side Connector (J200) with a simple TX/RX interface. By default, the flow control signals are not enabled but can be added to the console serial interface if desired.

Please reference the Top Side Pin-Out for specific Cyclone V pin-connections.

I2C0 Interface

The I2C0 peripheral is consumed local to the module. It is used for the Real Time Clock, Temperature Sensor, and Configuration EEPROM.

Table 1: I2C0 Peripherals

Address	Device	Feature
1010XXX	FT24C16A	16Kbit EEPROM for factory config parameters
1101001	AB1805-T3	Real Time Clock
1001000	AD7415ARTZ	Temperature sensor

QuadSPI Interface

The QUADSPI peripheral is wired to Bank 7B and is used for the NOR FLASH interface on the module. Both Slave select 0 and slave select 1 have been utilized for this NOR memory.

Table 2: QSPI Slave Selects

Slave Select	Feature	Memory Sizing
0	Boot flash*	128Mb –x4 width - 16MB max
1	Additional flash	128Mb –x4 width - 16MB max

***** Booting from QSPI requires a custom order / configuration, contact Critical Link

USB-2.0 OTG PHY

The USB1 interface of the Cyclone V processor is connected directly to a USB 2.0 OTG Physical Interface (PHY) on the PCA. The necessary USB ID, power and data pins are available on the Top Side board to board connector (J200) of the module.

Please see
Table 7 for the specific pin locations.

MicroSD / MMC Card

The HPS SD/MMC controller peripheral is connected via Bank 7 to a hinged micro-SD style connector (J103) on the PCA. The micro-SD media is primary boot and filesystem media for the default configuration of the MitySOM-5CSx-DSC PCA.

Debug JTAG

The JTAG interface signals for the Cyclone V processor have been brought out to a 10 pin dual row 2.0 mm right angle header, J2, which is intended for use with an available Critical Link breakout adapter.

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The debug adapter is not included with individual modules but is included with each Critical Link MitySOM-5CSx-DSC Development Kit that is ordered. If an adapter is needed please contact your Critical Link representative.

External Interfaces

The Cyclone V makes extensive use of functional pin multiplexing to provide a highly configurable device that can be tailored to a multitude of applications.

HPS Interfaces

A list of the interfaces/functions that are available to the user from the HPS is provided below.

- 1 Universal Serial Bus (USB) 2.0 High-Speed On-The-Go (OTG) port
- 2 Controller-Area Network (CAN) ports
- Up to 2 Gigabit Ethernet MAC's (10/100/1000 Mbps)
  - EMAC1 through HPS or FPGA fabric
  - EMAC0 through FPGA fabric
- 4 Serial Peripheral (SPI) ports
  - 2 Master
  - 2 Slave
- 2 Universal Asynchronous Receive/Transmit (UART) ports
- 4 Inter-Integrated Circuit (I2C) ports
  - I2C0 is connected to the on-board EEPROM, Temperature Sensor, and RTC

Additionally, most of the pin multiplexed signals can be configured as general purpose I/O signals with interrupt capability.

FPGA Interfaces

GPIO

Up to 112 FPGA IO pins are available externally to the module. Of these pins, up to 20 Receive LVDS pairs may be configured and up to 30 Transmit LVDS pairs may be configured.

The FPGA IO pins provided on the top side board to board connector are connected to Banks 5A, 5B, 3A, and 3B of the Cyclone V FPGA. The FPGA IO pins on the Bottom side board to board connector are connected Banks 3A, 4A, 7A, and 8A of the Cyclone V FPGA. The MityCAM Processor PCA supports configuring the IO voltages Bank 3A/3B (as a pair), Bank 4A, and Bank 5A/5B (as a pair) between either 2.5V or 1.8V. This is done with resistor pop/no-pop options on the PCA. The voltage for Bank 8A must be supplied by pin 1 of the bottom side board connector and may be 2.5V or 1.8V.

Two standard options for Bank Voltage configurations are currently supported and listed in the table below. If an alternate bank voltage configuration is required, please contact Critical Link.

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Table 3 Standard MitySOM-5CSx-DSC Bank Voltage Options

Configuration Option	Bank 3A/3B Voltage	Bank 4A Voltage	Bank 5A/5B Voltage
1.8V Sensor Interface	2.5 V	1.8 V	2.5V
2.5V Sensor Interface	2.5 V	2.5V	2.5V

3.125 Gbps Transceivers

A total of four (4) 3.125Gbps transceivers are available on the module for supporting high speed serial interfaces including PCIe Gen 1.0 x4 lanes. The module includes a reference 100 MHz low jitter clock source for use with the transceiver logic.

Configuration and Boot Modes

The Cyclone V has two groups of pins, documented below, that are read during reset to determine which media to boot from for the HPS (BSEL pins) and one group of pins that is used to configure the FPGA (MSEL pins). There are also pins used to control the HPS peripheral clock configuration on startup (CSEL pins). On the MitySOM-5CSx-DSC, the BSEL, MSEL, and CSEL pins are strapped to fixed settings on board as described below.

HPS Configuration pins

The BSEL and CSEL pins determine which memory interface has the bootloader and how to clock the interface. For booting the HPS, the BSEL and CSEL pins details are covered in CV-5400A[1].

BSEL (HPS Boot Select at Reset)

The MitySOM-5CSx-DSC supports two possible HPS boot options. The BSEL pins, which control the HPS boot configuration, are pulled high or low based on the selected option. The standard option is to boot from an installed MicroSD card flash memory (at 3.0V, BSEL pin option 5). A separate part number can be ordered for a MitySOM-5CSx-DSC to boot from the provided QSPI NOR flash (BSEL option 6). It is possible to convert the boot mode by populating and/or depopulating resistors on the board. If this is required, please contact Critical Link for assistance. Note: the pins for BSEL0 and BSEL2 are exposed on the board to board connectors to allow use after power up. Care must be taken to ensure these pins are floating during power up.

CSEL[0:1] (HPS Clock Select at Reset)

The HPS signals that include the two CLKSEL boot configuration pulled high or low on the MitySOM-5CSx-DSC to use the module's included 25MHz clock source into the osc1_clk pin. This is used as the primary clock source for the HPS processor PLL and HPS DDR PLL interface.

Note: the pins for CSEL0 and CSEL1 are exposed on the board to board connectors to allow use after power up. Care must be taken to ensure these pins are floating during power up.

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FPGA Configuration Pins

The FPGA MSEL configuration input pins are all pulled down to ground with a 1.0K resistors on the MitySOM-5CSx-DSC, selecting the Fast Passive Parallel (FPP) x16 mode. The FPGA should be configured using either the HPS internal FPGA manager or optionally using the JTAG interface.

Debug LEDs

There are 2 debug LEDs on the MitySOM-5CSx-DSC module.

The LEDs have been identified in Figure 2.

General Status LED's

Power OK

D4 indicates the MitySOM-5CSx-DSC on-module +3.3V supply is operating.

Configuration Debug

D2 indicates that FPGA configuration is not complete by lighting a yellow LED. This is only a warning rather than an error because the HPS can still boot and load the FPGA. This LED should turn on during initial power up until the FPGA is programmed.

Power Interfaces

The MitySOM-5CSx-DSC is powered using the +5V DC (+5VIN) input and ground pins on the top side board to board connector. The MitySOM-5CSx-DSC processor generates a +3.3V, +2.5V, +1.8V and +1.1V core voltage from the supplied +5V power supply for powering the local electronics. The MitySOM-5CSx-DSC processor provides the +3.3V, +2.5V, and +1.8V supply voltages to both the top and bottom connectors to support powering external electronics and proper supply sequencing for interfaces to the FPGA bank IO.

In addition, the MitySOM-5CSx-DSC allows several electrical pass-through connections between the top and bottom interfaces in order to allow providing custom power supplies and/ or signaling between the interface boards. These nets include the +12V, -5.0V, SPARE_V0, and SPARE_V1 signals present on both interfaces. The MitySOM-5CSx-DSC does not reference these nets, it simply connects them between the two connectors.

Software and Application Development Support

Users of the MitySOM-5CSx-DSC are encouraged to develop applications using the MitySOM-5CSx-DSC software development kit (SDK) provided by Critical Link LLC. The SDK is an expansion of the Intel/Altera platform support package for the Cyclone V and includes an implementation of a Yocto Project-compatible board support package providing a Linux root filesystem/distribution and compatible gcc compiler tool-chain with debugger.

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Growth Options

The MitySOM-5CSx-DSC has been designed to support several upgrade options. These options include a range of speed grades, FPGA density, HPS DDR memory configurations, and operating temperature specifications including commercial and industrial temperature ranges. The available options are listed in the section below containing ordering information. For additional ordering information and details regarding these options, or to inquire about a configuration not listed below, please contact a Critical Link sales representative.

Absolute Maximum Ratings

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office (info@criticallink.com) or unit Distributors for availability and specifications.

Table 4: Absolute Maximum Ratings

Maximum Supply Voltage (+5VIN)	5.2V
Storage Temperature Range	-55°C to 150°C

Operating Conditions

The following are the minimum temperature ratings for the components that are installed on a MitySOM-5CSx-DSC. For specifications not contained in this table please contact a Critical Link sales representative. Please see the Thermal Management section below concerning ambient/operating temperature recommendations.

Table 5: Module Component Temperature Ratings (minimum)

Temperature Range	Component Ratings
Commercial (-RC)	0°C to 70°C
Industrial (-RI)	-40°C to 85°C

Thermal Management

The MitySOM-5CSx-DSC module requires careful consideration of thermal management. Depending on processor load, thermal management may be required for operation at room temperatures and above. The primary thermal concern is with the Cyclone V SoC device. Even when idle, case temperature on this device rises significantly. Additional processing activity will require more power consumption and more heat dissipation.

Critical Link has operated the MitySOM-5CSx-DSC module without a heat sink or air flow on bench tops at room temperatures for long periods of time without issue.

Thermal management is a system level issue that must be addressed in conjunction with the overall system design. Some systems may have available airflow with limited space for a heat sink; others may have room for a heat sink with or without the possibility for additional airflow. As a result, the approach taken for thermal management is a design consideration that must be addressed by the overall system designers when integrating the MitySOM-5CSx-DSC.

Every end product is different and it is advisable to perform thorough testing to ensure that the product will meet desired performance and longevity specifications. Customers should use Intel/Altera's Early Power Estimator (EPE) for the Cyclone V. This utility will assist in

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estimating the potential power usage of the processor for a given application. Details can be found on the PowerPlay EPE[4] page at Altera.com. To achieve reliable operation at the maximum specified operating temperatures it has been determined that some form of thermal management (e.g., forced air, heat sink, etc.) will be required.

Example Thermal Dissipation Scenarios

By using the PowerPlay EPE for the Cyclone V SoC Critical Link has provided some example scenarios detailing the effects of different cooling fin and airflows. Please be advised these are only estimations based on the Intel/Altera modeling tool that are only being used to illustrate the effect of different heat dissipation techniques and are not tested conditions by Critical Link.

Table 6: Example EPE Based Scenarios

Cyclone V Power	Fin Size	Airflow	Max Ambient
2.90W	23 mm	200 LFM	71°C
4.25W	15 mm	None	49°C
4.25W	15 mm	100 LFM	55°C
4.25W	15 mm	400 LFM	65°C
4.25W	23 mm	200 LFM	65°C
4.25W	28 mm	400 LFM	67°C

Top Side Interface Description (J-200)

One of two primary interface connectors for the MitySOM-5CSx-DSC is the 120-pin board to board interface, J-200. The connector used for J-200 is a Samtech ERF8-060-05.0-S-DV-TR, which mates with Samtech ERM8-060-05.0-S-DV-TR (the mating height may be taller if desired). The interface consists of the following classes of signals:

- Power
  - Input – Input power to the module (**PWR_IN**)
  - Output – Voltage supply from the module (**PWR_OUT**)
  - Pass-Thru – Input Power that is passed from the Top Side to the Bottom Side of the module **(PWR_PT)**
- Dedicated signals mapped to the Cyclone V SoC HPS / FPGA pins (**5CSx_D**)
- Multi-function signals mapped to the Cyclone V SoC HPS pins (**5CSx_HPS**)
- General purpose I/O pins mapped to the Cyclone V SoC FPGA pins (**5CSx_IO**)
- Dedicated 3.125Gbps Transceiver signals mapped to the Cyclone V SoC (**5CSX_GXB**). Only available on Cyclone V SX based modules.
- USB 2.0 related functions (**USB**)

Table 7 contains a summary of the MitySOM-5CSx-DSC Top Side Interface pin-mapping.

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Table 7: MitySOM-5CSx-DSC Top Side Connector Pin-Out (J-200)

Module Pin Number	Class	SCH NET Name	Bank #	Cyclone V 5CSXFC6 U672
1	PWR_IN	GND		
2	PWR_IN	GND		
3	PWR_PT	+12V		
4	PWR_OUT	+3.3V		
5	PWR_IN	+5VIN		
6	PWR_PT	-5.0V		
7	PWR_IN	+5VIN		
8	PWR_OUT	+1.8V		
9	PWR_IN	+5VIN		
10	PWR_PT	SPARE_V0		
11	PWR_IN	GND		
12	PWR_PT	SPARE_V1		
13	5CSx_D	B7A_UART0_RTS/SPIM0_MOSI/**I2C1_SCL**/HPS_GPIO58	7A	C17
14	PWR_IN	GND		
15	5CSx_D	B7A_UART0_CTS/SPIM0_CLK/**I2C1_SDA**/HPS_GPIO57	7A	A18
16	5CSx_D	**B7A_UART0_TX**,CLKSEL0	7A	C16
17	5CSx_D	**B7A_UART0_RX**	7A	B19
18	PWR_IN	GND		
19	PWR_IN	GND		
20	5CSx_IO	B5A_PERSTL1_N	5A	W15
21	5CSx_IO	B5B_TX_R22_P	5B	AB26
22	5CSx_IO	B3B_RX_B35_P	3B	T13
23	5CSx_IO	B5B_TX_R22_N	5B	AA26
24	5CSx_IO	B3B_RX_B39_P	3B	V12
25	PWR_IN	GND		
26	5CSx_IO	B3B_RX_B39_N	3B	W12
27	5CSx_IO	B5A_TX_R1_N	5A	AE26
28	5CSx_IO	B3B_RX_B27_P	3B	T11
29	5CSx_IO	B5A_TX_R1_P	5A	AF26
30	5CSx_IO	B3B_RX_B27_N	3B	U11
31	5CSx_IO	B5A_TX_R3_N	5A	AD26
32	5CSx_IO	B3B_RX_B31_N	3B	W11
33	5CSx_IO	B5A_TX_R3_P	5A	AE25
34	5CSx_IO	B3A_RX_B3_N	3A	T8
35	5CSx_IO	B5A_TX_R5_P	5A	AC24
36	5CSx_IO	B3A_RX_B1_N	3A	W8
37	5CSx_IO	B5A_TX_R7_P	5A	AB23
38	5CSx_IO	B3B_TX_B2_P	3B	Y5
39	5CSx_IO	B5A_TX_R7_P	5A	AA24
40	5CSx_IO	B3A_TX_B2_N	3A	Y4
41	5CSx_IO	B5A_TX_R7_N	5A	AA23
42	5CSx_IO	B3A_RX_B1_N	3A	Y8
43	PWR_IN	GND		
44	PWR_IN	GND		
45	5CSx_IO	B3B_TX_B29_P	3B	AE8
46	5CSx_IO	B3B_TX_B28_P	3B	AE7
47	5CSx_IO	B3B_TX_B29_N	3B	AF9
48	5CSx_IO	B3B_TX_B29_N	3B	AF8
49	PWR_IN	GND		
50	PWR_IN	GND		
51	5CSx_IO	B3B_TX_B33_P	3B	AF7
52	5CSx_IO	B3B_TX_B32_N	3B	AF6
53	5CSx_IO	B3B_TX_B33_N	3B	AG6
54	5CSx_IO	B3B_TX_B32_P	3B	AF5
55	5CSx_IO	B3A_TX_B8_P	3A	AD5
56	5CSx_IO	B3B_TX_B40_P	3B	AH6
57	5CSx_IO	B3A_TX_B8_N	3A	AE6
58	5CSx_IO	B3B_TX_B40_N	3B	AH5
59	5CSx_IO	B3A_TX_B6_P	3A	AC4
60	5CSx_IO	B3B_TX_B37_P	3B	AG5
61	5CSx_IO	B3A_TX_B6_N	3A	AD4
62	5CSx_IO	B3B_TX_B37_N	3B	AH4
63	5CSx_IO	B3B_TX_B25_N	3B	AF4
64	5CSx_IO	B3B_TX_B36_P	3B	AH3
65	5CSx_IO	B3B_TX_B25_P	3B	AE4
66	5CSx_IO	B3B_TX_B36_N	3B	AH2
67	PWR_IN	GND		

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Module Pin Number	Class	SCH NET Name	Bank #	Cyclone V 5CSXFC6 U672
68	PWR_IN	GND		
69	5CSx_HPS	RGMII1_TX_CTL	7B	A12
70	5CSx_HPS	RGMII1_RX_CLK	7B	J12
71	5CSx_HPS	RGM11_TX_CLK	7B	J15
72	5CSx_HPS	RGMII1_RX_CTL	7B	J13
73	5CSx_HPS	RGMII1_TXD3	7B	D17
74	5CSx_HPS	RGMII1_RXD0	7B	A14
75	5CSx_HPS	RGMII1_TXD2	7B	A15
76	5CSx_HPS	RGMII1_RXD1	7B	A11
77	5CSx_HPS	RGMII1_TXD1	7B	J14
78	5CSx_HPS	RGMII1_RXD2	7B	C15
79	5CSx_HPS	RGMII1_TXD0	7B	A16
80	5CSx_HPS	RGMII1_RXD3	7B	A9
81	PWR_IN	GND		
82	5CSx_D	HPS_RST_N	7A	A23
83	5CSx_HPS	RGMII1_MDC	7B	A13
84	5CSx_HPS	RGMII1_MDIO	7B	E16
85	5CSx_HPS	HPS_GPIO28,BOOTSEL2/NAND_WE	7B	D15
86	USB	USB1_VBUS		
87	PWR_IN	+3VBAT		
88	USB	USB1_ID		
89	PWR_IN	GND		
90	PWR_IN	GND		
91	CSX_GXB	GXB_RX_0_P		
92	USB	USB1_D_N		
93	CSX_GXB	GXB_RX_0_N		
94	USB	USB1_D_P		
95	PWR_IN	GND		
96	PWR_IN	GND		
97	CSX_GXB	GXB_RX_1_P		
98	CSX_GXB	GXB_TX_0_P		
99	CSX_GXB	GXB_RX_1_N		
100	CSX_GXB	GXB_TX_0_N		
101	PWR_IN	GND		
102	PWR_IN	GND		
103	CSX_GXB	GXB_RX_2_P		
104	CSX_GXB	GXB_TX_1_P		
105	CSX_GXB	GXB_RX_2_N		
106	CSX_GXB	GXB_TX_1_N		
107	PWR_IN	GND		
108	PWR_IN	GND		
109	CSX_GXB	GXB_RX_3_P		
110	CSX_GXB	GXB_TX_2_P		
111	CSX_GXB	GXB_RX_3_N		
112	CSX_GXB	GXB_TX_2_N		
113	PWR_IN	GND		
114	PWR_IN	GND		
115	CSX_GXB	GXB_REFCLK1_P		
116	CSX_GXB	GXB_TX_3_P		
117	CSX_GXB	GXB_REFCLK1_N		
118	CSX_GXB	GXB_TX_3_N		
119	PWR_IN	GND		
120	PWR_IN	GND		

Bottom Side Interface Description (J-201)

One of two primary interface connectors for the MitySOM-5CSx-DSC is the 120-pin board to board interface, J-201. The connector used for J-201 is a Samtech ERM8-060-05.0-S-DV-TR, which mates with Samtech ERF8-060-05.0-S-DV-TR (the mating height may be taller if desired). The interface consists of the following classes of signals:

- Power
  - Output – Voltage supply from the module (**PWR_OUT**)
  - Pass-Thru – Input Power that is passed from the Top Side to the Bottom Side of the module **(PWR_PT)**

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- FPGA Bank Voltage – Input voltage used for a specified FPGA bank voltage **(PWR_BNK)**

- Dedicated signals mapped to the Cyclone V SoC HPS / FPGA pins (**5CSx_D**)
- Multi-function signals mapped to the Cyclone V SoC HPS pins (**5CSx_HPS**)
- General purpose I/O pins mapped to the Cyclone V SoC FPGA pins (**5CSx_IO**)

Table 8 contains a summary of the MitySOM-5CSx-DSC Bottom Side Interface pin-mapping.

Table 8: MitySOM-5CSx-DSC Bottom Side Connector Pin-Out (J-201)

Module Pin Number	Class	SCH NET Name	Bank #	Cyclone V 5CSXFC6 U672
1	PWR_BNK	VIO_8A	8A	E7
2	PWR_OUT	GND		
3	-	-		
4	5CSx_IO	B3A_RX_B5_N	3A	V10
5	-	-		
6	5CSx_IO	B3A_RX_B5_P	3A	U10
7	-	-		
8	PWR_OUT	GND		
9	-	-		
10	5CSx_IO	B3A_RX_B26_N	3A	AE9
11	-	-		
12	5CSx_IO	B3A_RX_B26_P	3A	AD10
13	PWR_OUT	GND		
14	PWR_OUT	GND		
15	5CSx_IO	B4A_RX_B43_N	4A	U13
16	5CSx_IO	B4A_TX_B44_N	4A	AH8
17	5CSx_IO	B4A_RX_B43_P	4A	U14
18	5CSx_IO	B4A_TX_B44_P	4A	AG9
19	5CSx_IO	B4A_RX_B51_N	4A	V13
20	5CSx_IO	B4A_TX_B48_P	4A	AG11
21	5CSx_IO	B4A_RX_B51_P	4A	W14
22	5CSx_IO	B4A_TX_B48_N	4A	AH11
23	5CSx_IO	B4A_TX_B45_N	4A	AH9
24	5CSx_IO	B4A_TX_B52_N	4A	AH13
25	5CSx_IO	B4A_TX_B45_P	4A	AG10
26	5CSx_IO	B4A_TX_B52_P	4A	AG14
27	5CSx_IO	B4A_RX_B42_N	4A	AF13
28	5CSx_IO	B4A_TX_B53_N	4A	AH14
29	5CSx_IO	B4A_RX_B42_P	4A	AG13
30	5CSx_IO	B4A_TX_B53_P	4A	AG15
31	PWR_OUT	GND		
32	PWR_OUT	GND		
33	5CSx_IO	B4A_RX_B47_CLK2_P	4A	Y13
34	5CSx_IO	B4A_RX_B46_N	4A	AE15
35	5CSx_IO	B4A_RX_B47_CLK2_N	4A	AA13
36	5CSx_IO	B4A_RX_B46_P	4A	AF15
37	PWR_OUT	GND		
38	5CSx_IO	B4A_TX_B56_N	4A	AH16
39	5CSx_IO	B4A_RX_B50_N	4A	AG16
40	5CSx_IO	B4A_TX_B56_P	4A	AH17
41	5CSx_IO	B4A_RX_B50_P	4A	AF17
42	5CSx_IO	B4A_RX_B54_N	4A	AE17
43	5CSx_IO	B4A_RX_B66_N	4A	AF21
44	5CSx_IO	B4A_RX_B54_P	4A	AD17
45	5CSx_IO	B4A_RX_B66_P	4A	AF22
46	5CSx_IO	B4A_TX_B60_N	4A	AH18
47	5CSx_IO	B4A_TX_B41_P	4A	AG8
48	5CSx_IO	B4A_TX_B60_P	4A	AG18
49	PWR_OUT	GND		
50	PWR_OUT	GND		
51	5CSx_HPS	GPIO61_A17	7A	A17
52	5CSx_IO	B4A_TX_B76_N	4A	AH26
53	PWR_OUT	GND		
54	5CSx_HPS	GPIO52_K18	7A	K18
55	5CSx_IO	CLKOUT/B8A_TX_T4_P	8A	E8
56	5CSx_HPS	GPIO54_J18	7A	J18
57	5CSx_IO	CLKOUT/B8A_TX_T4_N	8A	D8

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Module Pin Number	Class	SCH NET Name	Bank #	Cyclone V 5CSXFC6 U672
58	5CSx_HPS	GPIO56_C18	7A	C18
59	PWR_OUT	GND		
60	5CSx_HPS	GPIO49_A22	7A	A22
61	5CSx_D	B7A_UART0_CTS/SPIM0_CLK/**I2C1_SDA**/HPS_GPIO57	7A	A18
62	5CSx_HPS	GPIO53_A20	7A	A20
63	5CSx_D	B7A_UART0_RTS/SPIM0_MOSI/**I2C1_SCL**/HPS_GPIO58	7A	C17
64	5CSx_HPS	GPIO51_A21	7A	A21
65	PWR_OUT	GND		
66	5CSx_HPS	GPIO55_A19	7A	A19
67	5CSx_IO	REF_CLK_N	8A	C12
68	5CSx_HPS	GPIO50_B21		B21
69	5CSx_IO	REF_CLK_P	8A	D12
70	5CSx_IO	B4A_TX_B49_P	4A	AH12
71	PWR_OUT	GND		
72	PWR_OUT	GND		
73	5CSx_IO	B4A_TX_B57_P	4A	AF18
74	5CSx_IO	B4A_TX_B64_N	4A	AG20
75	5CSx_IO	B4A_TX_B61_N	4A	AH19
76	5CSx_IO	B4A_TX_B64_P	4A	AF20
77	5CSx_IO	B4A_TX_B61_P	4A	AG19
78	5CSx_IO	B4A_TX_B69_N	4A	AH22
79	5CSx_IO	B4A_TX_B58_P	4A	AE19
80	5CSx_IO	B4A_TX_B69_P	4A	AH23
81	5CSx_IO	B4A_TX_B58_N	4A	AD19
82	5CSx_IO	B4A_RX_B70_P	4A	AG23
83	PWR_OUT	GND		
84	5CSx_IO	B4A_RX_B70_N	4A	AF23
85	5CSx_IO	B4A_RX_B55_CLK3_N	4A	AA15
86	5CSx_IO	B4A_TX_B72_P	4A	AG24
87	5CSx_IO	B4A_RX_B55_CLK3_P	4A	Y15
88	5CSx_IO	B4A_TX_B72_N	4A	AH24
89	PWR_OUT	GND		
90	PWR_OUT	GND		
91	5CSx_IO	B4A_RX_B62_P	4A	AE20
92	5CSx_IO	B4A_RX_B74_P	4A	AE24
93	5CSx_IO	B4A_RX_B62_N	4A	AD20
94	5CSx_IO	B4A_RX_B74_N	4A	AE23
95	5CSx_IO	B4A_RX_B67_N	4A	AE22
96	5CSx_IO	B4A_RX_B78_N	4A	AG25
97	5CSx_IO	B4A_RX_B67_P	4A	AD23
98	5CSx_IO	B4A_RX_B78_P	4A	AF25
99	5CSx_IO	B4A_TX_B77_N	4A	AH27
100	5CSx_IO	B4A_TX_B80_N	4A	AF28
101	5CSx_IO	B4A_TX_B77_P	4A	AG28
102	5CSx_IO	B4A_TX_B80_P	4A	AF27
103	5CSx_IO	B4A_RX_B75_N	4A	AC23
104	5CSx_IO	B4A_RX_B59_N	4A	AA18
105	5CSx_IO	B4A_RX_B75_P	4A	AC22
106	5CSx_IO	B4A_RX_B59_P	4A	AA19
107	PWR_OUT	GND		
108	PWR_OUT	GND		
109	PWR_PT	SPARE_V1		
110	PWR_PT	+5VIN		
111	PWR_PT	SPARE_V0		
112	PWR_PT	+5VIN		
113	PWR_OUT	+1.8V		
114	PWR_OUT	GND		
115	PWR_PT	-5.0V		
116	PWR_OUT	+2.5V		
117	PWR_OUT	+3.3V		
118	PWR_PT	+12V		
119	PWR_OUT	GND		
120	PWR_OUT	GND		

Notes:

1) For more information about pin definitions and pin connection guidelines please refer to the Cyclone V Device Family Pin Connection Guidelines (http://www.altera.com/literature/dp/cyclone-v/PCG-01014.pdf)

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ELECTRICAL CHARACTERISTICS

Table 9: Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
+5VIN	Voltage supply, volt input.		4.8	5.0	5.15	Volts
$\mathbf{I_{5.0}}$	Quiescent Current draw	5.0 volt input, 800 MHz DDR3, no FPGA fabric, Linux prompt		410		mA
$\mathbf{I_{5.0\text{-}max}}$	Max current draw	5.0 volt input		TBS	TBS	mA
+3.3V	Voltage Supply, volt output.			3.3		Volts
$\mathbf{I_{3.3\text{-}max}}$	Max current draw	3.3 volt output			100	mA
+2.5V	Voltage Supply, volt output.			2.5		Volts
$\mathbf{I_{3.3\text{-}max}}$	Max current draw	2.5 volt output			TBS	mA
+1.8V	Voltage Supply, volt output.			1.8		Volts
$\mathbf{I_{3.3\text{-}max}}$	Max current draw	1.8 volt output			TBS	mA
	1. Power utilization of the MitySOM-5CSx-DSC is heavily dependent on end-user application. Major factors include: ARM CPU PLL configuration, CPU Utilization, and external DDR3 RAM utilization.					

ORDERING INFORMATION

The following table lists the standard module configurations. For shipping status, availability, and lead time of these configurations, or to inquire about a development kit for these products, contact Critical Link via email at info@criticallink.com.

Table 10: Standard Model Numbers

Model / Part Number	4A Bank	FPGA KLE	NOR	HPS BOOT	FPGA XCVR	HPS RAM	Component Temperature Ratings
5CSX-H6-4XA-RI-DA	1.8V	110	32MB	µSD	Y	1GB	-40°C to 85° C
5CSX-H6-4XA-RC-DA	1.8V	110	32MB	µSD	Y	1GB	0°C to 70° C
5CSX-H6-4XA-RI-DB	1.8V	110	32MB	NOR	Y	1GB	-40°C to 85° C
5CSX-H6-4XA-RI-DC	2.5V	110	32MB	µSD	Y	1GB	-40°C to 85° C
5CSX-H6-4XA-RC-DC	2.5V	110	32MB	µSD	Y	1GB	0°C to 70° C

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MECHANICAL INTERFACE

A top view mechanical outline of the MitySOM-5CSx-DSC is illustrated in Figure 2, below. A bottom view of the MitySOM-5CSx-DSC is illustrated in Figure 3. All dimensions are in mils.

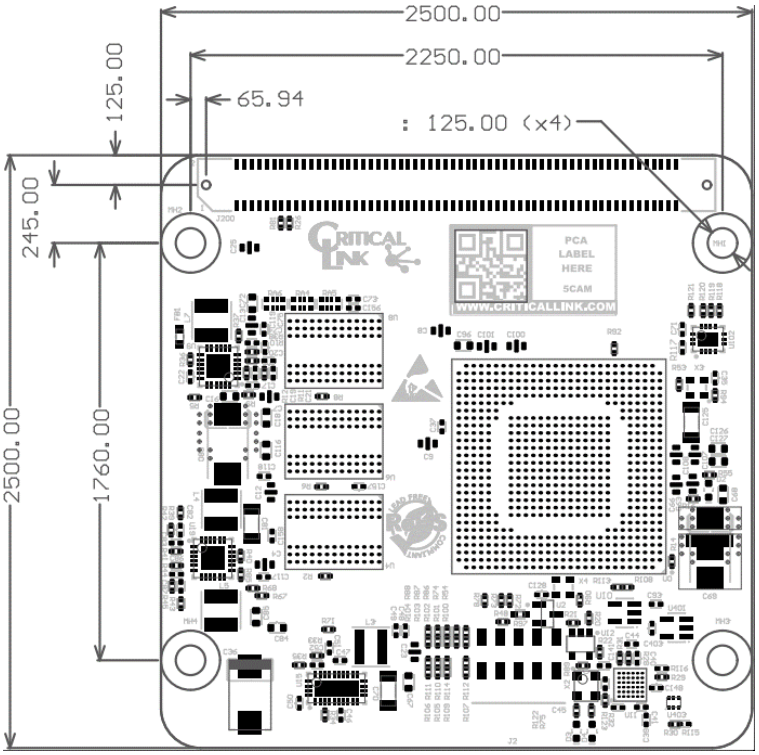

Figure 2 MitySOM-5CSx-DSC Mechanical Outline, View From Top

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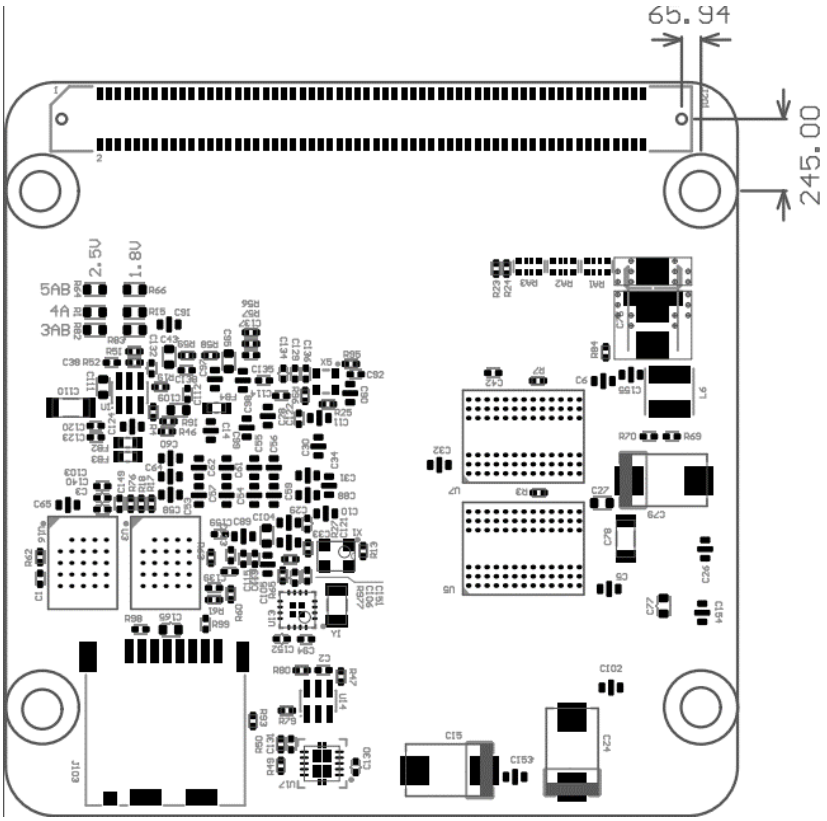

Figure 3 MitySOM-5CSx-DSC Mechanical Outline, View from Bottom

REVISION HISTORY

Revision	Date	Change Description
A	June 15, 2017	Initial release

FOOTNOTES

[1] http://www.altera.com/literature/hb/cyclone-v/cv_5400A.pdf

[2] http://www.altera.com/literature/hb/cyclone-v/cv_52007.pdf

[3] http://www.altera.com/support/devices/estimator/pow-powerplay.jsp

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