FEATURES

Intel Agilex 5E SoC

- Agilex 5 E-Series: 32mm x 32 mm package
- FPGA fabric up to 656 KLE
- Dual core Cortex-A76 + Dual core Cortex-A55

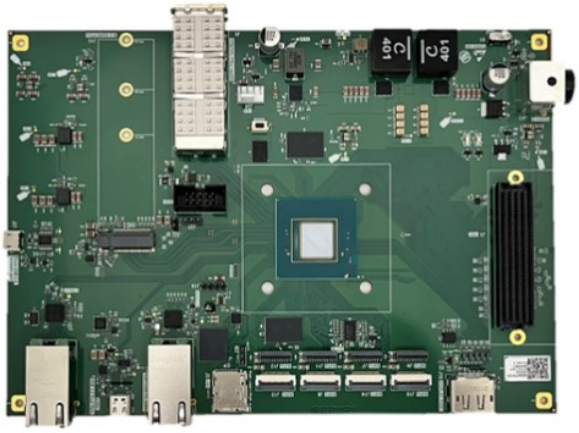
Memory

- Up to 8GB LPDDR4 HPS
- Up to 8GB LPDDR4 FPGA
- 64GB eMMC
- Micro-SD card
- 32MB QSPI NOR for configuration

Single 12V Power Input

Digital Interfaces

- DisplayPort Video Only Interface supporting 8K video at 60Hz
- USB-C port supporting USB 3.1
- 10/100/1000/25000 MBit Ethernet Interface
- 10/100/1000 MBit Ethernet Interface
- QSFP+ Interface supporting up to 40Gb/s
- Micro-USB 2.0 Console Interface
- Micro-SD/MMC Card Socket
- M.2 NVME / PCIe socket supporting up to 32Gb/s
- Eight 22-pin 4-lane MIPI camera interface ports
- FPGA Mezzanine Connector (FMC)



Software and Documentation

- Linux Kernel
- U-Boot

Applications

- IoT 4.0 edge computing
- Infrastructure and application acceleration
- Artificial intelligence (AI)
- 8K video processing
- Medical Equipment & Imaging
- Automated Test & Measurement
- Embedded Instrumentation
- Retail Automation
- Smart City / Infrastructure
- Broadcast & Pro-AV
- Radar & Defense
- FPGA Prototyping

DESCRIPTION

The MitySBC-A5E is a powerful single board computer utilizing Intel's Agilex 5E System on Chip (SoC) and provides multiple interfaces for developers. The Agilex 5E SoC is comprised of a dual core Cortex-A55 processor, dual core Cortex-A76 processor, and up to 656KLE of FPGA fabric, with on-board power supplies and memory subsystems.

Critical Link's MitySBC-A5E provides all the hardware and software support for system designers and developers to start a project utilizing the Agilex 5E Soc.

The MitySBC-A5E comes complete with all the connectivity needed in any application well suited for the Agilex 5E SoC, including DisplayPort, USB 3.1, up to 2.5Gb/s Ethernet, QSFP+, and PCIe 3.0. Additionally, the single board computer is equipped with a Micro-USB 2.0 console interface, Micro-SD card storage, and an FMC connector providing support for additional LVDS or high speed I/O signals.

A block diagram of the MitySBC-A5E is illustrated in Figure 1 below. All available processor interface pins are used directly by the MitySBC-A5E. Control of the onboard interface hardware and connected Expansion IO cards require proper configuration of the Agilex 5E. While not required, it is strongly recommended that the Agilex 5E software development kit and supplied API be used to manage these interfaces.

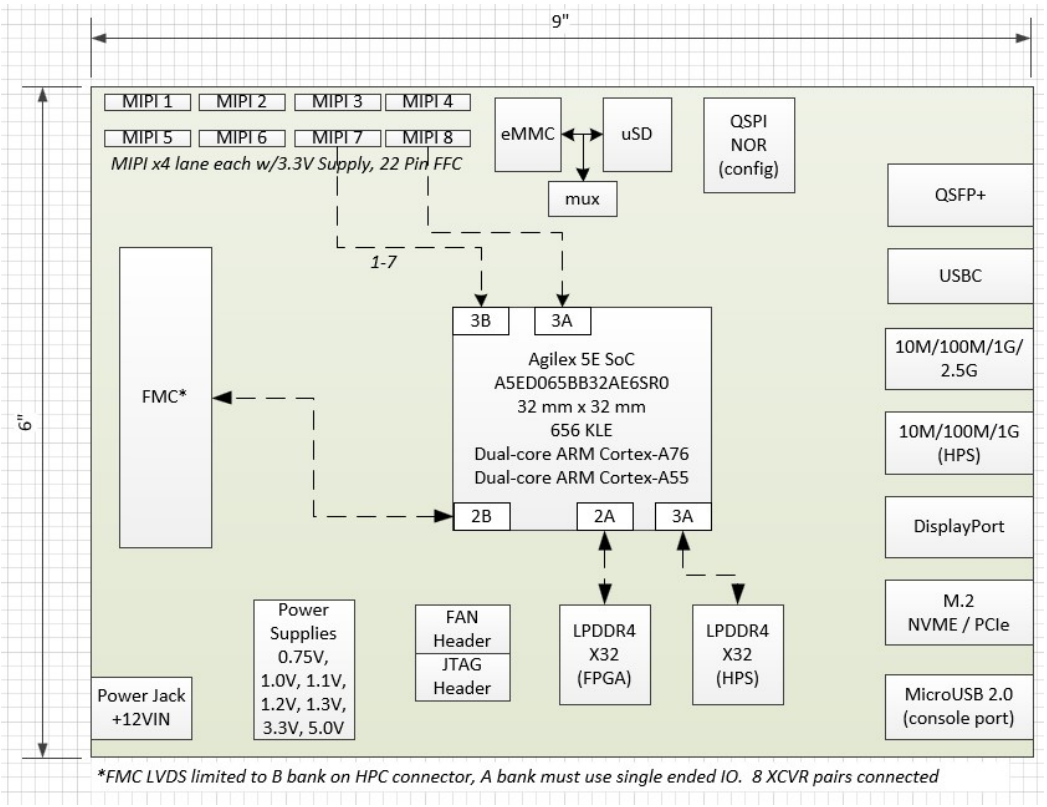


Figure 1: MitySBC-A5E Block Diagram

Additional details about the Intel Agilex 5, available peripherals, and their features are provided in the datasheet on the Intel website:
https://www.intel.com/content/www/us/en/products/details/fpga/agilex/5.html

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FEATURE DESCRIPTIONS

RS-232 / USB Bridge Console Port

The MitySBC-A5E includes a FT230XS UART to USB bridge chip interfacing the SoC. With a single micro-USB connection, the console port may be monitored using a standard terminal emulation program.

USB-C 3.1 Interface Description

A USB-C 3.1 is connected to the USB1 interface of the FPGA fabric. The interface is through a USB-C connector, J4, and the port is configured to operate in host mode. Linux drivers are available.

µSD/MMC Card Interface Description

The onboard Micro Secure Digital/MultiMedia Card (MMC) slot is MUXed between a Micro Secure Digital (µSD) connector J5 which supports SD Standard v3.01 and the eMMC flash. It is compatible with standard (SD), SDHC (up to 32GB), and SDXC (Up to 2TB) cards. By default, the MitySBC-A5E boots from this interface, specifically the µSD.

The eMMC flash provides 64GB of on-board storage utilizing the SDMMC interface. The eMMC flash is typically used to store the following types of data:

- Bootloaders
- ARM Linux embedded root file-system
- Runtime ARM software
- Runtime application data (non-volatile storage)

U-Boot configuration information and Linux drivers are available on Critical Link's support site.

Dual Gigabit Ethernet Interface Description

The on-board Ethernet interface features two network PHYs capable of running at 10/100/1000Mbit including link auto-negotiation and MII/MDIO capability. In addition, the network PHY associated with RJ-45 connector J18 also supports 2500Mbit. An industry-standard RJ-45 connector is provided for each external connection on J3 and J18. This Ethernet interface may be used to perform remote code download via U-Boot and flash updates to the MitySBC-A5E.

MIPI Camera Interface Description

The MitySBC-A5E provides eight 22-position flat flex cable interfaces, J7-J14, to the FPGA fabric, MIPI CSI v1.3 compliant devices supporting up to 4 data lanes at up to 2.5Gbps per lane, or 10Gbps total.

Display Port Interface Description

The MitySBC-A5E provides a standard display port interface, J16, for external monitor connection. The on-board DisplayPort supports DisplayPort 1.4 for a total bandwidth of 32.4Gbps with 32 audio channels and 8K video at 60Hz with 10-bit color resolution.

FMC Interface Description

The FMC interface, J1, is intended to support FMC cards utilizing up to 8 transceiver pairs. The LA bank IO signals support LVCMOS at 1.8V or 3.3V depending on the population of JP1 and JP2 respectively. The HA bank IO signals are not connected by default but can be by populating resistors R160-R207. These signals support LVDS or 1.2V LVCMOS. Note that the HA signals are not compliant with the FMC standard. The HB bank IO supports 1.2V LVCMOS or LVDS signaling.

QSFP+ Interface Description

The Quad Small Form-Factor Pluggable interface, J6, supports high data speeds of up to 10Gpbs per data lane. With four data lanes on the MitySBC-A5E, the maximum supported data rate is up to 40Gbps.

M.2 NVME/PCIe Interface

The MitySBC-A5E M.2 interface, J15, supports PCIe 3.0 protocol and is capable of data rates up to 32Gbps.

TI JTAG Interface Description

A 10-pin 0.1” pitch header, J2, is available onboard for debugging of the SoC with a compatible JTAG Emulator.

Control Pushbuttons

A debounced normally open, contact to ground, momentary pushbutton is included to signal the SoC HPS_COLD_nRESET button (S2).

LPDDR4 Memory

The MitySBC-A5E has 8GB of on board LPDDR4 memory for the HPS and another 8GB of on board LPDDR4 memory for the FPGA. Both LPDDR4 memories support operating at 800MHz clock rates, yielding up to 51.2Gbps data transfer speeds.

QSPI NOR Flash

The MitySBC-A5E has 256Mb of on board NOR Flash that supports 256Mbps data transfer speeds. The SoC can be configured to boot from this flash via the Secure Device Manager (SDM) AS_DATA interface.

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Supply Voltage[1]	12 V +/-10%
Storage Temperature Range	0 to 80C

OPERATING CONDITIONS

Ambient Temperature Range	0 to 70C
Humidity	0 to 95% Non-condensing

Notes:
1. The input voltage is used to supply both the 4-wire PC fan and the FMC connector. To comply with the FMC standard, the supply voltage should have a +/-5% tolerance.

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Typical	Limit	Units
Maximum Power Supply Output					
I_{Max}	12V Supply (AC Adapter) all components			TBD	A
I_{Max}	12V Supply[1] for external components			TBD	mA
I_{Max}	3.3V Supply[1] for external components			4.0	A
Power Dissipation					
V_S	Supply Voltage		12±10%		V
I_S	Supply Current[2]		TBD[1]		mA

Notes:
1. The maximum current supplied to external components should be limited to the specified maximum for both the 12V and 3.3V supplies.
2. Expansion card not attached, 100% SoC utilization, USB, and Dual Ethernet are enabled and active.

ELECTRICAL INTERFACE DESCRIPTIONS

Input Power – J17

The MitySBC-A5E power interface, J17, requires a single +12Volt power supply. J17 uses a Kycon Inc. KPJX-4S-S jack. Switch S1 is the main power switch to the SBC and can disable power to the SBC without having to disconnect J17.

Table 1: Input Power Interface Pin Description

Signal	J17 Position
+12V	1
+12V	2
GND	3
GND	4

MultiMedia Card (µSD) Interface – J5

The MitySBC-A5E provides an MMC interface that uses a standard Micro–Secure Digital (µSD) card slot for the physical interface. The slot is supplied with 3.3V for use with standard SD. The SDMMC signals from the SoC are MUXed between the multimedia card and the on board eMMC flash storage. The select pin of this MUX can be driven by the SoC with a selectable pull up/pull down resistor via a jumper on the J20 header. Placing the jumper over the pins along R216 to select the µSD storage at start up.

Table 2: J2 Micro SD Card Connector

J5 Pin	J6 Signal	FPGA Interface Signal	FPGA Pin
1	DAT2	SDMMC_DATA2	AL120
2	CD/DAT3	SDMMC_DATA3	R134
3	CMD	SDMMC_CMD	AG115
4	VDD	+3.3V	-
5	CLK	SDMMC_CLK	W134
6	VSS	GND	-
7	DAT0	SDMMC_DATA0	W135
8	DAT1	SDMMC_DATA1	U135
9	Switch (B)	SDCARD_PRSNT	U134
10	Switch(A)	GND	-

SDMMC Select Header – J20

The J20 header provides selection between booting from the µSD card slot or the eMMC flash. Table 3 lists the pinout for this header. If pins 1 and 2 are jumped, the µSD will be used to boot at startup. If pins 2 and 3 are jumped, the eMMC will be used to boot at startup.

Table 3: J20 SDMMC Select Pin Assignments

Pin	Schematic Signal	Type	Standard	FPGA Pin	Notes
1	GND	Power	-	-	This is the pin closest to the A5E processor
2	SDMMC_SELECT	I/O	1.8V LVCMOS	N134	
3	+1.8V	Power	-	-	

USB 3.1 Type-C – J4

The MitySBC-A5E features a USB C port J4. This interface is a USB 3.1 interface and supports up to 5Gbps throughput speeds and is backward compatible with USB 2.x USB C devices. The port can supply a maximum of 1A of current at +5V and an overcurrent detection circuit monitors the output power. The pinout for J4 is included in Table 4.

Table 4 USB Host Connector Pin Out, J4

J4 Pin	J4 Signal	IC
A1	GND	-
A2	TX1_P	DRP Port Cntrl
A3	TX1_N	DRP Port Cntrl
A4	VBUS	-
A5	CC1	DRP Port Cntrl
A6	USB1_DATA_P	ULPI
A7	USB1_DATA_N	ULPI
A8	NC	-
A9	VBUS	-
A10	RX2_N	DRP Port Cntrl
A11	RX2_P	DRP Port Cntrl
A12	GND	-
B1	GND	-
B2	TX2_P	DRP Port Cntrl
B3	TX2_N	DRP Port Cntrl
B4	VBUS	N/A
B5	CC2	DRP Port Cntrl
B6	USB1_DATA_P	ULPI
B7	USB1_DATA_N	ULPI
B8	NC	-
B9	VBUS	-
B10	RX1_N	DRP Port Cntrl
B11	RX1_P	DRP Port Cntrl
B12	GND	-

USB 3.1 DRP Port Controller – U8

The DRP port controller (MPN: HD3SS3220IRNHR) manages mode configuration, the detection of a USB device, cable orientation detection, role detection and the required power supply for the connected device. All of these can be communicated back to the FPGA via the signals listed below.

Table 5: DRP Port Controller Signals

J4 Pin	J4 Side Signal	FPGA Side Signal	FPGA Pin
A2	TX1_P	USB1_SSRX_P	AN129
A3	TX1_N	USB1_SSRX_N	AN126
A5	CC1	I3C1_Sxx	SDA – N135 SCL – AK120
		USBC_ID_3V3	CG135
A10	RX2_N	USB1_SSTX_N	AM133
A11	RX2_P	USB1_SSTX_P	AM135
B2	TX2_P	USB1_SSTX_P	AM135
B3	TX2_N	USB1_SSTX_N	AM133
B5	CC2	I3C1_Sxx	SDA – N135 SCL – AK120
		USBC_ID_3V3	CG135
B10	RX1_N	USB1_SSRX_N	AN126
B11	RX1_P	USB1_SSRX_P	AN129
N/A	N/A	USB1_MuxEnable_3V3	BH118

USB 3.1 ULPI Transceiver – U9

The ULPI transceiver (MPN: USB3320C-EZK) provides role detection and full support for On-The-Go protocol 2.0.

Table 6: ULPI Transceiver Signals

J4 Pin	J4 Sided Signal	FPGA Sided Signal	FPGA Pin
A6	USB1_DATA_P	USB1_DATAx	USB1_DATA0 – AD135 USB1_DATA1 – M132 USB1_DATA2 – K132 USB1_DATA3 – AG129 USB1_DATA4 – J134 USB1_DATA5 – AG120 USB1_DATA6 – G134 USB1_DATA7 – G135
A7	USB1_DATA_N		
B6	USB1_DATA_P	USB1_DATAx	USB1_DATA0 – AD135 USB1_DATA1 – M132 USB1_DATA2 – K132 USB1_DATA3 – AG129 USB1_DATA4 – J134 USB1_DATA5 – AG120 USB1_DATA6 – G134 USB1_DATA7 – G135
B7	USB1_DATA_N		
N/A	N/A	USB1_DIR	J135
N/A	N/A	USB1_NXT	AD134
N/A	N/A	USB1_STP	L135
N/A	N/A	USB1_CLK	P132

Display Port Interface – J16

The MitySBC-A5E provides a 20-pin standard display port connector, J16. Supporting display port 1.4, the SoC can output up to a resolution of 8K at 60Hz. The AUX signals are additionally routed through a transceiver resulting in signals AUX_TX_DRV_OUT_3V3 and AUX_TX_DRV_IN_3V3 which correspond to FPGA pins BR118 and CA118 respectively. The transceiver for AUX_TX_DRV_OUT_3V3 is gated by an enable signal: AUX_TX_DRV_OE_3V3 which is tied to BU118 of the FPGA.

Table 7: J16 Connector Pin Assignments

Pin	Signal	Type	Standard	FPGA Pin
1	DispPort Tx0_+	O	HSCL	AU7
2	Shield	Power	-	-
3	DispPort Tx0_-	O	HSCL	AU10
4	DispPort Tx1_+	O	HSCL	AR7
5	Shield	Power	-	-
6	DispPort Tx1_-	O	HSCL	AR10
7	DispPort Tx2_+	O	HSCL	AN7
8	Shield	Power	-	-
9	DispPort Tx2_-	O	HSCL	AN10
10	DispPort Tx3_+	O	HSCL	AL7
11	Shield	Power	-	-
12	DispPort Tx3_-	O	HSCL	AL10
13	TX_CONFIG1_3V3	I	-	CL125
14	Reserved	-	-	-
15	AUX_CH_+	O	HSCL	CH128
16	Shield	Power	-	-
17	AUX_CH_-	O	HSCL	CK134
18	TX_HPD_3V3	I	-	CF121
19	GND	Power	-	-
20	+3.3V	Power	-	-

Camera MIPI Interfaces – J7-J14

The MitySBC-A5E provides eight 22-pin 0.5 mm pitch flat flex connectors, J7-J14, to interface with the FPGA fabric. Note that the I2C interface is split utilizing an octal bidirectional translating switch (MPN: PCA9548A) which is controlled via the I2C1 bus.

Table 8: Camera Mipi Connector Pin Assignments

Pin	Signal	Type	Standard	FPGA Pin	Notes
CAM1 – J7					
1	+3.3V	-	-	-	Max 500 mA
2	CAM1_SDA_3V3	I/O	DPHY_RX	M127	
3	CAM1_SCL_3V3	I/O	DPHY_RX	K127	
4	GND	-	-	-	
5	CAM1_IO2_3V3	I/O	DPHY_RX	BF115	
6	CAM1_IO1_3V3	I/O	DPHY_RX	BE115	
7	GND	-	-	-	
8	CAM1_CSI_RX3_P	I	DPHY_RX	B45	
9	CAM1_CSI_RX3_N	I	DPHY_RX	A48	
10	GND	-	-	-	
11	CAM1_CSI_RX2_P	I	DPHY_RX	B51	
12	CAM1_CSI_RX2_N	I	DPHY_RX	A51	
13	GND	-	-	-	
14	CAM1_CSI_RXCLK_P	I	DPHY_RX	A54	
15	CAM1_CSI_RXCLK_N	I	DPHY_RX	B54	
16	GND	-	-	-	
17	CAM1_CSI_RX1_P	I	LVCMOS	A63	
18	CAM1_CSI_RX1_N	I	LVCMOS	B60	
19	GND	-	-	-	
20	CAM1_CSI_RX0_P	I	LVCMOS / OD	B56	
21	CAM1_CSI_RX0_N	I	LVCMOS / OD	A60	
22	GND	Power	-	-	
CAM2 – J9					
1	+3.3V	-	-	-	Max 500 mA
2	CAM2_SDA_3V3	I/O	DPHY_RX	M127	
3	CAM2_SCL_3V3	I/O	DPHY_RX	K127	
4	GND	-	-	-	
5	CAM2_IO2_3V3	I/O	DPHY_RX	BU109	
6	CAM2_IO1_3V3	I/O	DPHY_RX	BF107	
7	GND	-	-	-	
8	CAM2_CSI_RX3_P	I	DPHY_RX	P44	
9	CAM2_CSI_RX3_N	I	DPHY_RX	T44	
10	GND	-	-	-	
11	CAM2_CSI_RX2_P	I	DPHY_RX	V47	
12	CAM2_CSI_RX2_N	I	DPHY_RX	T47	
13	GND	-	-	-	
14	CAM2_CSI_RXCLK_P	I	DPHY_RX	K55	
15	CAM2_CSI_RXCLK_N	I	DPHY_RX	M55	
16	GND	-	-	-	
17	CAM2_CSI_RX1_P	I	LVCMOS	V58	
18	CAM2_CSI_RX1_N	I	LVCMOS	T58	
19	GND	-	-	-	
20	CAM2_CSI_RX0_P	I	LVCMOS / OD	P55	
21	CAM2_CSI_RX0_N	I	LVCMOS / OD	T55	
22	GND	Power	-	-	
CAM3 – J13					
1	+3.3V	-	-	-	Max 500 mA
2	CAM3_SDA_3V3	I/O	DPHY_RX	M127	
3	CAM3_SCL_3V3	I/O	DPHY_RX	K127	
4	GND	-	-	-	
5	CAM3_IO2_3V3	I/O	DPHY_RX	BR109	
6	CAM3_IO1_3V3	I/O	DPHY_RX	BF104	
7	GND	-	-	-	
8	CAM3_CSI_RX3_P	I	DPHY_RX	F47	
9	CAM3_CSI_RX3_N	I	DPHY_RX	H47	

Pin	Signal	Type	Standard	FPGA Pin	Notes
10	GND	-	-	-	
11	CAM3_CSI_RX2_P	I	DPHY_RX	M47	
12	CAM3_CSI_RX2_N	I	DPHY_RX	K47	
13	GND	-	-	-	
14	CAM3_CSI_RXCLK_P	I	DPHY_RX	F55	
15	CAM3_CSI_RXCLK_N	I	DPHY_RX	D55	
16	GND	-	-	-	
17	CAM3_CSI_RX1_P	I	LVCMOS	M58	
18	CAM3_CSI_RX1_N	I	LVCMOS	K58	
19	GND	-	-	-	
20	CAM3_CSI_RX0_P	I	LVCMOS / OD	H58	
21	CAM3_CSI_RX0_N	I	LVCMOS / OD	F58	
22	GND	Power	-	-	
CAM4 – J10					
1	+3.3V	-	-	-	Max 500 mA
2	CAM4_SDA_3V3	I/O	DPHY_RX	M127	
3	CAM4_SCL_3V3	I/O	DPHY_RX	K127	
4	GND	-	-	-	
5	CAM4_IO2_3V3	I/O	DPHY_RX	BK109	
6	CAM4_IO1_3V3	I/O	DPHY_RX	BE107	
7	GND	-	-	-	
8	CAM4_CSI_RX3_P	I	DPHY_RX	Y58	
9	CAM4_CSI_RX3_N	I	DPHY_RX	Y55	
10	GND	-	-	-	
11	CAM4_CSI_RX2_P	I	DPHY_RX	AC53	
12	CAM4_CSI_RX2_N	I	DPHY_RX	AC50	
13	GND	-	-	-	
14	CAM4_CSI_RXCLK_P	I	DPHY_RX	AG57	
15	CAM4_CSI_RXCLK_N	I	DPHY_RX	AG53	
16	GND	-	-	-	
17	CAM4_CSI_RX1_P	I	LVCMOS	AG61	
18	CAM4_CSI_RX1_N	I	LVCMOS	AC61	
19	GND	-	-	-	
20	CAM4_CSI_RX0_P	I	LVCMOS / OD	AC64	
21	CAM4_CSI_RX0_N	I	LVCMOS / OD	AG64	
22	GND	Power	-	-	
CAM5 – J8					
1	+3.3V	-	-	-	Max 500 mA
2	CAM5_SDA_3V3	I/O	DPHY_RX	M127	
3	CAM5_SCL_3V3	I/O	DPHY_RX	K127	
4	GND	-	-	-	
5	CAM5_IO2_3V3	I/O	DPHY_RX	BM109	
6	CAM5_IO1_3V3	I/O	DPHY_RX	BE107	
7	GND	-	-	-	
8	CAM5_CSI_RX3_P	I	DPHY_RX	K84	
9	CAM5_CSI_RX3_N	I	DPHY_RX	M84	
10	GND	-	-	-	
11	CAM5_CSI_RX2_P	I	DPHY_RX	V87	
12	CAM5_CSI_RX2_N	I	DPHY_RX	T87	
13	GND	-	-	-	
14	CAM5_CSI_RXCLK_P	I	DPHY_RX	K95	
15	CAM5_CSI_RXCLK_N	I	DPHY_RX	M95	
16	GND	-	-	-	
17	CAM5_CSI_RX1_P	I	LVCMOS	P95	
18	CAM5_CSI_RX1_N	I	LVCMOS	T95	
19	GND	-	-	-	
20	CAM5_CSI_RX0_P	I	LVCMOS / OD	V98	

Pin	Signal	Type	Standard	FPGA Pin	Notes
21	CAM5_CSI_RX0_N	I	LVCMOS / OD	T98	
22	GND	Power	-	-	
CAM6 – J12					
1	+3.3V	-	-	-	Max 500 mA
2	CAM6_SDA_3V3	I/O	DPHY_RX	M127	
3	CAM6_SCL_3V3	I/O	DPHY_RX	K127	
4	GND	-	-	-	
5	CAM6_IO2_3V3	I/O	DPHY_RX	BK118	
6	CAM6_IO1_3V3	I/O	DPHY_RX	BR112	
7	GND	-	-	-	
8	CAM6_CSI_RX3_P	I	DPHY_RX	H67	
9	CAM6_CSI_RX3_N	I	DPHY_RX	F67	
10	GND	-	-	-	
11	CAM6_CSI_RX2_P	I	DPHY_RX	M67	
12	CAM6_CSI_RX2_N	I	DPHY_RX	K67	
13	GND	-	-	-	
14	CAM6_CSI_RXCLK_P	I	DPHY_RX	D74	
15	CAM6_CSI_RXCLK_N	I	DPHY_RX	F74	
16	GND	-	-	-	
17	CAM6_CSI_RX1_P	I	LVCMOS	F77	
18	CAM6_CSI_RX1_N	I	LVCMOS	H77	
19	GND	-	-	-	
20	CAM6_CSI_RX0_P	I	LVCMOS / OD	K77	
21	CAM6_CSI_RX0_N	I	LVCMOS / OD	M77	
22	GND	Power	-	-	
CAM7 – J14					
1	+3.3V	-	-	-	Max 500 mA
2	CAM7_SDA_3V3	I/O	DPHY_RX	M127	
3	CAM7_SCL_3V3	I/O	DPHY_RX	K127	
4	GND	-	-	-	
5	CAM7_IO2_3V3	I/O	DPHY_RX	BP112	
6	CAM7_IO1_3V3	I/O	DPHY_RX	BM118	
7	GND	-	-	-	
8	CAM7_CSI_RX3_P	I	DPHY_RX	M65	
9	CAM7_CSI_RX3_N	I	DPHY_RX	K65	
10	GND	-	-	-	
11	CAM7_CSI_RX2_P	I	DPHY_RX	V67	
12	CAM7_CSI_RX2_N	I	DPHY_RX	T67	
13	GND	-	-	-	
14	CAM7_CSI_RXCLK_P	I	DPHY_RX	M74	
15	CAM7_CSI_RXCLK_N	I	DPHY_RX	K74	
16	GND	-	-	-	
17	CAM7_CSI_RX1_P	I	LVCMOS	V77	
18	CAM7_CSI_RX1_N	I	LVCMOS	T77	
19	GND	-	-	-	
20	CAM7_CSI_RX0_P	I	LVCMOS / OD	P74	
21	CAM7_CSI_RX0_N	I	LVCMOS / OD	T74	
22	GND	Power	-	-	
CAM8 – J11					
1	+3.3V	-	-	-	Max 500 mA
2	CAM8_SDA_3V3	I/O	DPHY_RX	M127	
3	CAM8_SCL_3V3	I/O	DPHY_RX	K127	
4	GND	-	-	-	
5	CAM8_IO2_3V3	I/O	DPHY_RX	BK112	
6	CAM8_IO1_3V3	I/O	DPHY_RX	BM112	
7	GND	-	-	-	
8	CAM8_CSI_RX3_P	I	DPHY_RX	B70	

Pin	Signal	Type	Standard	FPGA Pin	Notes
9	CAM8_CSI_RX3_N	I	DPHY_RX	A70	
10	GND	-	-	-	
11	CAM8_CSI_RX2_P	I	DPHY_RX	B73	
12	CAM8_CSI_RX2_N	I	DPHY_RX	A76	
13	GND	-	-	-	
14	CAM8_CSI_RXCLK_P	I	DPHY_RX	A80	
15	CAM8_CSI_RXCLK_N	I	DPHY_RX	B76	
16	GND	-	-	-	
17	CAM8_CSI_RX1_P	I	LVCMOS	B85	
18	CAM8_CSI_RX1_N	I	LVCMOS	A85	
19	GND	-	-	-	
20	CAM8_CSI_RX0_P	I	LVCMOS / OD	A82	
21	CAM8_CSI_RX0_N	I	LVCMOS / OD	B82	
22	GND	Power	-	-	

FMC Interface – J1

The MitySBC-A5E provides an FMC expansion connector on the top of the board. An ASP-134486-01 connector is used and mates with standard 0.1” dual row male headers. This expansion interface can be used for many different add-on cards due to it having I2C and General Purpose Memory Controller (GPMC) Address/Data pins with control signals directly from the SoC. 3.3V and +12V supply pins are provided on the connector to support powering external cards. All power to the FMC connector is gated by FMC_EN_3V3 which is tied to pin CG134 of the FPGA. Table 9 provides signal descriptions for each pin.

Table 9: J3 Connector Pin Assignments

Pin	Schematic Signal	Type	Standard	FPGA Pin	Notes
A1	GND	Power	-	-	
A2	DP1_M2C_P	I	-	BD1	GTSR4B_RX_CH1P
A3	DP1_M2C_N	I	-	BD3	GTSR4B_RX_CH1N
A4	GND	Power	-	-	
A5	GND	Power	-	-	
A6	DP2_M2C_P	I	-	BB1	GTSR4B_RX_CH2P
A7	DP2_M2C_N	I	-	BB3	GTSR4B_RX_CH2N
A8	GND	Power	-	-	
A9	GND	Power	-	-	
A10	DP3_M2C_P	I	-	AY1	GTSR4B_RX_CH3P
A11	DP3_M2C_N	I	-	AY3	GTSR4B_RX_CH3N
A12	GND	Power	-	-	
A13	GND	Power	-	-	
A14	DP4_M2C_P	I	-	BN1	GTSR4A_RX_CH2P
A15	DP4_M2C_N	I	-	BN3	GTSR4A_RX_CH2N
A16	GND	Power	-	-	
A17	GND	Power	-	-	
A18	DP5_M2C_P	I	-	BJ1	GTSR4A_RX_CH3P
A19	DP5_M2C_N	I	-	BJ3	GTSR4A_RX_CH3N
A20	GND	Power	-	-	
A21	GND	Power	-	-	
A22	DP1_C2M_P	O	-	BC7	GTSR4B_TX_CH1P
A23	DP1_C2M_N	O	-	BC10	GTSR4B_TX_CH1N
A24	GND	Power	-	-	
A25	GND	Power	-	-	
A26	DP2_C2M_P	O	-	BA7	GTSR4B_TX_CH2P
A27	DP2_C2M_N	O	-	BA10	GTSR4B_TX_CH2N
A28	GND	Power	-	-	
A29	GND	Power	-	-	
A30	DP3_C2M_P	O	-	AW7	GTSR4B_TX_CH3P
A31	DP3_C2M_N	O	-	AW10	GTSR4B_TX_CH3N
A32	GND	Power	-	-	
A33	GND	Power	-	-	
A34	DP4_C2M_P	O	-	BL7	GTSR4A_TX_CH2P
A35	DP4_C2M_N	O	-	BL10	GTSR4A_TX_CH2N
A36	GND	Power	-	-	
A37	GND	Power	-	-	
A38	DP5_C2M_P	O	-	BG7	GTSR4A_TX_CH3P
A39	DP5_C2M_N	O	-	BG10	GTSR4A_TX_CH3N
A40	GND	Power	-	-	
B1	N/C	-	-	-	
B2	GND	Power	-	-	
B3	GND	Power	-	-	
B4	N/C	-	-	-	
B5	N/C	-	-	-	
B6	GND	Power	-	-	
B7	GND	Power	-	-	
B8	N/C	-	-	-	
B9	N/C	-	-	-	
B10	GND	Power	-	-	
B11	GND	Power	-	-	
B12	DP7_M2C_P	I	-	BV1	GTSR4A_RX_CH1P
B13	DP7_M2C_N	I	-	BV3	GTSR4A_RX_CH1N
B14	GND	Power	-	-	
B15	GND	Power	-	-	
B16	DP6_M2C_P	I	-	CB1	GTSR4A_RX_CH0P
B17	DP6_M2C_N	I	-	CB3	GTSR4A_RX_CH0N
B18	GND	Power	-	-	
B19	GND	Power	-	-	
B20	GBTCLK1_M2C_P	I	LVDS	BB16	REFCLK_GTSR4A_CH1P
B21	GBTCLK1_M2C_N	I	LVDS	BB21	REFCLK_GTSR4A_CH1N
B22	GND	Power	-	-	
B23	GND	Power	-	-	

Pin	Schematic Signal	Type	Standard	FPGA Pin	Notes
B24	N/C	-	-	-	
B25	N/C	-	-	-	
B26	GND	Power	-	-	
B27	GND	Power	-	-	
B28	N/C	-	-	-	
B29	N/C	-	-	-	
B30	GND	Power	-	-	
B31	GND	Power	-	-	
B32	DP7_C2M_P	O	-	BT7	GTSR4A_TX_CH1P
B33	DP7_C2M_N	O	-	BT10	GTSR4A_TX_CH1N
B34	GND	Power	-	-	
B35	GND	Power	-	-	
B36	DP6_C2M_P	O	-	BY7	GTSR4A_TX_CH0P
B37	DP6_C2M_N	O	-	BY10	GTSR4A_TX_CH0N
B38	GND	Power	-	-	
B39	GND	Power	-	-	
B40	N/C	-	-	-	
C1	GND	Power	-	-	
C2	DP0_C2M_P	O	-	BE7	
C3	DP0_C2M_N	O	-	BE10	
C4	GND	Power	-	-	
C5	GND	Power	-	-	
C6	DP0_M2C_P	I	-	-	
C7	DP0_M2C_N	I	-	-	
C8	GND	Power	-	-	
C9	GND	Power	-	-	
C10	LA06_P	I/O	1.8V or 3.3V LVCMOS	BE29	HVIO_6B (1.8 or 3.3V)
C11	LA06_N	I/O	1.8V or 3.3V LVCMOS	BE25	HVIO_6B (1.8 or 3.3V)
C12	GND	Power	-	-	
C13	GND	Power	-	-	
C14	LA10_P	I/O	1.8V or 3.3V LVCMOS	BF32	HVIO_6B (1.8 or 3.3V)
C15	LA10_N	I/O	1.8V or 3.3V LVCMOS	BF36	HVIO_6B (1.8 or 3.3V)
C16	GND	Power	-	-	
C17	GND	Power	-	-	
C18	LA14_P	I/O	1.8V or 3.3V LVCMOS	BF29	HVIO_6B (1.8 or 3.3V)
C19	LA14_N	I/O	1.8V or 3.3V LVCMOS	BF25	HVIO_6B (1.8 or 3.3V)
C20	GND	Power	-	-	
C21	GND	Power	-	-	
C22	LA18_P	I/O	1.8V or 3.3V LVCMOS	BF16	HVIO_6B (1.8 or 3.3V)
C23	LA18_N	I/O	1.8V or 3.3V LVCMOS	BF19	HVIO_6B (1.8 or 3.3V)
C24	GND	Power	-	-	
C25	GND	Power	-	-	
C26	LA27_P	I/O	1.8V or 3.3V LVCMOS	BK22	HVIO_6B (1.8 or 3.3V)
C27	LA27_N	I/O	1.8V or 3.3V LVCMOS	BM19	HVIO_6B (1.8 or 3.3V)
C28	GND	Power	-	-	
C29	GND	Power	-	-	
C30	FMC_SCL	I/O	-	CD134	HVIO_5A (3.3V)
C31	FMC_SDA	I/O	-	CD135	HVIO_5A (3.3V)
C32	GND	Power	-	-	
C33	GND	Power	-	-	
C34	GND	Power	-	-	
C35	+12V_FMC	Power	-	-	
C36	GND	Power	-	-	
C37	+12V_FMC	Power	-	-	
C38	GND	Power	-	-	

Pin	Schematic Signal	Type	Standard	FPGA Pin	Notes
C39	+3.3V_FMC	Power	-	-	
C40	GND	Power	-	-	
D1	PG_C2M_3V3	Power	-	-	
D2	GND	Power	-	-	
D3	GND	Power	-	-	
D4	GBTCLK0_M2C_P	I	LVDS	AV16	REFCLK_GTSR4B_CH1P
D5	GBTCLK0_M2C_N	I	LVDS	AV21	REFCLK_GTSR4B_CH1N
D6	GND	Power	-	-	
D7	GND	Power	-	-	
D8	LA01_CC_P	I/O	1.8V or 3.3V LVCMOS	D8	HVIO_6C (1.8 or 3.3V)
D9	LA01_CC_N	I/O	1.8V or 3.3V LVCMOS	K8	HVIO_6C (1.8 or 3.3V)
D10	GND	Power	-		
D11	LA05_P	I/O	1.8V or 3.3V LVCMOS	A20	HVIO_6D (1.8 or 3.3V)
D12	LA05_N	I/O	1.8V or 3.3V LVCMOS	A17	HVIO_6D (1.8 or 3.3V)
D13	GND	Power	-		
D14	LA09_P	I/O	1.8V or 3.3V LVCMOS	A23	HVIO_6D (1.8 or 3.3V)
D15	LA09_N	I/O	1.8V or 3.3V LVCMOS	B20	HVIO_6D (1.8 or 3.3V)
D16	GND	Power	-		
D17	LA13_P	I/O	1.8V or 3.3V LVCMOS	B23	HVIO_6D (1.8 or 3.3V)
D18	LA13_N	I/O	1.8V or 3.3V LVCMOS	B26	HVIO_6D (1.8 or 3.3V)
D19	GND	Power	-		
D20	LA17_P	I/O	1.8V or 3.3V LVCMOS	B30	HVIO_6D (1.8 or 3.3V)
D21	LA17_N	I/O	1.8V or 3.3V LVCMOS	A30	HVIO_6D (1.8 or 3.3V)
D22	GND	Power	-		
D23	LA23_P	I/O	1.8V or 3.3V LVCMOS	A35	HVIO_6D (1.8 or 3.3V)
D24	LA23_N	I/O	1.8V or 3.3V LVCMOS	A33	HVIO_6D (1.8 or 3.3V)
D25	GND	Power	-		
D26	LA26_P	I/O	1.8V or 3.3V LVCMOS	BU19	HVIO_6B (1.8 or 3.3V)
D27	LA26_N	I/O	1.8V or 3.3V LVCMOS	BR19	HVIO_6B (1.8 or 3.3V)
D28	GND	Power	-	-	
D29	N/C	-	-	-	
D30	N/C	-	-	-	
D31	N/C	-	-	-	
D32	+3.3V	Power	-	-	
D33	N/C	-	-	-	
D34	N/C	-	-	-	
D35	GND	Power	-	-	
D36	+3.3V_FMC	Power	-	-	
D37	GND	Power	-	-	
D38	+3.3V_FMC	Power	-	-	
D39	GND	Power	-	-	
D40	+3.3V_FMC	Power	-	-	
E1	GND	Power	-	-	
E2	HA01_CC_P	I/O	LVDS or 1.2V LVCMOS	BR49	HSIO_2B_B (1.3V) – R160 [1]
E3	HA01_CC_N	I/O	LVDS or 1.2V LVCMOS	BU49	HSIO_2B_B (1.3V) – R161 [1]
E4	GND	Power	-	-	
E5	GND	Power	-	-	
E6	HA05_P	I/O	LVDS or 1.2V LVCMOS	CC52	HSIO_2B_B (1.3V) – R164 [1]

Pin	Schematic Signal	Type	Standard	FPGA Pin	Notes
E7	HA05_N	I/O	LVDS or 1.2V LVCMOS	CA52	HSIO_2B_B (1.3V) – R165 [1]
E8	GND	Power	-	-	
E9	HA09_P	I/O	LVDS or 1.2V LVCMOS	CF52	HSIO_2B_B (1.3V) – R172 [1]
E10	HA09_N	I/O	LVDS or 1.2V LVCMOS	CH52	HSIO_2B_B (1.3V) – R174 [1]
E11	GND	Power	-	-	
E12	HA13_P	I/O	LVDS or 1.2V LVCMOS	CL42	HSIO_2B_B (1.3V) – R180 [1]
E13	HA13_N	I/O	LVDS or 1.2V LVCMOS	CK45	HSIO_2B_B (1.3V) – R182 [1]
E14	GND	Power	-	-	
E15	HA16_P	I/O	LVDS or 1.2V LVCMOS	CL51	HSIO_2B_B (1.3V) – R188 [1]
E16	HA16_N	I/O	LVDS or 1.2V LVCMOS	CK54	HSIO_2B_B (1.3V) – R190 [1]
E17	GND	Power	-	-	
E18	HA20_P	I/O	LVDS or 1.2V LVCMOS	CK56	HSIO_2B_B (1.3V) – R196 [1]
E19	HA20_N	I/O	LVDS or 1.2V LVCMOS	CL54	HSIO_2B_B (1.3V) – R198 [1]
E20	GND	Power	-	-	
E21	HB03_P	I/O	LVDS or 1.2V LVCMOS	CH31	HSIO_2B_T (1.3V)
E22	HB03_N	I/O	LVDS or 1.2V LVCMOS	CF31	HSIO_2B_T (1.3V)
E23	GND	Power	-	-	
E24	HB05_P	I/O	LVDS or 1.2V LVCMOS	CK8	HSIO_2B_T (1.3V)
E25	HB05_N	I/O	LVDS or 1.2V LVCMOS	CL6	HSIO_2B_T (1.3V)
E26	GND	Power	-	-	
E27	HB09_P	I/O	LVDS or 1.2V LVCMOS	CK11	HSIO_2B_T (1.3V)
E28	HB09_N	I/O	LVDS or 1.2V LVCMOS	CL8	HSIO_2B_T (1.3V)
E29	GND	Power	-	-	
E30	HB13_P	I/O	LVDS or 1.2V LVCMOS	CL14	HSIO_2B_T (1.3V)
E31	HB13_N	I/O	LVDS or 1.2V LVCMOS	CL11	HSIO_2B_T (1.3V)
E32	GND	Power	-	-	
E33	HB19_P	I/O	LVDS or 1.2V LVCMOS	CK17	HSIO_2B_T (1.3V)
E34	HB19_N	I/O	LVDS or 1.2V LVCMOS	CL17	HSIO_2B_T (1.3V)
E35	GND	Power	-	-	
E36	HB21_P	I/O	LVDS or 1.2V LVCMOS	CL20	HSIO_2B_T (1.3V)
E37	HB21_N	I/O	LVDS or 1.2V LVCMOS	CK20	HSIO_2B_T (1.3V)
E38	GND	Power	-	-	
E39	VADJ	Power	-	-	1.8V, can be changed to +3.3
E40	GND	Power	-	-	
F1	PMC_PG_M2C_3V3	Power	-	-	
F2	GND	Power	-	-	
F3	GND	Power	-	-	
F4	HA00_CC_P	I/O	LVDS or 1.2V LVCMOS	BR49	HSIO_2B_B (1.3V) – R162 [1]
F5	HA00_CC_N	I/O	LVDS or 1.2V LVCMOS	BU49	HSIO_2B_B (1.3V) – R163 [1]
F6	GND	Power	-	-	
F7	HA04_P	I/O	LVDS or 1.2V LVCMOS	CL56	HSIO_2B_B (1.3V) – R167 [1]

Pin	Schematic Signal	Type	Standard	FPGA Pin	Notes
F8	HA04_N	I/O	LVDS or 1.2V LVCMOS	CL60	HSIO_2B_B (1.3V) – R170 [1]
F9	GND	Power	-	-	
F10	HA08_P	I/O	LVDS or 1.2V LVCMOS	CK63	HSIO_2B_B (1.3V) – R175 [1]
F11	HA08_N	I/O	LVDS or 1.2V LVCMOS	CL66	HSIO_2B_B (1.3V) – R178 [1]
F12	GND	Power	-	-	
F13	HA12_P	I/O	LVDS or 1.2V LVCMOS	CK73	HSIO_2B_B (1.3V) – R183 [1]
F14	HA12_N	I/O	LVDS or 1.2V LVCMOS	CL73	HSIO_2B_B (1.3V) – R186 [1]
F15	GND	Power	-	-	
F16	HA15_P	I/O	LVDS or 1.2V LVCMOS	CK66	HSIO_2B_B (1.3V) – R191 [1]
F17	HA15_N	I/O	LVDS or 1.2V LVCMOS	CL70	HSIO_2B_B (1.3V) – R194 [1]
F18	GND	Power	-	-	
F19	HA19_P	I/O	LVDS or 1.2V LVCMOS	BR52	HSIO_2B_B (1.3V) – R199 [1]
F20	HA19_N	I/O	LVDS or 1.2V LVCMOS	BU52	HSIO_2B_B (1.3V) – R202 [1]
F21	GND	Power	-	-	
F22	HB02_P	I/O	LVDS or 1.2V LVCMOS	BE61	HSIO_2B_T (1.3V)
F23	HB02_N	I/O	LVDS or 1.2V LVCMOS	BE57	HSIO_2B_T (1.3V)
F24	GND	Power	-	-	
F25	HB04_P	I/O	LVDS or 1.2V LVCMOS	BM52	HSIO_2B_T (1.3V)
F26	HB04_N	I/O	LVDS or 1.2V LVCMOS	BP52	HSIO_2B_T (1.3V)
F27	GND	Power	-	-	
F28	HB08_P	I/O	LVDS or 1.2V LVCMOS	BH38	HSIO_2B_T (1.3V)
F29	HB08_N	I/O	LVDS or 1.2V LVCMOS	BH41	HSIO_2B_T (1.3V)
F30	GND	Power	-	-	
F31	HB12_P	I/O	LVDS or 1.2V LVCMOS	BP41	HSIO_2B_T (1.3V)
F32	HB12_N	I/O	LVDS or 1.2V LVCMOS	BM41	HSIO_2B_T (1.3V)
F33	GND	Power	-	-	
F34	HB16_P	I/O	LVDS or 1.2V LVCMOS	BK49	HSIO_2B_T (1.3V)
F35	HB16_N	I/O	LVDS or 1.2V LVCMOS	BM49	HSIO_2B_T (1.3V)
F36	GND	Power	-	-	
F37	HB20_P	I/O	LVDS or 1.2V LVCMOS	BH49	HSIO_2B_T (1.3V)
F38	HB20_N	I/O	LVDS or 1.2V LVCMOS	BH52	HSIO_2B_T (1.3V)
F39	GND	Power	-	-	
F40	VADJ	Power	-	-	1.8V, can be changed to +3.3
G1	GND	Power	-	-	
G2	N/C	-	-	-	
G3	N/C	-	-	-	
G4	GND	Power	-	-	
G5	GND	Power	-	-	
G6	LA00_CC_P	I/O	1.8V or 3.3V LVCMOS	BK31	HVIO_6A (1.8 or 3.3V)
G7	LA00_CC_N	I/O	1.8V or 3.3V LVCMOS	BP22	HVIO_6A (1.8 or 3.3V)
G8	GND	Power	-	-	
G9	LA03_P	I/O	1.8V or 3.3V LVCMOS	BU28	HVIO_6A (1.8 or 3.3V)

Pin	Schematic Signal	Type	Standard	FPGA Pin	Notes
G10	LA03_N	I/O	1.8V or 3.3V LVCMOS	BP31	HVIO_6A (1.8 or 3.3V)
G11	GND	Power	-	-	
G12	LA08_P	I/O	1.8V or 3.3V LVCMOS	BR28	HVIO_6A (1.8 or 3.3V)
G13	LA08_N	I/O	1.8V or 3.3V LVCMOS	BR31	HVIO_6A (1.8 or 3.3V)
G14	GND	Power	-	-	
G15	LA12_P	I/O	1.8V or 3.3V LVCMOS	BU31	HVIO_6A (1.8 or 3.3V)
G16	LA12_N	I/O	1.8V or 3.3V LVCMOS	BM28	HVIO_6A (1.8 or 3.3V)
G17	GND	Power	-	-	
G18	LA16_P	I/O	1.8V or 3.3V LVCMOS	BW28	HVIO_6A (1.8 or 3.3V)
G19	LA16_N	I/O	1.8V or 3.3V LVCMOS	BM31	HVIO_6A (1.8 or 3.3V)
G20	GND	Power	-	-	
G21	LA20_P	I/O	1.8V or 3.3V LVCMOS	CH12	HVIO_6A (1.8 or 3.3V)
G22	LA20_N	I/O	1.8V or 3.3V LVCMOS	BU22	HVIO_6A (1.8 or 3.3V)
G23	GND	Power	-	-	
G24	LA22_P	I/O	1.8V or 3.3V LVCMOS	BW19	HVIO_6A (1.8 or 3.3V)
G25	LA22_N	I/O	1.8V or 3.3V LVCMOS	BH28	HVIO_6A (1.8 or 3.3V)
G26	GND	Power	-	-	
G27	LA25_P	I/O	1.8V or 3.3V LVCMOS	BM22	HVIO_6A (1.8 or 3.3V)
G28	LA25_N	I/O	1.8V or 3.3V LVCMOS	CF12	HVIO_6A (1.8 or 3.3V)
G29	GND	Power	-	-	
G30	LA29_P	I/O	1.8V or 3.3V LVCMOS	BK19	HVIO_6A (1.8 or 3.3V)
G31	LA29_N	I/O	1.8V or 3.3V LVCMOS	CF9	HVIO_6A (1.8 or 3.3V)
G32	GND	Power	-	-	
G33	LA31_P	I/O	1.8V or 3.3V LVCMOS	BF21	HVIO_6B (1.8 or 3.3V)
G34	LA31_N	I/O	1.8V or 3.3V LVCMOS	BE21	HVIO_6B (1.8 or 3.3V)
G35	GND	Power	-	-	
G36	LA33_P	I/O	1.8V or 3.3V LVCMOS	BE43	HVIO_6B (1.8 or 3.3V)
G37	LA33_N	I/O	1.8V or 3.3V LVCMOS	BF40	HVIO_6B (1.8 or 3.3V)
G38	GND	Power	-	-	
G39	VADJ	Power	-	-	1.8V, can be changed to +3.3
G40	GND	Power	-	-	
H1	N/C	-	-	-	
H2	FMC_PRSNT_N_3V3	Power	-	-	
H3	GND	Power	-	-	
H4	N/C	-	-	-	
H5	N/C	-	-	-	
H6	GND	Power	-	-	
H7	LA02_P	I/O	1.8V or 3.3V LVCMOS	F27	HVIO_6A (1.8 or 3.3V)
H8	LA02_N	I/O	1.8V or 3.3V LVCMOS	F24	HVIO_6A (1.8 or 3.3V)
H9	GND	Power	-	-	
H10	LA04_P	I/O	1.8V or 3.3V LVCMOS	D24	HVIO_6A (1.8 or 3.3V)
H11	LA04_N	I/O	1.8V or 3.3V LVCMOS	H18	HVIO_6A (1.8 or 3.3V)

Pin	Schematic Signal	Type	Standard	FPGA Pin	Notes
H12	GND	Power	-	-	
H13	LA07_P	I/O	1.8V or 3.3V LVCMOS	D15	HVIO_6A (1.8 or 3.3V)
H14	LA07_N	I/O	1.8V or 3.3V LVCMOS	F18	HVIO_6A (1.8 or 3.3V)
H15	GND	Power	-	-	
H16	LA11_P	I/O	1.8V or 3.3V LVCMOS	F15	HVIO_6A (1.8 or 3.3V)
H17	LA11_N	I/O	1.8V or 3.3V LVCMOS	D8	HVIO_6A (1.8 or 3.3V)
H18	GND	Power	-	-	
H19	LA15_P	I/O	1.8V or 3.3V LVCMOS	C2	HVIO_6A (1.8 or 3.3V)
H20	LA15_N	I/O	1.8V or 3.3V LVCMOS	D4	HVIO_6A (1.8 or 3.3V)
H21	GND	Power	-	-	
H22	LA19_P	I/O	1.8V or 3.3V LVCMOS	F4	HVIO_6A (1.8 or 3.3V)
H23	LA19_N	I/O	1.8V or 3.3V LVCMOS	K4	HVIO_6A (1.8 or 3.3V)
H24	GND	Power	-	-	
H25	LA21_P	I/O	1.8V or 3.3V LVCMOS	G2	HVIO_6A (1.8 or 3.3V)
H26	LA21_N	I/O	1.8V or 3.3V LVCMOS	J2	HVIO_6A (1.8 or 3.3V)
H27	GND	Power	-	-	
H28	LA24_P	I/O	1.8V or 3.3V LVCMOS	J1	HVIO_6A (1.8 or 3.3V)
H29	LA24_N	I/O	1.8V or 3.3V LVCMOS	G1	HVIO_6A (1.8 or 3.3V)
H30	GND	Power	-	-	
H31	LA28_P	I/O	1.8V or 3.3V LVCMOS	A8	HVIO_6B (1.8 or 3.3V)
H32	LA28_N	I/O	1.8V or 3.3V LVCMOS	B4	HVIO_6B (1.8 or 3.3V)
H33	GND	Power	-	-	
H34	LA30_P	I/O	1.8V or 3.3V LVCMOS	A11	HVIO_6B (1.8 or 3.3V)
H35	LA30_N	I/O	1.8V or 3.3V LVCMOS	B11	HVIO_6B (1.8 or 3.3V)
H36	GND	Power	-	-	
H37	LA32_P	I/O	1.8V or 3.3V LVCMOS	B14	HVIO_6B (1.8 or 3.3V)
H38	LA32_N	I/O	1.8V or 3.3V LVCMOS	A14	HVIO_6B (1.8 or 3.3V)
H39	GND	Power	-	-	
H40	VADJ	Power	-	1.8V	1.8V, can be changed to +3.3
J1	GND	Power	-	-	
J2	N/C	-	-	-	
J3	N/C	-	-	-	
J4	GND	Power	-	-	
J5	GND	Power	-	-	
J6	HA03_P	I/O	LVDS or 1.2V LVCMOS	CA38	HSIO_2B_B (1.3V) – R165 [1]
J7	HA03_N	I/O	LVDS or 1.2V LVCMOS	BW38	HSIO_2B_B (1.3V) – R168 [1]
J8	GND	Power	-	-	
J9	HA07_P	I/O	LVDS or 1.2V LVCMOS	BR38	HSIO_2B_B (1.3V) – R173 [1]
J10	HA07_N	I/O	LVDS or 1.2V LVCMOS	BU38	HSIO_2B_B (1.3V) – R176 [1]
J11	GND	Power	-	-	
J12	HA11_P	I/O	LVDS or 1.2V LVCMOS	BR41	HSIO_2B_B (1.3V) – R181 [1]

Pin	Schematic Signal	Type	Standard	FPGA Pin	Notes
J13	HA11_N	I/O	LVDS or 1.2V LVCMOS	BU41	HSIO_2B_B (1.3V) – R184 [1]
J14	GND	Power	-	-	
J15	HA14_P	I/O	LVDS or 1.2V LVCMOS	BW49	HSIO_2B_B (1.3V) – R189 [1]
J16	HA14_N	I/O	LVDS or 1.2V LVCMOS	CA49	HSIO_2B_B (1.3V) – R192 [1]
J17	GND	Power	-	-	
J18	HA18_P	I/O	LVDS or 1.2V LVCMOS	CH41	HSIO_2B_B (1.3V) – R197 [1]
J19	HA18_N	I/O	LVDS or 1.2V LVCMOS	CF41	HSIO_2B_B (1.3V) – R200 [1]
J20	GND	Power	-	-	
J21	HA22_P	I/O	LVDS or 1.2V LVCMOS	CK48	HSIO_2B_B (1.3V) – R204 [1]
J22	HA22_N	I/O	LVDS or 1.2V LVCMOS	CL45	HSIO_2B_B (1.3V) – R205 [1]
J23	GND	Power	-	-	
J24	HB01_P	I/O	LVDS or 1.2V LVCMOS	CF19	HSIO_2B_T (1.3V)
J25	HB01_N	I/O	LVDS or 1.2V LVCMOS	CC19	HSIO_2B_T (1.3V)
J26	GND	Power	-	-	
J27	HB07_P	I/O	LVDS or 1.2V LVCMOS	CF22	HSIO_2B_T (1.3V)
J28	HB07_N	I/O	LVDS or 1.2V LVCMOS	CH22	HSIO_2B_T (1.3V)
J29	GND	Power	-	-	
J30	HB11_P	I/O	LVDS or 1.2V LVCMOS	CC22	HSIO_2B_T (1.3V)
J31	HB11_N	I/O	LVDS or 1.2V LVCMOS	CA22	HSIO_2B_T (1.3V)
J32	GND	Power	-	-	
J33	HB15_P	I/O	LVDS or 1.2V LVCMOS	CF28	HSIO_2B_T (1.3V)
J34	HB15_N	I/O	LVDS or 1.2V LVCMOS	CC28	HSIO_2B_T (1.3V)
J35	GND	Power	-	-	
J36	HB18_P	I/O	LVDS or 1.2V LVCMOS	CA31	HSIO_2B_T (1.3V)
J37	HB18_N	I/O	LVDS or 1.2V LVCMOS	CC31	HSIO_2B_T (1.3V)
J38	GND	Power	-	-	
J39	FMC_VIO_B_M2C	Power	-	-	
J40	GND	Power	-	-	
K1	N/C	-	-	-	
K2	GND	Power	-	-	
K3	GND	Power	-	-	
K4	N/C	-	-	-	
K5	N/C	-	-	-	
K6	GND	Power	-	-	
K7	HA02_P	I/O	LVDS or 1.2V LVCMOS	CK30	HSIO_2B_B (1.3V) – R169 [1]
K8	HA02_N	I/O	LVDS or 1.2V LVCMOS	CL26	HSIO_2B_B (1.3V) – R171 [1]
K9	GND	Power	-	-	
K10	HA06_P	I/O	LVDS or 1.2V LVCMOS	CK33	HSIO_2B_B (1.3V) – R177 [1]
K11	HA06_N	I/O	LVDS or 1.2V LVCMOS	CL30	HSIO_2B_B (1.3V) – R179 [1]
K12	GND	Power	-	-	
K13	HA10_P	I/O	LVDS or 1.2V LVCMOS	CK35	HSIO_2B_B (1.3V) – R185 [1]
K14	HA10_N	I/O	LVDS or 1.2V LVCMOS	CL35	HSIO_2B_B (1.3V) – R187 [1]

Pin	Schematic Signal	Type	Standard	FPGA Pin	Notes
K15	GND	Power	-	-	
K16	HA17_CC_P	I/O	LVDS or 1.2V LVCMOS	CF49	HSIO_2B_B (1.3V) – R193 [1]
K17	HA17_CC_N	I/O	LVDS or 1.2V LVCMOS	CH49	HSIO_2B_B (1.3V) – R195 [1]
K18	GND	Power	-	-	
K19	HA21_P	I/O	LVDS or 1.2V LVCMOS	CK39	HSIO_2B_B (1.3V) – R201 [1]
K20	HA21_N	I/O	LVDS or 1.2V LVCMOS	CL39	HSIO_2B_B (1.3V) – R203 [1]
K21	GND	Power	-	-	
K22	HA23_P	I/O	LVDS or 1.2V LVCMOS	CK48	HSIO_2B_B (1.3V) – R206 [1]
K23	HA23_N	I/O	LVDS or 1.2V LVCMOS	CL45	HSIO_2B_B (1.3V) – R207 [1]
K24	GND	Power	-	-	
K25	HB00_CC_P	I/O	LVDS or 1.2V LVCMOS	BF68	HSIO_2B_T (1.3V)
K26	HB00_CC_N	I/O	LVDS or 1.2V LVCMOS	BE68	HSIO_2B_T (1.3V)
K27	GND	Power	-	-	
K28	HB06_CC_P	I/O	LVDS or 1.2V LVCMOS	BK38	HSIO_2B_T (1.3V)
K29	HB06_CC_N	I/O	LVDS or 1.2V LVCMOS	BM38	HSIO_2B_T (1.3V)
K30	GND	Power	-	-	
K31	HB10_P	I/O	LVDS or 1.2V LVCMOS	BE46	HSIO_2B_T (1.3V)
K32	HB10_N	I/O	LVDS or 1.2V LVCMOS	BF46	HSIO_2B_T (1.3V)
K33	GND	Power	-	-	
K34	HB14_P	I/O	LVDS or 1.2V LVCMOS	BF50	HSIO_2B_T (1.3V)
K35	HB14_N	I/O	LVDS or 1.2V LVCMOS	BE50	HSIO_2B_T (1.3V)
K36	GND	Power	-	-	
K37	HB17_P	I/O	LVDS or 1.2V LVCMOS	BF57	HSIO_2B_T (1.3V)
K38	HB17_N	I/O	LVDS or 1.2V LVCMOS	BF53	HSIO_2B_T (1.3V)
K39	GND	Power	-	-	
K40	FMC_VIO_B_M2C	Power	-	-	

Note that many of these signals are pin-muxed in the CPU and may be available for a variety of functions.

1. The HA signals are not connected from the FMC connector (J1) to the SoC by default. 0-ohm 0402 jumpers must be installed in the respective designator location to make a connection.

10/100/1000 Ethernet Interface – J3

The MitySBC-A5E provides an RJ-45 connection for a Gigabit 10/100/1000 Ethernet connection. This connection follows standard TIA/EIA-568B pin-out as shown in Table 10 below. By default, the Ethernet PHY will auto-negotiate with its link partner. The J3 connector corresponds to EMAC1 on the SoC. The reset signal for the PHY associated with J3 is gated by ETH1_RESETN and HPS_COLD_nRESET which are tied to FPGA pins F127 and CH109 respectively.

Table 10: J3 Ethernet RJ45 Pin Assignments

Pin	Signal	Type	Notes
1	TXVA_P	I/O	
2	TXVA_N	I/O	
3	TXVB_P	I/O	
4	TXVB_N	I/O	
5	TXVC_P	I/O	
6	TXVC_N	I/O	
7	TXVD_P	I/O	
8	TXVD_N	I/O	

Table 11: EMAC1 Signal Connections

Signal	Type	FPGA Pin	Notes
EMAC1_RXD0	I	V127	
EMAC1_RXD1	I	AB132	
EMAC1_RXD2	I	T124	
EMAC1_RXD3	I	P124	
EMAC1_RX_CLK	I	D132	
EMAC1_RX_CTL	I	AG123	
EMAC1_TXD0	O	B134	
EMAC1_TXD1	O	AA135	
EMAC1_TXD2	O	T127	
EMAC1_TXD3	O	Y132	
EMAC1_TX_CLK	O	E135	
EMAC1_TX_CTL	O	F132	
I2C_EMAC1_SDA	I/O	H127	
I2C_EMAC1_SCL	O	AB124	

10/100/1000/2500 Ethernet Interface – J18

The MitySBC-A5E provides an RJ-45 connection for a 2.5 Gigabit 10/100/1000/2500 Ethernet connection. This connection follows standard TIA/EIA-568B pin-out as shown in Table 12 below. By default, the Ethernet PHY will auto-negotiate with its link partner. The J18 connector corresponds to SGMII on the SoC.

Table 12: J18 Ethernet RJ45 Pin Assignments

Pin	Signal	Type	Notes
1	TXVA_P	I/O	
2	TXVA_N	I/O	
3	TXVB_P	I/O	
4	TXVB_N	I/O	
5	TXVC_P	I/O	
6	TXVC_N	I/O	
7	TXVD_P	I/O	
8	TXVD_N	I/O	

Table 13: EMAC1 Signal Connections

Signal	Type	FPGA Pin	Notes
SGMII_RX_P	I	AK135	
SGMII_RX_N	I	AK133	
SGMII_TX_P	O	AL129	
SGMII_TX_N	O	AL126	
I2C_EMAC0_SDA	I/O	F124	
I2C_EMAC0_SCL	O	D124	
ETH2_RESETN_3V3	O	CF128	

JTAG Interface – J9

Table 14 lists the connections to the JTAG interface connector.

Table 14: J9 JTAG Pin Assignments

Pin	Schematic Signal	Type	Standard	FPGA Pin	Notes
1	TCK	I	1.8V LVCMOS	CA109	
2	GND	Power	-	-	
3	TDO	O	1.8V LVCMOS	BW109	
4	+1.8V	Power	-	-	
5	TMS	I	1.8V LVCMOS	CA112	
6	NC	-	-	-	
7	NC	-	-	-	
8	NC	-	-	-	
9	TDI	I	1.8V LVCMOS	BW112	
10	GND	Power	-	-	

Fan Header Interface – J24

This header interfaces with the SoC cooling fan. Table 15 lists the connections to the fan header interface.

Table 15: J24 Fan Header Pin Assignments

Pin	Schematic Signal	Type	FPGA Pin	Notes
1	GND	Power	-	
2	+12VIN	Power	-	
3	SENSE	I	BF120	12V Tolerant
4	CONTROL	O	B39	Open Drain

External Battery Headers – J22 and J23

The J23 header provides the option of providing an external VCCBAT or using the on board 1.8V to supply the SoC. To supply VCCBAT with the on board +1.8V supply, jump pins 1 and 2 of J23. To supply VCCBAT with an external battery connect the battery to J22 and jump pins 2 and 3 of J23. The external VCCBAT is connected to the J22 header. Table 16 lists the pinout of the J22 connector and Table 17 lists the pinout for J23.

Table 16: J22 External Battery Pin Assignments

Pin	Schematic Signal	Type	FPGA Pin	Notes
1	GND	Power	-	This is the pin closest to the J22 silk screen designator
2	EXT_BAT	Power	-	Battery voltage should be within 1.0-1.8V

Table 17: J23 VCCBAT Select Pin Assignments

Pin	Schematic Signal	Type	FPGA Pin	Notes
1	+1.8V	Power	-	This is the pin closest to the A5E processor
2	VCCBAT	Power	BD86	
3	EXT_BAT	Power	-	

External I3C Header – J19

The J19 header provides an external I3C bus that is connected to the SoC. Table 18 lists the pinout for this header.

Table 18: J22 External Battery Pin Assignments

Pin	Schematic Signal	Type	Standard	FPGA Pin	Notes
1	+1.8V	Power	-	-	This is the pin closest to the A5E processor
2	I3C0_SDA	I/O	1.8V LVCMOS	K124	
3	I3C0_SCL	O	1.8V LVCMOS	Y127	
4	GND	Power	-	-	

USB Serial Interface – J21

The J21 header provides an external serial interface that is connected to a UART channel of the SoC. The J21 connector is a MicroUSB Type B receptacle. This interface uses UART1 which corresponds to pins AB127 (RX) and M124 (TX).

QSFP Interface – J6

The pinout for the J6 connector is listed in Table 19 below.

Table 19: J6 QSFP Pin Assignments

Pin	Schematic Signal	Type	FPGA Pin	Notes
A1	GND	Power	-	
A2	QSFP_TX1_N	O	BT129	
A3	QSFP_TX1_P	O	BT126	
A4	GND	Power	-	
A5	QSFP_TX3_N	O	BG126	
A6	QSFP_TX3_P	O	BG129	
A7	GND	Power	-	
A8	MODELSELN_3V3	O	BW118	
A9	RESETN_3V3	O	CL128	
A10	ZQSFP_VCCR	Power	-	
A11	I3C1_SCL_3V3	O	AK120	
A12	I3C1_SDA_3V3	I/O	N135	
A13	GND	Power	-	
A14	QSFP_RX2_P	I	BN135	
A15	QSFP_RX2_N	I	BN133	
A16	GND	Power	-	
A17	QSFP_RX0_P	I	BF135	
A18	QSFP_RX0_N	I	BF133	
A19	GND	Power	-	
B20	GND	Power	-	
B21	QSFP_RX1_N	I	BJ133	
B22	QSFP_RX1_P	I	BJ135	
B23	GND	Power	-	
B24	QSFP_RX3_N	I	BV133	
B25	QSFP_RX3_P	I	BV135	
B26	GND	Power	-	
B27	MODPRSN_3V3	I/O	CL130	
B28	INTN_3V3	I/O	CK128	
B29	ZQSFP_VCCT	Power	-	
B30	ZQSFP_VCC	Power	-	
B31	LPMODE_3V3	O	CK125	
B32	GND	Power	-	
B33	QSFP_TX2_P	O	BL129	
B34	QSFP_TX2_N	O	BL126	
B35	GND	Power	-	
B36	QSFP_TX0_P	O	BY129	
B37	QSFP_TX0_N	O	BY126	
B38	GND	Power	-	

M.2 NVME/PCIe Interface – J15

The pinout for the J15 connector is listed in Table 20 below. Note that any unlisted pins are N/C.

Table 20: J15 M.2 PCIe Interface Pin Assignments

Pin	Schematic Signal	Type	FPGA Pin	Notes
1	GND	Power	-	
2	+3.3V	Power	-	
3	GND	Power	-	
4	+3.3V	Power	-	
5	PCIe_RX3_N	I	BD133	
7	PCIe_RX3_P	I	BD135	
9	GND	Power	-	
10	DISK_LED_OD	I	-	
11	PCIe_TX3_N	O	AW126	
12	+3.3V	Power	-	
13	PCIe_TX3_P	O	AW129	
14	+3.3V	Power	-	
15	GND	Power	-	
16	+3.3V	Power	-	
17	PCIe_RX2_N	I	BB133	
18	+3.3V	Power	-	
19	PCIe_RX2_P	I	BB135	
21	GND	Power	-	
23	PCIe_TX2_N	O	BA126	
25	PCIe_TX2_P	O	BA129	
27	GND	Power	-	
29	PCIe_RX1_N	I	AY133	
31	PCIe_RX1_P	I	AY135	
33	GND	Power	-	
35	PCIe_TX1_N	O	BC126	
37	PCIe_TX1_P	O	BC129	
39	GND	Power	-	
40	I3C1_SCL	O	AK120	R117[1]
41	PCIe_RX0_N	I	AV133	
42	I3C1_SDA	I/O	N135	R116[1]
43	PCIe_RX0_P	I	AV135	
45	GND	Power	-	
47	PCIe_TX0_N	O	BE126	
49	PCIe_TX0_P	O	BE129	
50	PCIE1_PERSTn_3V3	O	CH132	
51	GND	Power	-	
52	GND	Power	-	
53	PCIe_CLK_N	O	AV115	
54	PCIE1_WAKEn_3V3	O	CF118	
55	PCIe_CLK_P	O	AV120	
57	GND	Power	-	
61	+3.3V	Power	-	
62	+3.3V	Power	-	
63	GND	Power	-	
64	+3.3V	Power	-	
65	GND	Power	-	
66	+3.3V	Power	-	
67	GND	Power	-	

1. The I2C is not connected from the M.2 NVME connector (J15) to the SoC by default. 0-ohm 0603 jumpers must be installed in the respective designator location to make a connection.

HPS LPDDR4 Interface – U15

The pinout for the HPS LPDDR4 is listed in Table 21 below.

Table 21: U15 HPS LPDDR4 Interface Signals

Schematic Signal	Type	FPGA Pin	Notes
HPS_MEM_RESET_N	O	AG111	
Byte 0			
HPS_DQ0	I/O	B128	
HPS_DQ1	I/O	A128	
HPS_DQ2	I/O	B130	
HPS_DQ3	I/O	A130	
HPS_DQ4	I/O	B116	
HPS_DQ5	I/O	A116	
HPS_DQ6	I/O	B113	
HPS_DQ7	I/O	A113	
HPS_DQS0_T	O	B122	
HPS_DQS0_C	O	A125	
HPS_DMI0	O	B119	
Byte 1			
HPS_DQ8	I/O	F117	
HPS_DQ9	I/O	H117	
HPS_DQ10	I/O	K117	
HPS_DQ11	I/O	M117	
HPS_DQ12	I/O	H108	
HPS_DQ13	I/O	F108	
HPS_DQ14	I/O	M108	
HPS_DQ15	I/O	K108	
HPS_DQS1_T	O	F114	
HPS_DQS1_C	O	D114	
HPS_DMI1	O	F105	
Byte 2			
HPS_DQ16	I/O	H98	
HPS_DQ17	I/O	F98	
HPS_DQ18	I/O	M98	
HPS_DQ19	I/O	K98	
HPS_DQ20	I/O	K87	
HPS_DQ21	I/O	M87	
HPS_DQ22	I/O	F84	
HPS_DQ23	I/O	D84	
HPS_DQS2_T	O	F95	
HPS_DQS2_C	O	D95	
HPS_DMI2	O	H87	
Byte 3			
HPS_DQ24	I/O	A106	
HPS_DQ25	I/O	B103	
HPS_DQ26	I/O	B106	
HPS_DQ27	I/O	A110	
HPS_DQ28	I/O	B91	
HPS_DQ29	I/O	A94	
HPS_DQ30	I/O	B88	
HPS_DQ31	I/O	A91	
HPS_DQS3_T	O	A101	
HPS_DQS3_C	O	B101	
HPS_DMI3	O	B97	
Address Control			
HPS_CS0	O	T105	
HPS_CS1	O	P105	
HPS_CA0	O	T114	

Schematic Signal	Type	FPGA Pin	Notes
HPS_CA1	O	P114	
HPS_CA2	O	V117	
HPS_CA3	O	T117	
HPS_CA4	O	M114	
HPS_CA5	O	K114	
HPS_CKE0	O	V108	
HPS_CKE1	O	T108	
HPS_CK_T	O	AK107	
HPS_CK_C	O	AK104	
HPS_CLKIN_P	I	M105	
HPS_CLKIN_N	I	K105	

FPGA LPDDR4 Interface – U16

The pinout for the FPGA LPDDR4 is listed in Table 22 below.

Table 22: U16 FPGA LPDDR4 Interface Signals

Schematic Signal	Type	FPGA Pin	Notes
FPGA_MEM_RESET_N	O	BH92	
Byte 0			
FPGA_DQ0	I/O	CL91	
FPGA_DQ1	I/O	CK94	
FPGA_DQ2	I/O	CK97	
FPGA_DQ3	I/O	CL97	
FPGA_DQ4	I/O	CK80	
FPGA_DQ5	I/O	CL82	
FPGA_DQ6	I/O	CK76	
FPGA_DQ7	I/O	CL76	
FPGA_DQS0_T	O	CL88	
FPGA_DQS0_C	O	CK88	
FPGA_DMI0	O	CK85	
Byte 1			
FPGA_DQ8	I/O	CC92	
FPGA_DQ9	I/O	CA92	
FPGA_DQ10	I/O	CF92	
FPGA_DQ11	I/O	CH92	
FPGA_DQ12	I/O	CA81	
FPGA_DQ13	I/O	CC81	
FPGA_DQ14	I/O	CH78	
FPGA_DQ15	I/O	CF78	
FPGA_DQS1_T	O	CH89	
FPGA_DQS1_C	O	CF89	
FPGA_DMI1	O	CF81	
Byte 2			
FPGA_DQ16	I/O	BR69	
FPGA_DQ17	I/O	BU69	
FPGA_DQ18	I/O	BR71	
FPGA_DQ19	I/O	BU71	
FPGA_DQ20	I/O	BU59	
FPGA_DQ21	I/O	BR59	
FPGA_DQ22	I/O	BW59	
FPGA_DQ23	I/O	CA59	
FPGA_DQS2_T	O	BW69	
FPGA_DQS2_C	O	CA69	
FPGA_DMI2	O	BU62	
Byte 3			
FPGA_DQ24	I/O	CF71	
FPGA_DQ25	I/O	CH71	
FPGA_DQ26	I/O	CC71	
FPGA_DQ27	I/O	CA71	
FPGA_DQ28	I/O	CF62	
FPGA_DQ29	I/O	CH62	
FPGA_DQ30	I/O	CF59	
FPGA_DQ31	I/O	CH59	
FPGA_DQS3_T	O	CH69	
FPGA_DQS3_C	O	CF69	
FPGA_DMI3	O	CA62	
Address Control			
FPGA_CS0	O	BR78	
FPGA_CS1	O	BU78	
FPGA_CA0	O	BR89	

Schematic Signal	Type	FPGA Pin	Notes
FPGA_CA1	O	BU89	
FPGA_CA2	O	BR92	
FPGA_CA3	O	BU92	
FPGA_CA4	O	BW89	
FPGA_CA5	O	CA89	
FPGA_CKE0	O	BR81	
FPGA_CKE1	O	BU81	
FPGA_CK_T	O	BM81	
FPGA_CK_C	O	BP81	
FPGA_CLKIN_P	I	BW78	
FPGA_CLKIN_N	I	CA78	

MitySBC-A5E CONNECTOR LOCATIONS

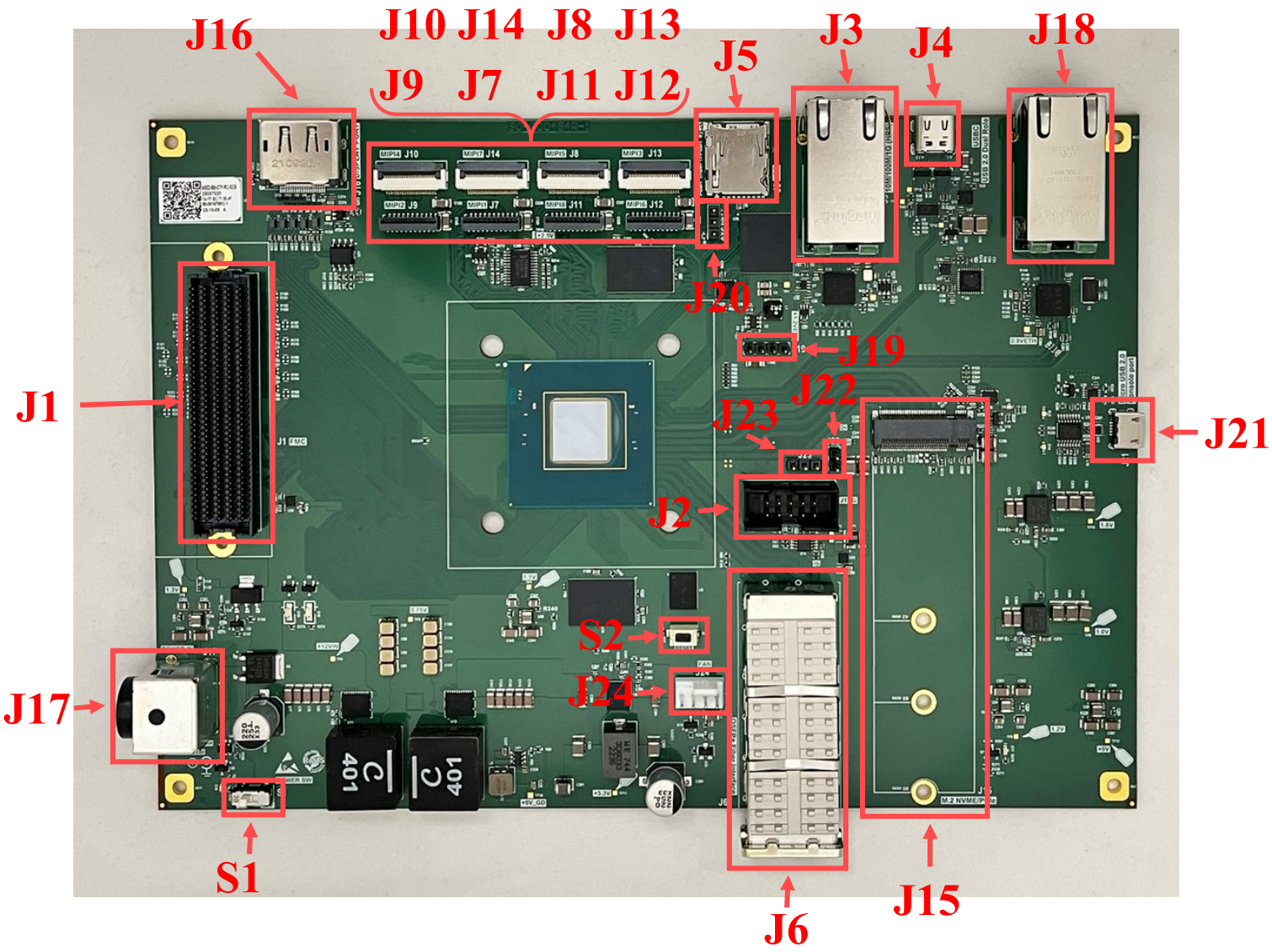

Figure 2: MitySBC-A5E Connector Locations (Top View)

SBC ORDERING INFORMATION

The following table lists the standard MitySBC-A5E configurations. For shipping status, availability, and lead time of these or other configurations please contact Critical Link at info@criticallink.com.

Table 23: Standard Model Numbers

Model	XCVR	Max A76 Speed	FPGA Size	eMMC Flash	FPGA RAM Size	Operating Temp
A5EB-B9-C7F-RC-SBC-X[1]	Yes	1.8GHz	656 KLE's	64GB	8GB	0ºC to +70º C
A5EB-B9-C7F-RC-SBC	Yes	1.8GHz	656 KLE's	64GB	8GB	0ºC to +70º C

1. See *Intel Agilex 5 ES Device Errata and User Guidelines* (document number: 780905) for information about the pre-production silicon.

SBC DEV KIT ORDERING INFORMATION – Not Currently Available

The following table lists the standard MitySBC-A5E dev kit configurations. For shipping status, availability, and lead time of these or other configurations please contact Critical Link at info@criticallink.com.

Table 24: Standard Model Numbers

Model	Module Included	Operating Temp
80-001750	A5EB-B9-C7F-RC-SBC[1]	0ºC to +70º C

1. The included module may or may not be pre-production silicon.

INCLUDED DEV KIT COMPONENTS

The following table lists the components that are included with a MitySBC-A5E. See Table 25 for specific ordering information.

Table 25: Included Items

Description	Interface Port	Qty. Included
MitySBC-A5E	n/a	Qty. 1
TBD	-	-
TBD	-	-
TBD	-	-
TBD	-	-

MECHANICAL INTERFACE DESCRIPTION

Main Board Interface / Mounting

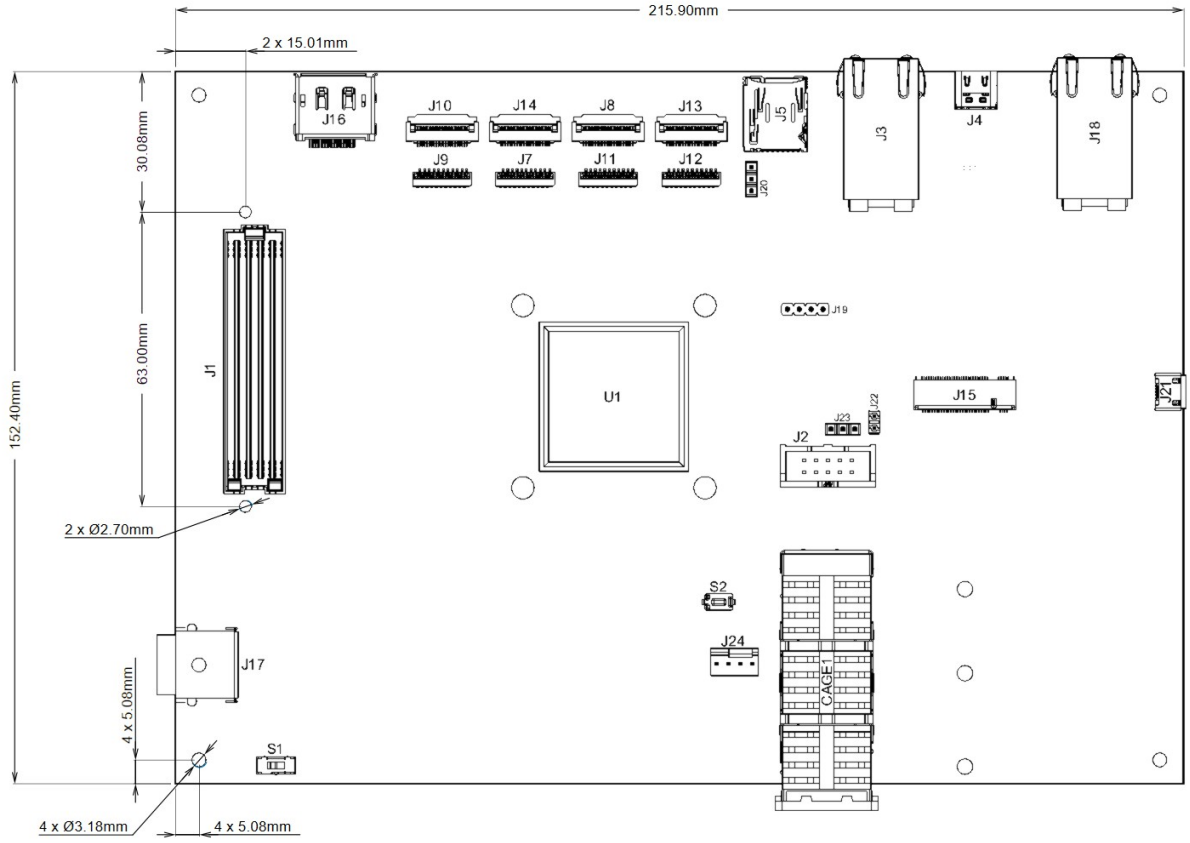

Figure 3: MitySBC-A5E Outline and Mounting Hole Locations (Top View, millimeters)

REVISION HISTORY

Date	Rev	Change Description
013-FEB-2024	A	Initial revision.