FEATURES

- TI OMAP-L138 Dual Core Application Processor
  - **456 MHz (Max) C674x VLIW DSP**
    - Floating Point DSP
    - 32 KB L1 Program Cache
    - 32 KB L1 Data Cache
    - 256 KB L2 cache
    - 1024 KB boot ROM
    - JTAG Emulation/Debug
  - **456 MHz (Max) ARM926EJ-S MPU**
    - 16 KB L1 Program Cache
    - 16 KB L1 Data Cache
    - 8 KB Internal RAM
    - 64 KB boot ROM
    - JTAG Emulation/Debug
- On-Board Xilinx Artix-7 FPGA
  - Up To XC7A50
    - Up To 2,700 KBits Block RAM
    - Up To 8,150 Slices (6 Input LUTs)
  - 1250 Mbps data rate
  - JTAG Interface/Debug
- Up To 256 MB mDDR2 CPU RAM
- Up To 512 MB Parallel NAND FLASH
- Up to 16 MB SPI based NOR FLASH
- Integrated Power Management
- Standard SO-DIMM-200 Interface
  - 96 FPGA User I/O Pins
  - 10/100 EMAC MII / MDIO
  - 2 UARTS
  - 2 McBSPs
  - 2 USB Ports
  - Video Output
  - Camera/Video Input
  - MMC/SD
  - SATA
  - Single 3.3V Power Supply

(actual size)

APPLICATIONS

- Embedded Instrumentation
- Industrial Automation
- Industrial Instrumentation
- Medical Instrumentation
- Embedded Control Processing
- Network Enabled Data Acquisition
- Test and Measurement
- Software Defined Radio
- Bar Code Scanners
- Power Protection Systems
- Portable Data Terminals

BENEFITS

- Rapid Development / Deployment
- Multiple Connectivity and Interface Options
- Rich User Interfaces
- High System Integration
- Fixed & Floating Point Operations in Single CPU
- High Level OS Support
  - Linux
  - QNX 6.4
  - Windows Embedded CE Ready
  - ThreadX Real Time OS
- Embedded Digital Signal Processing

DESCRIPTION

The MityDSP-L138F-A7 is a highly configurable, small form-factor processor card that features a Texas Instruments OMAP-L138 456 MHz (max) Applications Processor (OMAP) tightly integrated with the Xilinx Artix-7 Field Programmable Gate Array (FPGA), FLASH (NAND, and NOR) and mDDR2 RAM memory subsystems. The MityDSP-L138F-A7 is intended to serve as a drop-in replacement for the MityDSP-L138F. The design of the MityDSP-L138F-A7 allows end users the capability to develop programs/logic images for both the OMAP and the FGPA.

The onboard OMAP-L138 processor provides a dual CPU core topology. The OMAP-L138 includes an ARM926EJ-S micro-processor unit (MPU) capable of running the rich software applications programmer interfaces (APIs) expected by modern system designers. The ARM architecture supports several operating systems, including Linux and Windows Embedded CE. In addition to the ARM core, the OMAP-L138 also includes a TMS320C674x floating point digital signal processing (DSP) core. The DSP core supports the freely provided TI DSP/BIOS real-time kernel. Users can leverage the DSP to execute real-time compute algorithms (codecs, image/data processing, compression techniques, filtering, etc.).

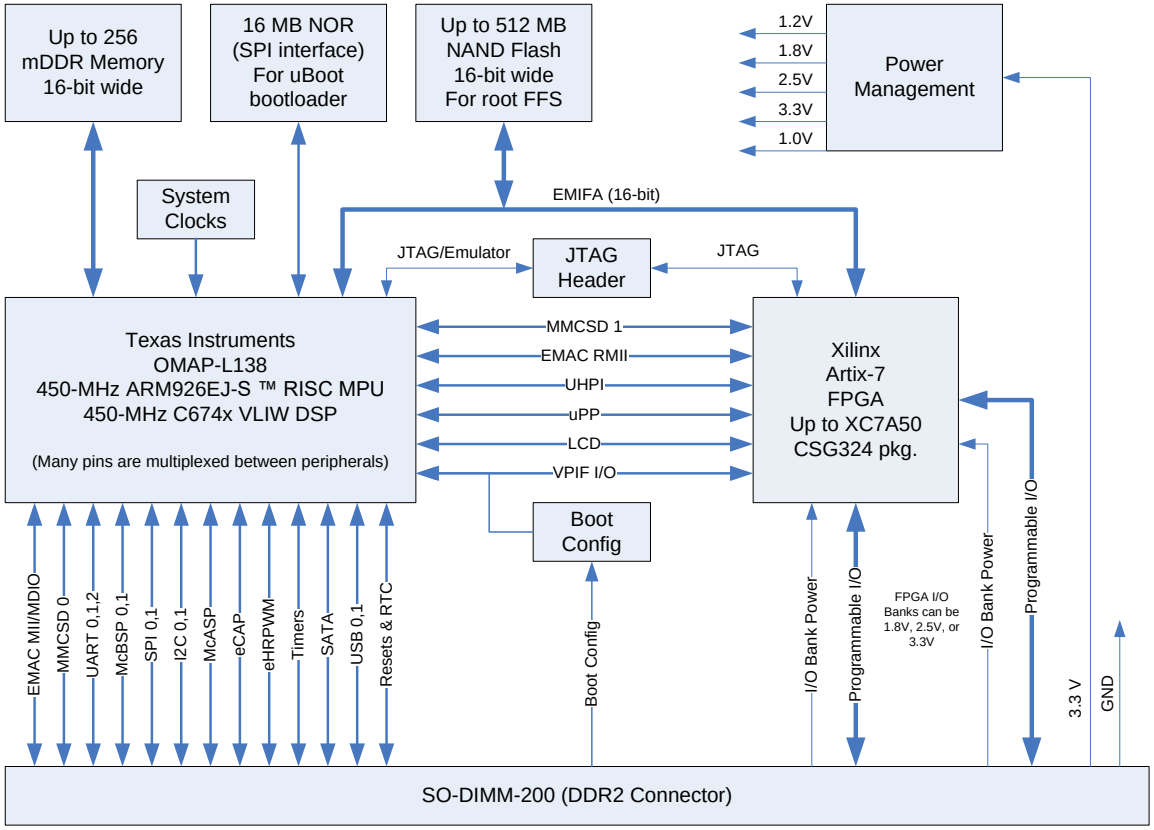

Figure 1 MityDSP-L138F-A7 Block Diagram

Figure 1 provides a top level block diagram of the MityDSP-L138F-A7 processor card. As shown in the figure, the primary interface to the MityDSP-L138F-A7 is through a standard SO-DIMM-200 card edge interface. The interface provides power, synchronous serial connectivity, and up to 96 pins of configurable FPGA I/O for application defined interfacing. Details of the SO-DIMM-200 connector interface are included in the SO-DIMM-200 Interface Description, as shown below.

FPGA Bank I/O

The MityDSP-L138F provides 96 lines of FPGA I/O directly to the SO-DIMM-200 card edge interface. The 96 lines of FPGA I/O are distributed across 2 banks, Bank 15 and Bank 35, of the FPGA. These I/O lines and their associated logic are completely configurable within the FPGA at the end user's discretion.

With the Xilinx Artix-7 series FPGA, up to the XC7A50, each of the user controlled banks may be configured to operate on a different electrical interface standard based on input voltage provided at the card edge connector. The banks support 3.3V, 2.5V, and 1.8V standard CMOS switching level technology.

- The Bank 15 input voltage is provided to Pins 197 and 199
  - Bank 15 FPGA signals are identified as "B15" in Table 1
- The Bank 35 input voltage is provided to Pins 198 and 200
  - Bank 35 FPGA signals are identified as "B35" in Table 1

In addition, the I/O lines from the FPGA have been routed as differential pairs and support higher speed LVDS standards as well as SSTL 1.8/2.5 switching standards. Various forms of termination (pull-up/pull-down, digitally controlled impedance matching) are available within the FPGA switch fabric. Refer to the Xilinx Artix 7 user's guide for more information.

OMAP-L138 mDDR2 Memory Interface

The OMAP-L138 includes a dedicated DDR2 SDRAM memory interface shared between the onboard ARM and DSP cores. The MityDSP-L138F includes up to 256 MB of mDDR2 RAM integrated with the OMAP-L138 processor. The bus interface is capable of burst transfer rates of 600 MB / second. Note that the OSCIN frequency to the OMAP-L138 processor on the module is 24MHz.

OMAP-L138 SPI NOR FLASH Interface

The MityDSP-L138F includes 16 MB of SPI NOR FLASH. This FLASH memory is intended to store a factory provided bootloader, and typically a compressed image of a Linux kernel for the ARM core processor.

EMIFA - FPGA / NAND FLASH Interface

The OMAP-L138 and the Artix-7 FPGA are connected using the DSP Asynchronous External Memory Interface (EMIFA). The EMIFA interface includes 3 chip select spaces. The EMIF interface supports multiple data width transfers and bus wait state configurations based on chip select space. 8, and 16 bit data word sizes may be used. Two of the three chip select lines (CE2, CE3) are reserved for the FPGA interface. The MityDSP-L138F-A7 also includes 4 lines between the FPGA and the OMAP for the purposes of generating interrupt signals.

In addition to the FPGA, up to 512 MB of on-board NAND FLASH memory is connected to the OMAP-L138 using the EMIFA bus. The FLASH memory is 8 bits wide

and is connected to third chip select line of the EMIFA (CE1). The FLASH memory is typically used to store the following types of data:

- ARM Linux / Windows Embedded CE / QNX embedded root file-system
- FPGA application images
- runtime DSP or ARM software
- runtime application data (non-volatile storage)

OMAP-L138 Camera and Video Interfaces

The OMAP-L138 includes an optional video port I/O interface commonly used to drive LCD screens as well as a camera input interface. These interfaces have been routed to the FPGA, which may be routed to the FPGA output pins on the SO-DIMM-200 connector. By routing the video data through the FPGA, additional user customization and/or processing (e.g., overlays of video output, preprocessing or filtering of camera input) may be offloaded from the OMAP-L138 to the FPGA for computation intensive applications.

OMAP-L138 RTC

The OMAP-L138 features an integrated real-time clock, RTC. MityDSP-L138F-A7 modules have a 32.768KHz tuning fork crystal connected to RTC XI & RTC XO of the OMAP-L138 to support the RTC functionality. Additionally there is a battery input, module Pin 35, which will power the RTC when the module is off, if utilized. Please visit our Redmine Wiki pages at support.criticallink.com for additional details about the RTC feature.

Debug Interface

Both the JTAG interface signals for the FPGA and the JTAG and emulator signals for the OMAP-L138 processor have been brought out to a Hirose header that is intended for use with an available breakout adapter, Critical Link part number 80-000286. This header can be removed for production units; please contact Critical Link at info@criticallink.com for details.

This adapter is not included with individual modules but is included with each Critical Link Development Kit that is ordered. Additional adapters are available through Critical Link distribution partners.

Software and Application Development Support

Users of the MityDSP-L138F-A7 are encouraged to develop applications and FPGA firmware using the hardware and software development kit provided by Critical Link. The development kit includes a board support package providing a Linux based distribution and compatible gcc compiler tool-chain with debugger. In addition, the development kit includes support libraries necessary to program the DSP core using the TI Code Composer Studio DSP compiler tool-chain.

To support rapid FPGA and applications development, VHDL components - compatible with the Xilinx Vivado FPGA synthesis tool – for commonly used FPGA designs and a corresponding set of Linux loadable kernel modules and/or DSP interface APIs are included. The libraries provide the necessary functions needed to configure the MityDSP-L138F-A7, program standalone embedded applications, and interface with the various hardware components both on the processor board as well as a custom application carrier card. The libraries include several interface "cores" – FPGA and DSP software modules designed to interface with various high performance data converter modules (ADCs, DACs, LCD and touchscreen interfaces, etc) – as well as bootloading and FLASH programming utilities.

Growth Options

The MityDSP-L138F-A7 has been designed to support several upgrade options. These options include various speed grades, memory configurations, and operating temperature specifications including commercial and industrial temperature ranges. The available options are listed in the section below containing ordering information. For additional ordering information and details regarding these options, or to inquire about a particular configuration not listed below, please contact Critical Link at info@criticallink.com.

ABSOLUTE MAXIMUM RATINGS

Maximum Supply Voltage, Vcc	3.5 V
Storage Temperature Range	-65ºC to 80ºC
Shock, Z-Axis	±10 g
Shock, X/Y-Axis	±10 g

OPERATING CONDITIONS

Ambient Temperature Range Commercial	0ºC to 70ºC
Ambient Temperature Range Industrial	-40ºC to 85ºC
Humidity	0 to 95% Non-condensing
MIL-STD-810F	Contact Critical Link for Details

SO-DIMM-200 Interface Description

The primary interface connector for the MityDSP-L138F-A7 is the SO-DIMM card edge interface which contains 4 types of signals:

- Power (PWR)
- Dedicated signals mapped to the OMAP-L138 device (D)
- Multi-function signals mapped to the OMAP-L138 device (M)
- Dedicated signals mapped to the Xilinx Artix 7 device (F)

Table 1 contains a summary of the MityDSP-L138F pin mapping.

Table 1 SO-DIMM Pin-Out

Pin	Ball	Type	I/O	Signal	Pin	Ball	Type	I/O	Signal
1	-	PWR	-	+3.3 V in	2	-	PWR	-	+3.3 V in
3	-	PWR	-	+3.3 V in	4	-	PWR	-	+3.3 V in
5	-	PWR	-	+3.3 V in	6	-	PWR	-	+3.3 V in
7	-	PWR	-	GND	8	-	PWR	-	GND
9	-	PWR	-	GND	10	-	PWR	-	GND
11	K14	D	I	RESET_IN#	12	-	D		EXT_BOOT#
13	J1	D	O	SATA_TX_P	14	A4	M	I/O	GP0_7
15	J2	D	O	SATA_TX_N	16	A3	M	I/O	GP0_10
17	L1	D	I	SATA_RX_P	18	A2	M	I/O	GP0_11
19	L2	D	I	SATA_RX_N	20	A1	M	I/O	GP0_15
21	P16	D	I	USB0_ID	22	B4	M	I/O	GP0_6
23	P18	D	I/O	USB1_D_N	24	B1	M	I/O	GP0_14
25	P19	D	I/O	USB1_D_P	26	B2	M	I/O	GP0_12
27	N19	D	O	USB0_VBUS	28	B3	M	I/O	GP0_5
29	M18	D	I/O	USB0_D_N	30	C2	M	I/O	GP0_13
31	M19	D	I/O	USB0_D_P	32	C3	M	I/O	GP0_1
33	K18	D	O	USB0_DRVVBUS	34	C4	M	I/O	GP0_4
35	-	D	-	3V RTC Battery	36	C5	M	I/O	GP0_3
37	-	PWR	-	+3.3 V in	38	-	PWR	-	+3.3 V in
39	-	PWR	-	+3.3 V in	40	-	PWR	-	+3.3 V in
41	-	PWR	-	GND	42	-	PWR	-	GND
43	H17	D	I/O	SPI1_MISO	44	D4	M	I/O	GP0_2
45	G17	D	I/O	SPI1_MOSI	46	E4	M	I/O	GP0_0
47	H16	D	I/O	SPI1_ENA	48	F4	M	I/O	GP0_8
49[1]	G19	D	I/O	SPI1_CLK	50	D5	M	I/O	GP0_9
51	F18	M	I/O	SPI1_SCS1	52	A12	M	I/O	MMCSD0_DAT7
53	-	D	I/O	Reserved	54	C11	M	I/O	MMCSD0_DAT6
55[2]	G16	D	I/O	I2C0_SCL	56	E12	M	I/O	MMCSD0_DAT5
57[2]	G18	D	I/O	I2C0_SDA	58	B11	M	I/O	MMCSD0_DAT4
59	F16	M	I/O	UART2_TXD / I2C1_SDA	60	E11	M	I/O	MMCSD0_DAT3
61	F17	M	I/O	UART2_RXD / I2C1_SCL	62	C10	M	I/O	MMCSD0_DAT2
63	-	PWR	I/O	GND	64	-	PWR	I/O	GND
65	F19	M	I/O	UART1_TXD	66	A11	M	I/O	MMCSD0_DAT1
67	E18	M	I/O	UART1_RXD	68	B10	M	I/O	MMCSD0_DAT0
69	E16	M	I/O	MDIO_CLK	70	A10	M	I/O	MMCSD0_CMD

Pin	Ball	Type	I/O	Signal	Pin	Ball	Type	I/O	Signal
71	D17	M	I/O	MDIO_DAT	72	E9	M	I/O	MMCSD0_CLK
73	D19	M	I/O	MII_RXCLK	74	D3	M	I/O	MII_TXCLK
75	C17	M	I/O	MII_RXDV	76	E3	M	I/O	MII_TXD3
77	D16	M	I/O	MII_RXD0	78	E2	M	I/O	MII_TXD2
79	E17	M	I/O	MII_RXD1	80	E1	M	I/O	MII_TXD1
81	D18	M	I/O	MII_RXD2	82	F3	M	I/O	MII_TXD0
83	C19	M	I/O	MII_RXD3	84	C1	M	I/O	MII_TXEN
85	-	PWR	-	GND	86	-	PWR	-	GND
87	C18	M	I/O	MII_CRS	88	D1	M	I/O	MII_COL
89	C16	M	I/O	MII_RXER	90[4]	-	-	-	NO CONNECT
91	J17	F	I/O	B15_47_P.J17	92	K13	F	I/O	B15_48_P.K13
93	J18	F	I/O	B15_47_N.J18	94	J13	F	I/O	B15_48_N.J13
95	H17	F	I/O	B15_45_P.H17	96	H14	F	I/O	B15_46_P.H14
97	G17	F	I/O	B15_45_N.G17	98	G14	F	I/O	B15_46_N.G14
99	G18	F	I/O	B15_43_P.G18	100	H16	F	I/O[3]	B15_44_P.H16
101	F18	F	I/O	B15_43_N.F18	102	G16	F	I/O[3]	B15_44_N.G16
103	K15	F	I/O	B15_41_P.K15	104	F13	F	I/O	B15_42_P.F13
105	J15	F	I/O	B15_41_N.J15	106	F14	F	I/O	B15_42_N.F14
107	-	PWR	-	GND	108	-	PWR	-	GND
109	J14	F	I/O	B15_39_P.J14	110	F15	F	I/O[4]	B15_40_P.F15
111	H15	F	I/O	B15_39_N.H15	112	F16	F	I/O[4]	B15_40_N.F16
113	E18	F	I/O	B15_37_P.E18	114	E15	F	I/O[4]	B15_38_P.E15
115	D18	F	I/O	B15_37_N.D18	116	E16	F	I/O[4]	B15_38_N.E16
117	E17	F	I/O	B15_35_P.E17	118	C16	F	I/O	B15_36_P.C16
119	D17	F	I/O	B15_35_N.D17	120	C17	F	I/O	B15_36_N.C17
121	B18	F	I/O	B15_33_P.B18	122	B16	F	I/O	B15_34_P.B16
123	A18	F	I/O	B15_33_N.A18	124	B17	F	I/O	B15_34_N.B17
125	D15	F	I/O[3]	B15_31_P.D15	126	D14	F	I/O	B15_32_P.D14
127	C15	F	I/O[3]	B15_31_N.C15	128	C14	F	I/O	B15_32_N.C14
129	-	PWR	-	GND	130	-	PWR	-	GND
131	A15	F	I/O	B15_29_P.A15	132	B13	F	I/O	B15_30_P.B13
133	A16	F	I/O	B15_29_N.A16	134	B14	F	I/O	B15_30_N.B14
135	A13	F	I/O	B15_27_P.A13	136	C12	F	I/O	B15_28_P.C12
137	A14	F	I/O	B15_27_N.A14	138	B12	F	I/O	B15_28_N.B12
139	B11	F	I/O	B15_25_P.B11	140	D12	F	I/O	B15_26_P.D12
141	A11	F	I/O	B15_25_N.A11	142	D13	F	I/O	B15_26_N.D13
143	E6	F	I/O	B35_23_P.E6	144	H6	F	I/O	B35_24_P.H6
145	E5	F	I/O	B35_23_N.E5	146	H5	F	I/O	B35_24_N.H5
147	C6	F	I/O	B35_21_P.C6	148	E7	F	I/O	B35_22_P.E7
149	C5	F	I/O	B35_21_N.C5	150	D7	F	I/O	B35_22_N.D7
151	-	PWR	-	GND	152	-	PWR	-	GND
153	B7	F	I/O	B35_19_P.B7	154	D8	F	I/O	B35_20_P.D8
155	B6	F	I/O	B35_19_N.B6	156	C7	F	I/O	B35_20_N.C7
157	A6	F	I/O	B35_17_P.A6	158	G6	F	I/O	B35_18_P.G6
159	A5	F	I/O	B35_17_N.A5	160	F6	F	I/O	B35_18_N.F6
161	A4	F	I/O	B35_15_P.A4	162	G4	F	I/O	B35_16_P.G4
163	A3	F	I/O	B35_15_N.A3	164	G3	F	I/O	B35_16_N.G3
165	B1	F	I/O	B35_13_P.B1	166	D5	F	I/O[4]	B35_14_P.D5
167	A1	F	I/O	B35_13_N.A1	168	D4	F	I/O[4]	B35_14_N.D4
169	C2	F	I/O	B35_11_P.C2	170	C4	F	I/O	B35_12_P.C4
171	C1	F	I/O	B35_11_N.C1	172	B4	F	I/O	B35_12_N.B4

Pin	Ball	Type	I/O	Signal	Pin	Ball	Type	I/O	Signal
173	-	PWR	-	GND	174	-	PWR	-	GND
175	F1	F	I/O	B35_9_P.F1	176	E3	F	I/O[3]	B35_10_P.E3
177	E1	F	I/O	B35_9_N.E1	178	D3	F	I/O[3]	B35_10_N.D3
179	E2	F	I/O[4]	B35_7_P.E2	180	B3	F	I/O	B35_8_P.B3
181	D2	F	I/O[4]	B35_7_N.D2	182	B2	F	I/O	B35_8_N.B2
183	F4	F	I/O[3]	B35_5_P.F4	184	H2	F	I/O	B35_6_P.H2
185	F3	F	I/O[3]	B35_5_N.F3	186	G2	F	I/O	B35_6_N.G2
187	H1	F	I/O	B35_3_P.H1	188	J4	F	I/O	B35_4_P.J4
189	G1	F	I/O	B35_3_N.G1	190	H4	F	I/O	B35_4_N.H4
191	K2	F	I/O	B35_1_P.K2	192	J3	F	I/O	B35_2_P.J3
193	K1	F	I/O	B35_1_N.K1	194	J2	F	I/O	B35_2_N.J2
195	-	PWR	-	GND	196	-	PWR	-	GND
197	-	PWR	-	VCCO_15	198	-	PWR	-	VCCO_35
199	-	PWR	-	VCCO_15	200	-	PWR	-	VCCO_35

Note 1: Pin 49, SPI1_CLK, has a 100K Ohm pull-down resistor on the module
Note 2: Pins 55 and 57 have 4.70K pull-up resistors on the module
Note 3: Pins are dual function Multi-Region Clock Capable input pins (MRCC)
Note 4: Pins are dual function Single-Region Clock Capable input pins (SRCC)

The signal group description for the above pins is included in Table 2.

Table 2 Signal Group Description

Signal / Group	I/O	Description
3.3 V in	N/A	3.3 volt input power referenced to GND.
EXT_BOOT#	I	Bootstrap configuration pin. Pull low to configure booting from external UART1.
RESET_IN#	I	Manual Reset. When pulled to GND for a minimum of 1 usec, resets the DSP processor.
SPI_XXXX	I/O	The pins with an SPI_ prefix are direct connections to the OMAP-L138 pins supporting the SPI1 interface. The SPI1_CLK, SPI1_ENA, SPI1_MISO, SPI1_MOSI pins must remain configured for the SPI function in order to support interfacing to the on-board SPI boot ROM. For details please refer to the OMAP-L138 processor specifications.
MII_XXXX	I/O	The pins with an MII_ prefix are direct connections to the OMAP-L138 pins supporting the media independent interface (MII) function. The MII pins provide multiplex capability and may alternately be used as UART, GPIO, and SPI control pins. For details please refer to the OMAP-L138 processor specification.
MDIO_XX	I/O	The MDIO_CLK and MDIO_DAT signals are direct connects to the corresponding MDIO signals on the OMAP-L138 processor. These pins may be configured for GPIO.
GP0_X	IO	General Purpose / multiplexed pins. These pins are direct connects to the corresponding GP0[X] pins on the OMAP-L138 processor. The include support for the McASP, general purpose I/O, UART flow control, and McBSP 1. For details please refer to the OMAP-L138 processor specifications.
SATA_TX_P/N	O	These pins are direct connects to the OMAP-L138 SATA_TX differential Serial ATA controller pins.
SATA_RX P/N	I	These pins are direct connects to the OMAP-L138 SATA_RX differential Serial ATA controller pins.
GND	N/A	System Digital Ground.
BX_Y_P.ZZ, BX_Y_N.ZZ	IO	FPGA I/O pins. These pins are routed directly to FPGA pins ZZ. The “X” indicates which FPGA bank the pin is allocated. The bank is either 0 or 1. The FPGA fabric supports routing pins in differential pairs, the Y_P and Y_N portion of the name indicates the pair number and polarity. The pins have been routed in pairs with phase matched line lengths.
VCCO_X	I	FPGA Bank interface power input. These pins must

Signal / Group	I/O	Description
		be tied to the desired voltage used for the FPGA Bank 15 or 34 interface pins. Please refer to the VCCO input pin specifications for the Xilinx Artix 7 family of devices for further information. Typical values are 3.3V, 2.5, and 1.8 volts. Each VCCO_X pair should have a 100uF X5R (or better) capacitor place near the pins on the carrier board.
USB0_XXXX, USB1_XXXX	I/O	The USBN_ prefixed pins are direct connects to the corresponding pins on the OMAP-L138 processor. For details please refer to the OMAP-L138 processor specifications.

DEBUG INTERFACE

Below is the pin-out for the Hirose 31 pin header (DF9-31P-1V(32)) that interfaces with an available adapter board, Critical Link part number 80-000286, to debug the OMAP-L138 and FPGA.

Debug Interface Connector Description (J2)

Table 3 OMAP-L138 Hirose Connector

Pin	I/O	Signal	Pin	I/O	Signal
1	-	GND	2	O	OMAP EMU1
3	-	GND	4	O	OMAP EMU0
5	-	GND	6	I	OMAP TCK
7	-	GND	8	O	OMAP RTCK
9	-	GND	10	O	OMAP TDO
11	-	GND	12	-	OMAP VCC / 3.3V
13	-	GND	14	I	OMAP TDI
15	-	GND	16	I	OMAP TRST
17	-	GND	18	I	OMAP TMS
19	-	GND	20	-	GND
21	-	GND	22	O	FPGA VREF / VCCAUX
23	-	GND	24	I	FPGA TMS
25	-	GND	26	I	FPGA TCK
27	-	GND	28	O	FPGA TDO
29	-	GND	30	I	FPGA TDI
31	-	GND			

ELECTRICAL CHARACTERISTICS

Table 4: Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{33}	Voltage supply, 3.3 volt input.		3.2	3.3	3.4	Volts
I_{33}	Quiescent Current draw, 3.3 volt input			340[1,2]	TBS[1,2]	mA
$I_{33\text{-max}}$	Max current draw, positive 3.3 volt input.			TBS[1,2]	2200[1,2]	mA
$V_{3V\_RTC\_Battery}$	Voltage supply, RTC Battery			3.0	5.0V	Volts
$I_{3V\_RTC\_Battery}$	Current, RTC Battery, V_{33} = 0V			10		uA
F_{CPU}	CPU internal clock Frequency (PLL output)		25	300	456	MHz
F_{EMIF}	EMIF bus frequency	Must be ½ CPU	-	100	-	MHz

1. Power utilization of the MityDSP-L138F-A7 is heavily dependent on end-user application. Major factors include: ARM CPU PLL configuration, DSP Utilization, FPGA utilization, and external DDR2 RAM utilization.
2. For power utilization information please visit our product support Wiki pages on support.criticallink.com

ORDERING INFORMATION

The following table lists the standard module configurations. For shipping status, availability, and lead time of these or other configurations please contact Critical Link at info@criticallink.com.

Table 5: Standard Model Numbers

Module P/N	CPU	FPGA	NOR	NAND	RAM	Temperature
L138-FJ-326-RC	456 MHz	XC7A15	16MB	256MB	256MB	0ºC to 70º C
L138-DJ-325-RI	375 MHz	XC7A15	16MB	256MB	128MB	-40ºC to 85º C
L138-FM-336-RL	456 MHz	XC7A50	16MB	512MB	256MB	-40ºC to 70º C
L138-DM-336-RI	375 MHz	XC7A50	16MB	512MB	256MB	-40ºC to 85º C

MECHANICAL INTERFACE

The mechanical outline of the MityDSP-L138F-A7 is illustrated in Figure 2, as shown below.

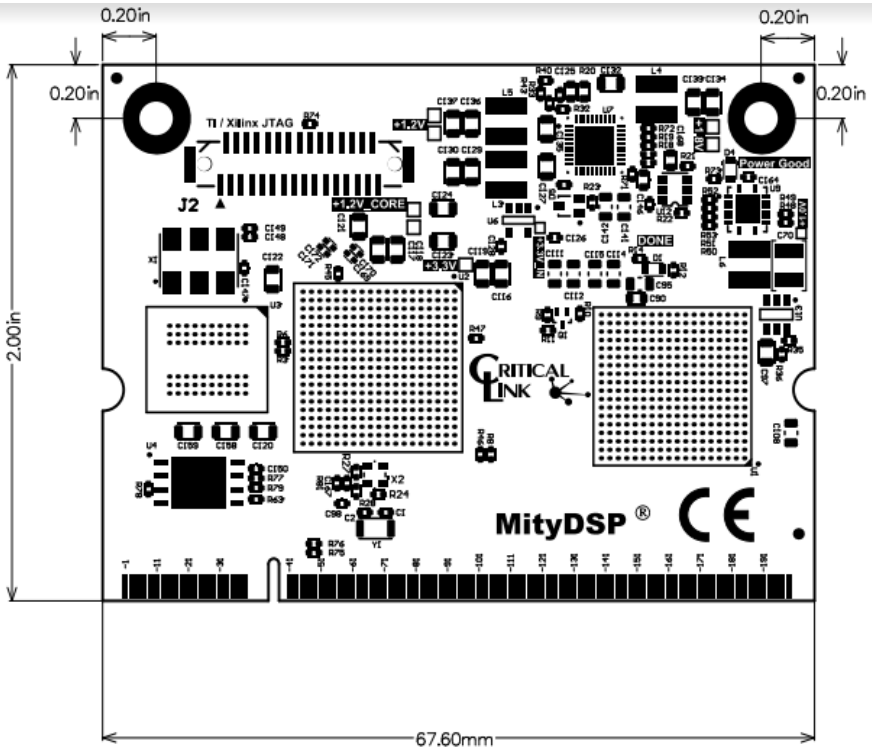

Figure 2 MityDSP-L138F-A7 Mechanical Outline

REVISION HISTORY

Rev	Date	Change Description
-1A	02-DEC-2021	Initial Release