MityCAM-35MMFHDXS EVK

User's Manual

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1 Introduction

The purpose of this document is to detail features of the MityCAM-35MMFHDXS EVK.

1.1 Additional Documentation

In addition to this document, the following documents are also useful / pertinent to the use and operation of the MityCAM-35MMFHDXS cameras.

Table 1: Reference Documentation

Title	Description
35MMFHDXSCA / 35MMFHDXSMA Datasheet	35MMFHDXS_A_DS Sensor Data Sheet https://canon-cmos-sensors.com/
35MMFHDXSCA / 35MMFHDXSMA Application Note	35MMFHDXS_A_AN Application Note. https://canon-cmos-sensors.com/
MityCAM-35MMFHDXS datasheet	Complete specification for MityCAM-35MMFHDXS.
USB3 Vision Standard 1.0.1	See https://www.visiononline.org/vision-standards-details.cfm?type=11
GenTL Viewer User's Manual	Users guide for the Critical Link Supplied GenTL Viewer PC software. https://support.criticallink.com/files/GenTLViewer/GenTLViewer%20Manual.pdf

2 Interfaces

2.1 AIA USB3 Vision

The MityCAM-35MMFHDXS EVK includes a USB 3.1 Gen 1 interface that is compliant with the AIA USB3 Vision standard (U3V). This is the main control and data interface to the camera system. A list of the GenICam registers available for control of the system is included in Section 15 of this document.

Critical Link supplies a free PC application, GenTL Viewer, that may be used to control, capture and save images generated by the evaluation kit. However, this kit should also be compatible with any third-party software that is compliant with the AIA USB3 Vision standard, such as the National Instruments Vision Acquisition Software, HALCON, etc. Figures in this document are captured using the Critical Link provided software. This Software can be downloaded from https://support.criticallink.com/files/GenTLViewer/GenTLViewer_latest_setup.exe

2.2 Power Interface

The MityCAM-35MMFHDXS EVK requires a +12 V input voltage supply. A minimum of 1.0 amps is recommended. See the datasheet for details on the connector.

2.3 USB 2.0 RNDIS Debug

The USB 2.0 port on the MityCAM-35MMFHDXS EVK provides an RNDIS (Ethernet) connection to an attached HOST PC. The port is configured to run a DHCP server and present an Ethernet IP address of 10.1.47.2/8 for the camera and assign an address of 10.1.47.2/8 to the attached HOST PC. The camera supports accessing the embedded Linux shell on the device using the SSH protocol. Using this protocol, it is also possible to transfer files

onto the camera subsystem. There is also a simple web-server running on the camera to support firmware upgrades.

3 Sensor Interface Overview

The sensor interface to the FPGA is illustrated in Figure 1. There are 3 main interface sections: a power supply section, a timing generation section, and the sensor sampling / analog conversion section.

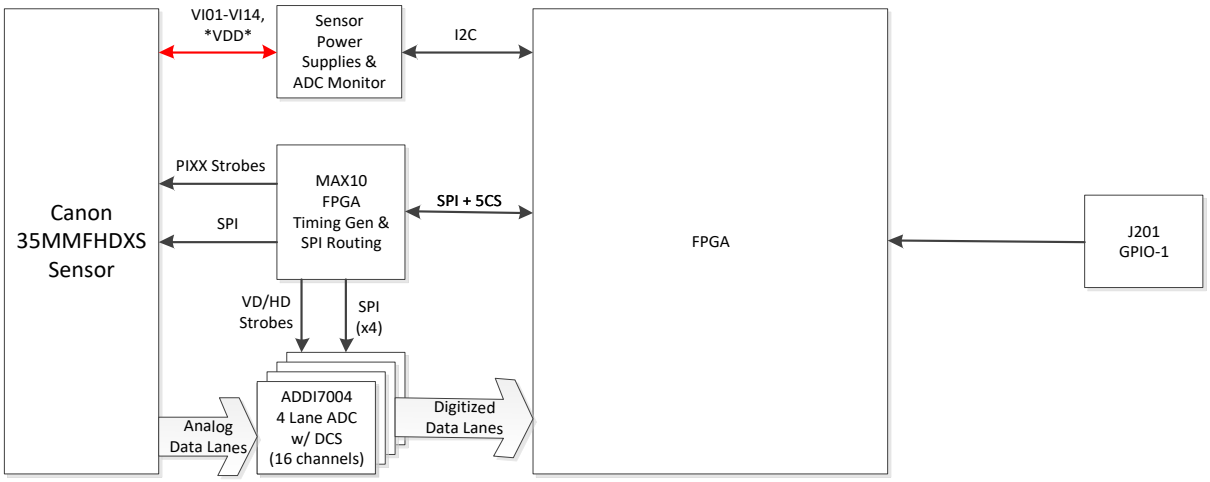

Figure 1 Sensor Connections Relating to Frame Exposure and Timing Control

The EVK includes a full suite of analog supplies to support powering the 35MMFHDXS sensor, and provides the option to externally bias all of the VIXX sensor inputs (via jumper configuration) if desired. In addition, a simple readback ADC has been added to support monitoring all of the sensor supply voltages in the circuit. Please refer to the sensor board schematic for more information on the power supply, sequencing, and jumper configurations.

The timing signal generation logic, driving the sensor PIXX input strobes, is controlled by a local Intel MAX 10 field programmable gate array (FPGA). The FPGA includes a programming timing generator and strobe control circuit and is commanded by the main processing board via a serial peripheral interface (SPI) bus.

For sensor sampling, the EVK utilizes the Analog Devices ADDI7004 Quad-Channel HD Image Signal Processor chipset (4 chips total) to sample the analog outputs of the 35MMFHDXS sensor. The ADDI7004 includes a correlated double sampler (CDS) ADC front end with -3 dB, 0dB, +3 dB and +6 dB gain selections. The ADDI7004 also includes a 6 dB to 42 dB variable gain amplifier section (VGA) prior to a 14 bit analog to digital converter (ADC). In addition, the EVK takes advantage of black level clamping in order to provide consistent background levels across each channel from the sensor. The 14 bit output data can be packed into a 16 bit, 12 bit, or 8 bit output word (most significant bit aligned).

4 Sensor Voltage Biasing

The MityCAM-35MMFHDXS EVK supports various sensor biasing options for the VI01, VI02, …., VI14 sensor input supply voltages. The sensor does provide internal biasing supplies that may be used in place of driving the inputs. The EVK supports 3 biasing modes via the use of jumpers on the sensor board. The modes are:

a. Full External biasing – in this case all VI01, VI02, …, VI14 voltage inputs are supplied via external linear power supplies.
b. **[default]** Internal Biasing with external VI03 (-1.5V) – in this case the sensor is configured to use internal biasing for all VI01, VI02, …, VI14 with the exception of the VI03 voltage rail. This allows use of the sensor internal biasing regulators but still supports long exposure mode of operation.
c. Full internal biasing – in this case the sensor is configured to use internal biasing for all VI01, VI02, … VI14 inputs.

It is recommended that the biasing scheme be left at the default setting (option b, above) unless there is a specific customer need to operate the sensor in a different configuration. Please contact Critical Link or Canon for assistance in this situation.

The jumper settings that control the biasing are listed in the following table. No other jumper configurations are supported. The jumpers should be configured while the kit is unplugged from the power supply. The on-board firmware will properly detect the jumper configuration and program / sequence the sensor accordingly.

Table 2: Jumper Settings

Jumper	Full External	Internal w/ext VI03	Full Internal	Description
JP1	X			Connects 4.5V to VI01
JP2	X			Connects 3.5V to VI02
JP3	X			Connects 2.5V to VI08
JP4	X	X		Connects -1.5V to VI03
JP6	X			Connects 4.5V to VI04
JP7	X			Connects 2.5V to VI09
JP8	X			Connects 0.4V to VI05
JP9	X			Connects 2.5V to VI10
JP10	X			Connects 2.6V to VI06
JP12	X			Connects 1.0V to VI07
JP13	X			Connects 2.5V to VI11
JP14	X			Connects 1.5V to VI12
JP15	X			Connects 4.4V to VI13
JP16	X			Connects 2.0V to VI14
JP17	X			Controls sequencing for external biasing.
JP18	X			Controls sequencing for external biasing.
JP19		X	X	Controls sequencing for internal biasing.
JP20		X	X	Controls sequencing for internal biasing.

Figure 2, Figure 3, and Figure 4 illustrate the jumper settings for each of the supported biasing configurations.

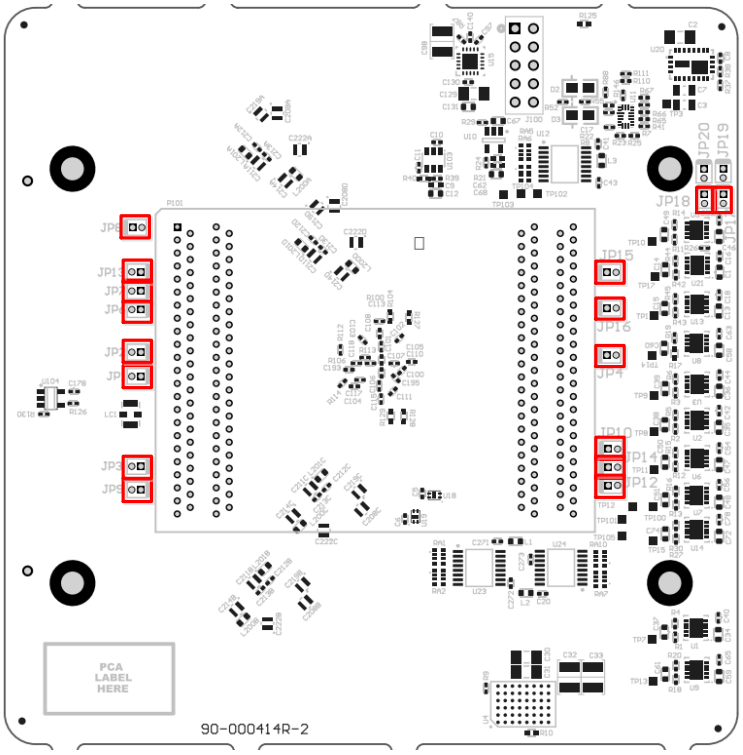

Figure 2 Jumper Selections for Full External Biasing

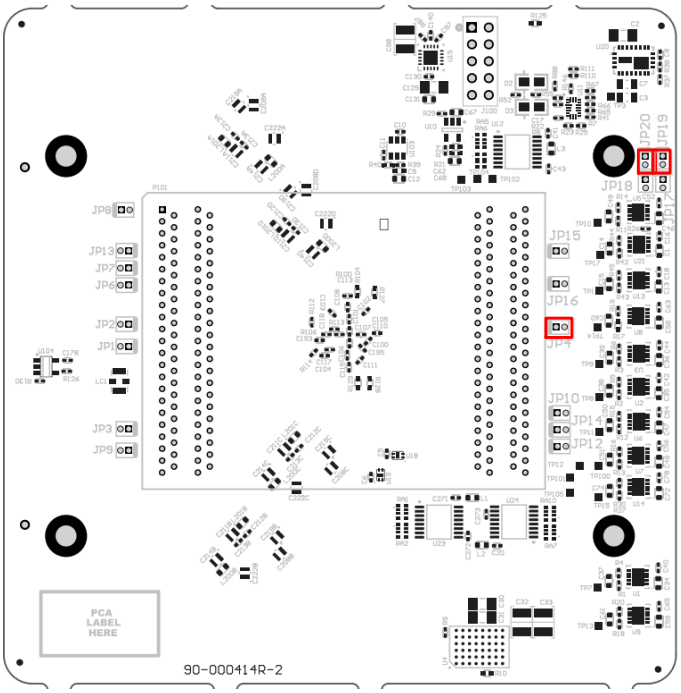

Figure 3 Jumper settings for Default Internal Biasing with External VI03 (-1.5V)

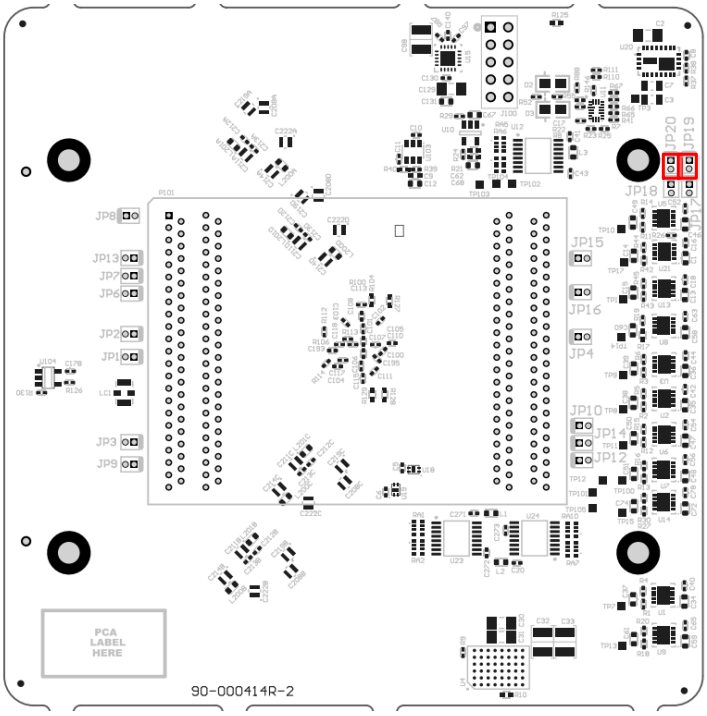

Figure 4 Jumper settings for Full Internal Biasing

5 Analog Chain / Gain and Offset control

The MityCAM-35MMFHDXS EVK uses the ADDI7004 external correlated double sampling (CDS) 14 bit analog to digital converter (ADC) circuit to measure each of the pixels output on the 16 output lanes from the sensor. A block diagram of the analog path to ADC is illustrated in Figure 5. In the figure, there are multiple variable gain stages shown. The default settings for each stage are indicated in bold text. These gain settings may be controlled using the U3V GenICam register interface. The control settings are indicated in the figure.

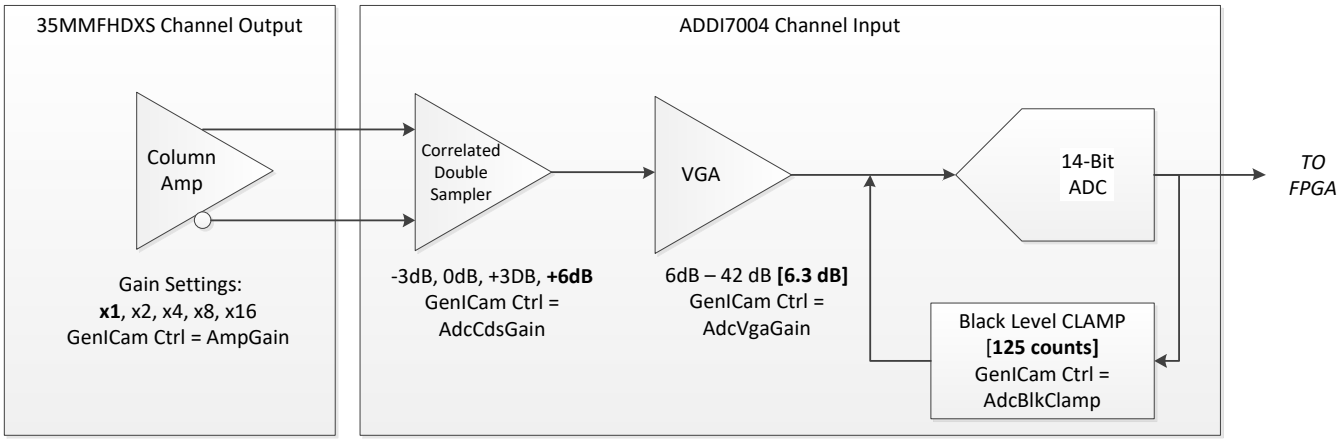

Figure 5 Pixel Analog Gain Path to ADC

Once the 14 bit ADC data is transmitted to the FPGA, the FPGA packs the pixel samples into 8, 12, or 16 bit output words according to Figure 6. The selection of the packing mode allows the user to trade off readout rate vs. available dynamic range of the sensor.

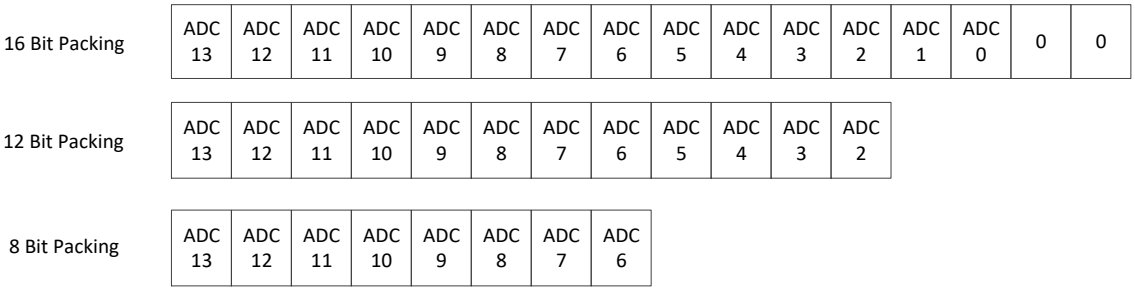

Figure 6 ADC Pixel Data packing into 16, 12, or 8 bit output words

Given the default gain settings and the output swing for a saturated signal for a monochrome revision A sensor, Table 3 outlines the approximate saturation levels expected at the U3V output to the PC. Depending on the desired sensitivity and scaling, the user may desire to adjust the VGA gain levels to set the saturation level for the sensor, or set the Column Amplifier gain higher if working in a low light / noise dominant environment.

Table 3: Approximate Saturation Levels, Monochrome Rev A sensor, Default Settings

Chain Signal Point	Value	Units	Notes
Saturated Pixel (pk-pk)	370	mV	Column Amp Gain = x1, Mono Rev A Datasheet
CDS Output (pk-pk)	738	mV	CDS = 6 dB gain
VGA Output (pk-pk)	1525	mV	VGA = 6.3 dB
ADC Counts	12365	cnts	14 bits, max input = 2000 mV, offset to 125 cnts
16-bit U3V output	49460	cnts	Shift left by 2 bits.
12-bit U3V output	3091	cnts	Shift right by 2 bits.
8-bit U3V output	193	cnts	Shift right by 6 bits.

6 Low Light Operation

Customers desiring to operate the sensor in low light scenarios should consider the following steps:

1. Select 16 bits per pixel mode. This will allow gathering the lowest level signals in the least significant bits of the sensor. Other modes will truncate these bits.
2. Maximize the aperture on the lens where possible. Or select a lens with a larger aperture.
3. Optimize your exposure time. Typically, the exposure time should be set according to the desired frame rate. E.g., for 60 Hz operation, exposure time should be approximately 16 ms (e.g., 1/60 Hz). Other situations may limit exposure time.
4. Adjust the AmpGain GenICam parameter in the Image Format group. On power up, the GenICam AmpGain setting is x1. This can be increased to as high as x16 to increase sensitivity. Increasing the

gain also makes it easier to saturate the ADC, but for typical low light conditions, saturation is not likely. The evaluation kit does not include an autogain function.

5. If necessary, the AdcVGAGain GenICam control may be increased. Increasing this parameter will linearly increase the sensor read noise, however.

Also, users should keep in mind that the GenTL Viewer software package does not perform any significant contrast enhancement techniques beyond a simple gamma correction operator, which could be enabled and adjusted to be less than 1.0 to enhance contrast at low levels. Further image signal processing (ISP) techniques, such as adaptive histogram equalization (AHE) or contrast limited adaptive histogram equalization (CLAHE) will improve image output. Images can be saved by the GenTl Viewer and processed with various opensource tools such as ImageJ to see the advantages of applying such techniques.

7 Black Level Clamping

The MityCAM-35MMFHDXS EVK uses the optical black clamp loop on the ADDI7004 ADC chip to remove residual channel offsets and track low frequency variations in the output black level. The optical black clamping is initialized / updated over the frame by sampling dark pixel data. Three operating regions are defined in the setup according to the list below. For more information, please refer to the ADDI7004 datasheet, or contact Critical Link.

1. The first region ignores the first eight pedestal rows output at the start of the readout pattern. This data is not used or processed by the black level clamping.
2. The second region integrates all pixels along rows 9 through 78 (rows 79 and 80 are not used).
3. The third region integrates the center 40 pixels of the 60 dark column pixels output with each row to generate the black level filter correction value. The active data is black level clamped with the filter outputs.

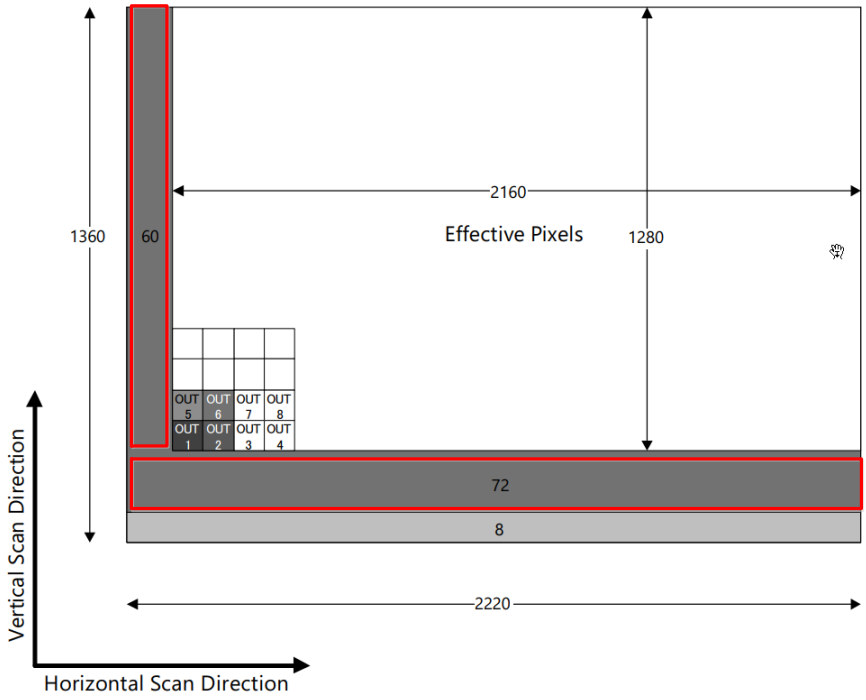

Figure 7 Notional Regions of Pixels use to load the ADDI7004 Optical Black Clamp Filter

8 Frame Interval and Exposure Time

Control of the Frame Interval and Exposure Time can be performed internally on the kit using the GenICam control registers. The block diagram shows how the kit interfaces with the 35MMFHDXS sensor. The FPGA generates the proper PIXX pulses needed by the sensor to operate the camera at a specified frame rate.

8.1 Internal Frame Rate and Internal Exposure

For exposure times less than 200 milliseconds, this mode will use the nominal 98 Hz timing modes extending the frame interval time with additional N / horizontal periods at the end of the readout as required. This is described in the 35MMFHDXS application note. For exposure times greater than 200 milliseconds, the mode will use the long exposure mode as described in the 35MMFHDXS application note. Note: when operating in long exposure mode, the frame interval time will be automatically set to match the exposure time (the exposure time and frame interval time must be the same in this mode). The FPGA configures the timing generation logic in the Max 10 FPGA on the sensor board using the SPI interface such that the PIXX timing and control pins are driven properly to start acquisition. To configure this mode, the following GenICam registers of the camera must be configured as listed:

GenICam Register	Setting
ExposureTime	User Required Exposure Time
AcquisitionFrameRate	User Required Sensor Frame Rate

8.2 Notes on Frame Interval

The maximum frame interval time is defined in the 35MMFHDXS datasheet. For a full ROI, up to 98 Hz may be achieved. For ROIs that are smaller in height, higher frame rates out of the sensor are possible. However, the USB 3.1 Gen 1 interface is limited to approximately 320 MB/sec. Therefore, for a full ROI image at 16 bits per pixel, the maximum continuous frame rate achievable is limited to approximately 60 Hz. For continuous operation, if the requested frame rate is higher than can be achieved, frames will be periodically dropped on the USB output interface. Table 4 lists the maximum readout rates for the different VSKIP settings.

Table 4: Effective Readout Rates for various VSKIP settings

VSKIP Setting	1280x2160	1080x2160	720x2160	360x2160
Sensor Rate 16 bpp	98	114	165	298
Max Rate 16 bpp	48	57	85	168
Max Rate 8 bpp	98	114	165	298

9 Continuous Operation

9.1 USB Output

When the GenICam AcquisitionMode register is set to Continuous and acquisition is started, the camera will configure the sensor to operate at the requested Frame Rate and start transmitting data to the USB 3.1 Gen 1 interface. If the requested data rate exceeds the capability of the USB 3.1 Gen 1 link, the camera will periodically

drop incoming frames prior to transmission to the host PC in order to reduce the latency of the data shown on a host PC display.

10 Burst Mode Operation

10.1 USB 3 Output

The camera has a section of RAM dedicated as a circular image buffer. When the AcquisitionMode GenICam register is set to Single or Multi-Frame, data will be streamed at the configured rate into the image buffer and streamed out at the maximum achievable rate on the USB 3.1 Gen 1 interface, which is approximately 320 MB/sec. The number of frames that can be streamed into the frame buffer is defined by the GenICam FrameCountMax register setting and is a function of the configured ROI.

11 Configurable Region of Interest

The MityCAM-35MMFHDXS supports a single ROI. The sensor vertical skip controls are available via GenICam VSkip register with the options for reading the center 1280x2160, 1080x2160, 720x2160, and 360x2160 pixels from the sensor as described by the 35MMFHDXS application note. Changing the VSkip setting will allow the sensor to be read out faster at the expense of reduced available ROI. Change the Vskip setting will reset the ROI to the maximum output available from the sensor in that mode. The output ROI can be reduced by clipping the sensor readout in the FPGA image pipeline using the GenICam OffsetX, OffsetY, Width, and Height settings. Note: the original of the GenICam register settings is the top-left coordinate of the active sensor readout area.

11.1 USB3 VISION

The base ROI captured from the Sensor and transmitted via the USB3 Vision interface is configured using the GenICam defined Width, Height, OffsetX, and OffsetY registers while the camera is IDLE.

12 Color Processing

The MityCAM-35MMFHDXS EVK currently outputs the RAW bayer RGB data and does not perform demosaicing in the kit hardware. The GenTL Viewer software, however, does support demosaicing the data and white balance operations to support color presentation. See the GenTL Viewer user manual for more details.

13 GPIO Interface

The EVK comes with a breakout cable for the GPIO interface harness. The pin connections are listed in Table 5. P1 is the 12-Pin GPIO connector interface. P2 is the USB Type A interface for Host PC insertion. P3 is the 9 Pin receptacle (female) cable end. P4 is the 9 pin plug (male) cable end.

Table 5: GPIO Break Out Cable Pin Assignments

GPIO Port (P1)	Break Out Cable Port-Pin	Description
1	P3-6	FPGA IO 0 – 1.8V CMOS Logic Level
2	P3-7	FPGA IO 1 – 1.8V CMOS Logic Level
3	P3-8	FPGA IO 2 – 1.8V CMOS Logic Level
4	P3-9	FPGA IO 3 – 1.8V CMOS Logic Level
5	P3-4	Camera shutdown, short to GND to turn off camera, otherwise leave unconnected.
6	P3-5	Ground
7	USB-A Connector, P2	1.8V Serial Console Output
8	USB-A Connector, P2	1.8V Serial Console Input
9	P4-5	Reference / Return for Isolated input currents.
10	P4-6	Opto-isolated Input 0
11	P4-7	Opto-isolated Input 1
12	P4-8	Opto-isolated Input 2

The available modes of operation for the 4 GPIO pins are listed in Table 6.

Table 6: GPIO Modes

#	Mode
1.	Input for reading
2.	Output driven low
3.	Output driven high
4.	Input for external trigger (FPGA IO 0 only)

The following sections will cover Modes 1, 2 and 3. Mode 4 is covered in separate sections.

The Opto-Isolated Input pins may be used as inputs for reading. Input 0 may be used as an optional trigger source in the same way as GPIO 0.

13.1 Input

In the input mode of operation, the pin can be queried for its current logical value (High or Low).

13.2 Output

In output mode, the pin can be driven high or low. This can be used to toggle a light source or some other operation.

14 Firmware Upgrade

The MityCAM-35MMFHDXS EVK allows upgrading the firmware via the network interface. Details for acquiring the firmware and downloading the firmware to the camera are available on the Critical Link MityCAM Support Site.

15 MityCAM 35MMFHDXS GenICam Features

This section presents a summary of the Generic Interface for Cameras (GenICam) available features provided by the camera. Many of the listed features, identified by the SFNC=Y field, are defined by the European Machine Vision Association (EMVA) Standard Features Naming Convention.

15.1 Device Control Group

Feature	Type	SFNC?	Description
DeviceReset	Command	Y	This command is used to reset the device and to put it in its power up state.
DeviceVendorName	StringReg	Y	Name of camera vendor
DeviceModelName	StringReg	Y	Name of the camera model
DeviceManufacturerInfo	StringReg	Y	Manufacturer Info
DeviceVersion	StringReg	Y	Device Version
DeviceSerialNumber	StringReg	Y	Displays the factory set camera serial number.
DeviceFirmwareVersion	StringReg	Y	Firmware Version
DeviceSFNCVersionMajor	Integer	Y	Major version of the Standard Features Naming Convention that was used to create GenICam XML
DeviceSFNCVersionMinor	Integer	Y	Minor version of the Standard Features Naming Convention that was used to create GenICam XML
DeviceSFNCVersionSubMinor	Integer	Y	Sub-Minor version of the Standard Features Naming Convention that was used to create GenICam XML
SoftwareBuildDate	StringReg	N	Build date of the camera software.
FpgaVersion	IntReg	N	Version information of the FPGA.
Fx3Version	StringReg	N	Version information for the FX3.

VoltageSelect	Enumeration	N	This enumeration selects which ADC channel to display in the Voltage Field. The camera includes an ADC monitor of all of the sensor voltages that may be use to check their status. **Allowed Values :** • VI14 • VI13 • VI12 • VI11 • VI10 • VI09 • VI08 • VI07 • VI06 • VI05 • VI04 • VI03 • VI02 • VI01 • NET_1V8ADC • NET_1V8DADC • NET_3V0 • NET_3v3_AVDD3 • NET_3v3ADC • NET_3V0ADC • NET_5V0_AVDD • NET_5V0_SVDD • NET_5V0_DVDD
Voltage	Float	N	The measured voltage at the VoltageSelect Position.

15.2 Image Format Control Group

Feature	Type	SFNC?	Description
OffsetX	Integer	Y	Horizontal offset from the origin to the region of interest (in pixels). **Min Value:**0 **Increment:**4
OffsetY	Integer	Y	Vertical offset from the origin to the region of interest (in pixels). **Min Value:**0 **Increment:**2

SensorWidth	Integer	N	Effective Width of the sensor in pixels.
SensorHeight	IntSwissKnife	N	Effective Height of the sensor in pixels.
Width	Integer	Y	Width of the image provided by the device (in pixels). **Min Value:**32 **Increment:**4
Height	Integer	Y	Height of the image provided by the device (in pixels). **Min Value:**4 **Increment:**2
PixelFormat	Enumeration	Y	Format of the pixels provided by the device. It represents all the information provided by PixelSize, PixelColorFilter combined in a single feature. **Allowed Values :** • Mono16 • Mono12p • Mono8 • BayerRG8 • BayerRG12p
TestPattern	Enumeration	N	Selects the type of test pattern that is generated by the device as image source. **Allowed Values :** • SensorData • ADCTestPattern
AmpGain	Enumeration	N	Controls the programmable column amplifier gain in the sensor. **Allowed Values :** • x1 • x2 • x4 • x8 • x16
VSkip	Enumeration	N	Set the vertical frame size in the sensor. **Allowed Values :** • Height1280 • Height1080 • Height720

			• Height360
BadPixelReplacementEnable	Enumeration	N	This control allows the user to enable or disable the replacement of pixels marked as bad by the system. **Allowed Values :** • On • Off
BadPixelReplacementMap	Enumeration	N	When on, marked bad pixels are set to 0 and non-marked pixels are set to maximum value during image transmission. **Allowed Values :** • On • Off
AdcSelection	Enumeration	N	Select which ADC to configure for CDS/VGA gain and Black clamp. ALL sets all ADCs to same value. **Allowed Values :** • ALL • CH0_A • CH0_B • CH0_C • CH0_D • CH1_A • CH1_B • CH1_C • CH1_D • CH2_A • CH2_B • CH2_C • CH2_D • CH3_A • CH3_B • CH3_C • CH3_D
AdcCdsGain	Enumeration	N	Set CDS Gain in ADC selected by ADC Selection **Allowed Values :** • dBneg3 • dB0 • dB3

			• dB6
AdcVgaGain	Integer	N	Set VGA Gain in ADC selected by ADC Selection. Gain = 6-42dB (5.76 + 0.0359*value) dB **Min Value:**0 **Max Value:**1023
AdcBlkClamp	Integer	N	Set Black clamp in ADC selected by ADC Selection **Min Value:**0 **Max Value:**1023

15.3 Acquisition Control Group

Feature	Type	SFNC?	Description
AcquisitionMode	Enumeration	Y	Sets the acquisition mode of the device. It defines mainly the number of frames to capture during an acquisition and the way the acquisition stops. **Allowed Values :** • Continuous • SingleFrame • MultiFrame
AcquisitionStart	Command	Y	Starts the Acquisition of the device. The number of frames captured is specified by AcquisitionMode.
AcquisitionStop	Command	Y	Stops the Acquisition of the device at the end of the current Frame. It is mainly used when AcquisitionMode is Continuous but can be used in any acquisition mode.
ExposureTime	Float	Y	Exposure duration, in microseconds. This controls the duration where the photosensitive cells are exposed to light. **Min Value:**30.0 **Max Value:**200000000
AcquisitionFrameRate	Converter	Y	Controls the acquisition rate (in Hertz) at which the frames are captured.
AcquisitionFramePeriod	Integer	Y	Period between frames, in microseconds. **Max Value:**20000000 **Increment:**1
AcquisitionFrameCount	Integer	Y	Number of frames to aquire in MultiFrame Acquisition mode. **Min Value:**1 **Increment:**1

FrameCountMax	IntSwissKnife	Y	Maximum AcquisitionFrameCount possible given current payload size
TriggerSelector	Enumeration	Y	Selects the type of trigger to configure. **Allowed Values :** • FrameStart
TriggerMode	Enumeration	N	Controls if the selected trigger is active. External Triggering is not supported. **Allowed Values :** • Off
TriggerActivation	Enumeration	N	Specifies the activation mode of the trigger. **Allowed Values :** • RisingEdge

15.4 Sensor Peek/Poke Group

Feature	Type	SFNC?	Description
RegAddress	Integer	N	Register address of the Peek/Poke **Min Value:**0 **Max Value:**2047 **Increment:**1
RegValue	Integer	N	Value of the address peeked or to be written when poked **Min Value:**0 **Max Value:**268435455 **Increment:**1
ExecRead	Command	N	Command reads and invalidates/replaces the RegValue register with the setting read back from the sensor.
ExecWrite	Command	N	Command writes the value stored in the RegValue register to the sensor at the specified RegAddress location.
DeviceSelect	Enumeration	N	Selects the device that peek/poke will address. **Allowed Values :** • Sensor35MM • ADC0 • ADC1 • ADC2 • ADC3

15.5 Digital IO Control Group

Feature	Type	SFNC?	Description
LineSelector	Enumeration	Y	Selects the physical line (or pin) of the external device connector or the virtual line of the Transport Layer to configure. When a Line is selected, all the other Line features will be applied to its associated I/O control block and will condition the resulting input or output signal. For this case, Line0-3 correspond to High Speed FPGA IO numbers 1-4 on the GPIO connector interface. **Allowed Values :** • Line0 • Line1 • Line2 • Line3
LineMode	Enumeration	Y	Controls if the physical Line is used to Input or Output a signal. When a Line supports input and output mode, the default state is Input to avoid possible electrical contention. **Allowed Values :** • Input • Output • OptoInput
LineSource	Enumeration	Y	Selects which internal acquisition or I/O source signal to output on the selected Line. LineMode must be Output. **Allowed Values :** • Off • ExposureActive • UserOutput0 • UserOutput1
UserOutputSelector	Enumeration	Y	Selects which bit of the User Output register will be set by UserOutputValue. **Allowed Values :** • UserOutput0 • UserOutput1
UserOutputValue	Boolean	Y	Sets the value of the bit selected by UserOutputSelector.
LineStatus	Boolean	Y	Returns the current status of the selected input or output Line. The status of the signal is taken after the input Line inverter of the I/O control block.

15.6 Transport Layer Control Group

Feature	Type	SFNC?	Description
PayloadSize	Integer	Y	Size of payload, in bytes **Min Value:**16 **Max Value:**243927040 **Increment:**1

16 Revision History

Revision	Date	Author	Description
1A	4/28/20	Mike Williamson	Initial Release
1B	7/22/20	Mike Williamson	Add section 6 Low Light Operation.