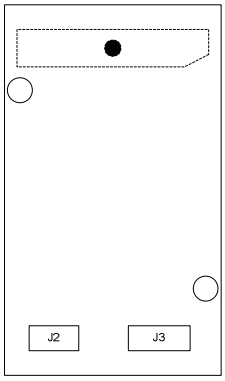
FEATURES

- MDK-8 Interface Form Factor
- 1 Msps maximum sample rate
- 16 Bit Resolution
- +/- 10 Volt Maximum Input Range
- Selectable Input Gain Control
  - 10 V pk-pk Range
  - 5 V pk-pk Range
  - 2 V pk-pk Range
  - 1 V pk-pk Range
- Adjustable Offset
  - –5 to 5 V offset range
- Anti-Alias Filtering
  - 4 Pole Chebychev
  - Sallen-Key
  - 500 KHz 3dB cut-off
  - Can be bypassed
- Internal or External Triggering
- Internal or External Clock Source

APPLICATIONS

- Embedded Signal Processing
- Medical Instrumentation
- Accelerometer Sampling
- CCD Sampling
- Remote Sensing



DESCRIPTION

The MDK8-ADS8239 provides a 16 bit, 1 Msps analog to digital converter with anti-alias filtering in the MityDSP Development Kit 8 (MDK-8) series form factor. The card uses the Texas Instruments ADS8329 converter. The MDK8-ADS8329 is compatible with the MityDSP hardware and software development kit API. Refer to the User's Manual provided with the libraries for further information.

A block diagram of the MDK8-ADS8329 is illustrated in Figure 1. All interface signals available on the ADS8329 chip are routed to the MDK-8 FPGA I/O connector pins for full control by a connected MityDSP. In addition, 2 external pins are routed to the I/O connectors for the purposes of external triggering and ADC clocking. This allows synchronization and/or phase locking to system equipment external to the MDK-MB card/configuration.

The MDK8-ADS8329 uses the available MDK-MB digital to analog converter output in order to generate an offset control signal in the front stage signal conditioning. This provides, effectively, 12 bit gain control over a +/- 5 volt range, or offset adjustment steps of 2.44 millivolts.

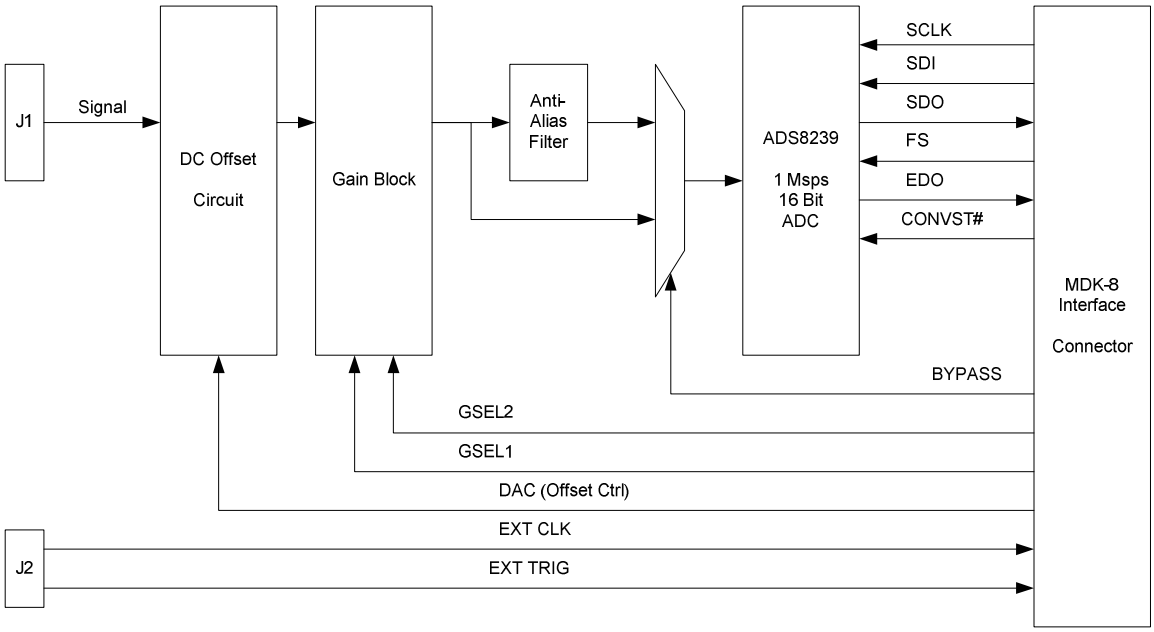


Figure 1 MDK8-ADS8329 Block Diagram

Table 1 DAC Voltage Offset Settings

DAC Setting [cnts]	DAC Voltage [v]	Input DC Offset [v]
0	0	-5
1024	1.024	-2.5
2048	2.048	0
3072	3.072	2.5
4095	4.095	+4.9975

Table 2 Gain Select Control Settings

GSEL2	GSEL1	Linear Voltage Range (following DC offset) [pk-pk]
0	0	10 V
0	1	5
1	0	2
1	1	1

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Storage Temperature Range	-65 to 80C
Shock, Z-Axis	±10 g
Shock, X/Y-Axis	±10 g

OPERATING CONDITIONS

Ambient Temperature Range	0 to 55C
Humidity	0 to 95% Non-condensing
Vibration, Z-Axis	TBS
Vibration, X/Y-Axis	TBS

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Typical	Limit	Units (Limits)
Power Dissipation					
BW_{ADC}	3 DB Bandwidth Anti-Alias Filter	R/C filtering	500	510	KHz (Max)
$V_{Min,ADC-Ext}$	Minimum Analog Input Voltage, External ADC connection.		-10	-10.5	Volts
$V_{Max,ADC-Ext}$	Maximum Analog Input voltage External ADC connection.		10	10.5	Volts
$V_{Min,ADC-DBC}$	Minimum Analog Input Voltage, MDK-8 Daughter Board ADC Interface.		0	-0.1	Volts
$V_{Max,ADC-DBC}$	Minimum Analog Input Voltage, MDK-8 Daughter Board ADC Interface.		4.096	4.1	Volts
Fs_{ADC}	Maximum Sample Rate, ADC		1	1	MHz
R_{input}	Input Impedance		TBD	> 10K	Ohm
SNR	Signal to Noise Ratio	20 KHz input, 1MSPS			dBc
SFDR	Spurious Free Dynamic Range	20 KHz input, 1 MSPS			dB
Notes:					

MDK-8 Socket Interface Description

The bottom connector of the MDK-ADS8329 card uses the required Hirose FX6-50P-0.8SV 50 position socket. The pin assignments for the card are listed in Table 3.

Table 3 MDK-8 Connector Pin Assignments

Pin	Signal	I/O	Pin	Signal	I/O
A1	FS	I	B1	+5 V	-
A2	SCLK	I	B2	+5 V	-
A3	SDI	I	B3	+3.3 V	-
A4	SDO	O	B4	+3.3 V	-
A5	CONVST#	I	B5	+12 VA	-
A6	EOC	O	B6	GND	-
A7	EXT_TRIG	O	B7	GND	-
A8	EXT_CLK	O	B8	GND	-
A9	GSEL1	I	B9	-12 VA	-
A10	GSEL2	I	B10	+15 V	-
A11	BYPASS	I	B11	+15 V	-
A12	Not Used	-	B12	-15 V	-
A13	Not Used	-	B13	-15 V	-
A14	Not Used	-	B14	AGND	-
A15	Not Used	-	B15	AGND	-
A16	Not Used	-	B16	DO_CLK	-
A17	Not Used	-	B17	RSV	-
A18	Not Used	-	B18	RSV	-
A19	Not Used	-	B19	RSV	-
A20	Not Used	-	B20	RSV	-
A21	Not Used	-	B21	RSV	-
A22	Not Used	-	B22	RSV	-
A23	Not Used	-	B23	RSV	-
A24	Not Used	-	B24	RSV	-
A25	Offset Adjust	I	B25	RSV	-

Analog Input Interface Description

The analog input interface to the MDK-ADS8329 uses a locking Molex 2 pin connector on standard 0.100 inch spacing. AMP TBD connectors (or equivalent) should be used with interface cables.

Table 4 J2 Pin Assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	AI	I	2	AGND	-

External Trigger and Clock Source Interface Description

Connector J3 includes TTL compliant inputs for external trigger signals and external clock sources for use by the electrically connected MityDSP FPGA (through the MDK-MB interconnects). The interfaces uses a 4 position locking connect using standard 0.100 inch spacing. AMP TBD connectors (or equivalent) should be used with interface cables.

Table 5 J2 Pin Assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	TRIG_IN	I	2	GND	-
3	CLK_IN	I	4	GND	-

Software API and Supported Modes

The MityDSP software and firmware development kit includes a core interface and C++ API for interfacing to the ADS8329 part. Refer to the MDK Software User's Guide for more information. Use of the on-board MDK-MB TLV5610 DAC API is required in order to properly configure the offset. Use of the GPIO MDK-MB API is required in order to properly configure the gain. Example software is included in the appendix of this specification for configuration of the card.

On-Board Anti-Alias Filtering

A figure of the on-board anti-alias filter frequency response is included in TBS.