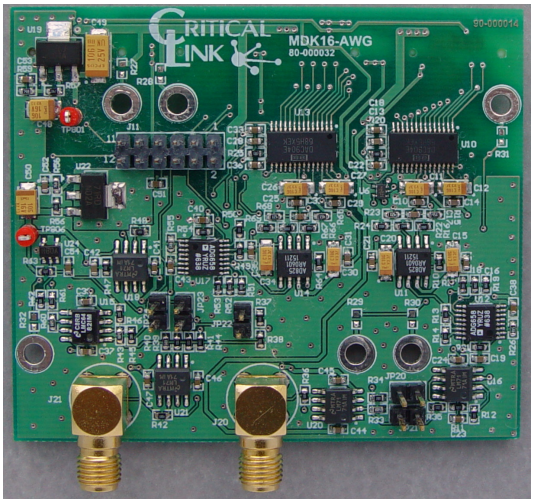
FEATURES

- MDK-16 Interface Form Factor
- Dual DAC Outputs
  - 14 Bit Output
  - 50 Msps Max Clock Rate for Dual Channel Outputs
  - 100 Msps Clock Rate for Single Channel Output
  - Synchronous Clocking
- Optional Output Summing Circuit
- Selectable Output Range
  - 0.5 to 10 V pk-pk Range
- Adjustable Offset
  - –5 to 5 V offset range
- Internal or External Triggering
- Internal or External Clock Source
- 3 General Purpose Inputs
- 1 General Purpose Output

APPLICATIONS

- Laser Modulation
- RF / IF Excitation
- Lock-In Amplifier Design
- Embedded Signal Generators
- Frequency Synthesis



DESCRIPTION

The MDK16-AWG provides dual 14 bit digital to analog converter (DAC) outputs capable of up to 165 Msps output sample rates in the MityDSP Development Kit 8 (MDK-8) series form factor. The card utilizes the Texas Instruments DAC904E converter. The MDK16-AWG is compatible with the MityDSP hardware and software development kit API. Refer to the User's Manual provided with the libraries for further information.

A block diagram of the MDK16-AWG is illustrated in Figure 1. All interface signals available on the DAC904E chips are routed to the MDK16 form factor (two MDK-4 and one MDK-8) FPGA I/O connector pins for full control by a connected MityDSP. The DAC chips share data and clock lines. DAC data is time-division multiplexed between the two channels and the DACs are clocked on opposite edges of the clock. A data update frequency of 100 MHz maximum is recommended. Therefore, dual DAC update rates of 50 Msps and single DAC update rates of 100 Msps are achievable.

In addition, 5 external pins are routed to a digital I/O connector. One of the pins are used for the purposes of external triggering and/or ADC clocking. This allows synchronization and/or phase locking to system equipment external to the MDK-MB card/configuration. The remaining pins provide 3 "slow" (<2 us response time) digital inputs and 1 "fast" (<1 50 ns response time) digital outputs.

The MDK16-AWG uses the available MDK-MB digital to analog converter output in order to generate an offset voltage prior to signal output. The DC offset voltage is common for both DAC outputs. This provides, effectively, 12 bit control over a +/- 5 volt range, or offset adjustment steps of 2.44 millivolts.

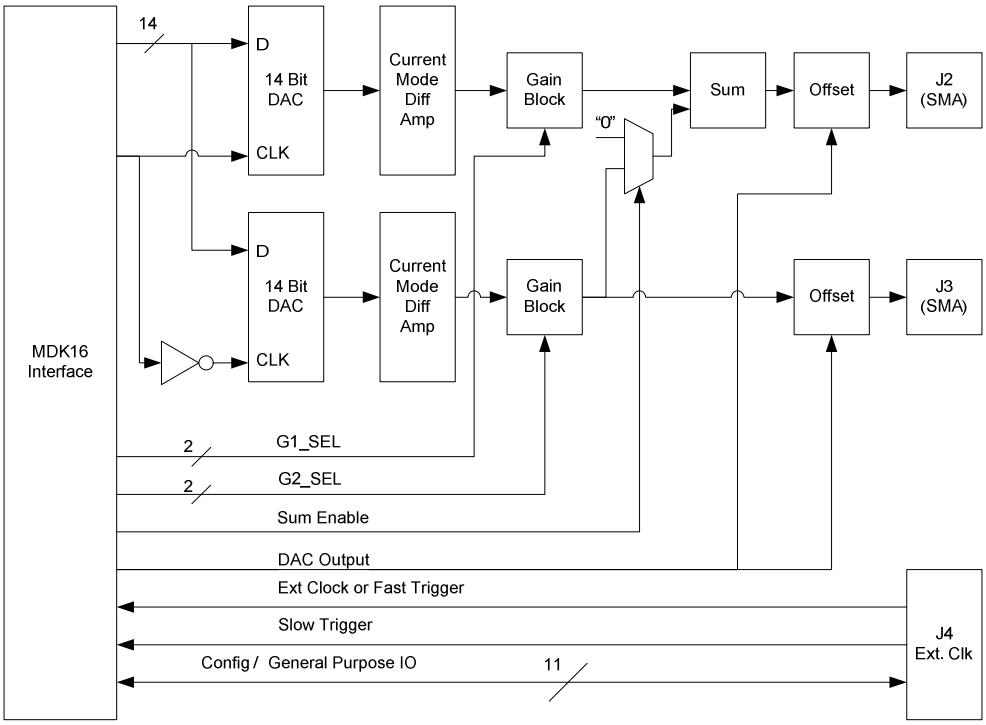


Figure 1 MDK16-AWG Functional Block Diagram

Table 1 describes the typical voltage offsets developed for various MDK-MB DAC settings applied to the MDK16-AWG circuit card. The implementation provides for a low and high gain/output jumper setting via JP TBD for DAC1 and JP TBD for DAC2. Note that only one DAC setting is available for both circuits; an DAC offset of 1024 counts will result in –1 volt for a Low Gain setting on one channel will correspond and a –2.5 Volt setting in the second channel if it is configured for high gain.

Table 1 DAC Voltage Offset Settings

DAC Setting [cnts]	DAC Voltage [v]	Output DC Offset Low Gain Setting [V]	Output DC Offset High Gain Setting [v]
0	0	-2	-5
1024	1.024	-1	-2.5
2048	2.048	0	0
3072	3.072	+1	+2.5
4095	4.095	+1.999	+4.9975

Table 2 describes the gain select settings that must be applied for each of the 2 DAC channels in order to develop a given output voltage range prior to the summing circuit (channel 1) or the offset circuit (channel 2).

Table 2 Gain Select Control Settings

G#_SEL<1>	G#_SEL1<0>	Voltage Range Low Gain Setting [pk-pk]	Voltage Range High Gain Setting [pk-pk]
0	0	0.5 V	1.25 V
0	1	1.0 V	2.5 V
1	0	2.0 V	5 V
1	1	4.0 V	10 V

The MDK16-AWG also includes a summing circuit on channel 1 in order to allow generation of lock-in type modulation signals. The summing circuit is enabled configuring jumper JP TBD as a short circuit.

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vout,max	Maximum Output Voltage, DAC 1 or 2		9.9	10	10.1	V
Vout,min	Minimum Output Voltage, DAC 1 or 2		-10.1	-10	-9.9	V
Iout,max	Maximum Output Current, DAC 1 or 2 Chain		100	100	120	mA
R_{DAC1}	Output Impedence, DAC 1 Chain		-	50	80	Ohms
R_{DAC2}	Output Impedence, DAC 2 Chain		-	50	08	Ohms
Fs_{ADC}	Maximum Sample Rate, DAC		0.05	5	100	MHz
SNR	Achievable Signal to Noise Ratio					dB
T_{jitter}	Jitter Time					pS
Notes:						

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Storage Temperature Range	-65 to 80C
Shock, Z-Axis	±10 g
Shock, X/Y-Axis	±10 g

OPERATING CONDITIONS

Ambient Temperature Range	0 to 55C
Humidity	0 to 95% Non-condensing
Vibration, Z-Axis	TBS
Vibration, X/Y-Axis	TBS

MDK16 Socket Interface Description

The output frequency response for each DAC chain is shown in the figures below. The bandwidth at higher output levels will fall off as indicated in the figure.

TO BE SUPPLIED

Figure 2 DAC Output Frequency Response

MDK16 Socket Interface Description

The bottom connector of the MDK16-AWG card uses the required Hirose FX6-50P-0.8SV 50 position and two FX6-20P-0.8SV 20 position sockets. The pin assignments for the card are listed in Table 4.

Table 3 MDK-4 Connector (Left Side viewed from Top) Pin Assignments

Pin	Signal	I/O	Pin	Signal	I/O
A1			B1	+5 V	-
A2			B2	+5 V	-
A3			B3	+3.3 V	-
A4			B4	+3.3 V	-
A5	GND	-	B5	GND	-
A6	Not Used	-	B6	Not Used	-
A7	Not Used	-	B7	Not Used	-
A8	Not Used	-	B8	Not Used	-
A9	Not Used	-	B9	Not Used	-
A10	Not Used	-	B10	Not Used	-

Table 4 MDK-8 Connector Pin Assignments

Pin	Signal	I/O	Pin	Signal	I/O
A1			B1	+5 V	-
A2			B2	+5 V	-
A3			B3	+3.3 V	-
A4			B4	+3.3 V	-
A5			B5	+12 VA	-
A6			B6	GND	-
A7			B7	GND	-
A8			B8	GND	-
A9			B9	-12 VA	-
A10			B10	+15 V	-
A11			B11	+15 V	-
A12	Not Used	-	B12	-15 V	-
A13	Not Used	-	B13	-15 V	-
A14	Not Used	-	B14	AGND	-
A15	Not Used	-	B15	AGND	-
A16		-	B16	DO_CLK	-
A17		-	B17	RSV	-
A18		-	B18	RSV	-
A19		-	B19	RSV	-
A20		-	B20	RSV	-
A21		-	B21	RSV	-
A22		-	B22	RSV	-
A23	Not Used	-	B23	RSV	-
A24	Not Used	-	B24	RSV	-
A25	Offset Adjust	I	B25	RSV	-

Table 5 MDK-4 Connector (Right Side viewed from Top) Pin Assignments

Pin	Signal	I/O	Pin	Signal	I/O
A1			B1	+5 V	-
A2			B2	+5 V	-
A3			B3	+3.3 V	-
A4			B4	+3.3 V	-
A5	GND	-	B5	GND	-
A6	Not Used	-	B6	Not Used	-
A7	Not Used	-	B7	Not Used	-
A8	Not Used	-	B8	Not Used	-
A9	Not Used	-	B9	Not Used	-
A10	Not Used	-	B10	Not Used	-

DAC-1 Output Interface Description

The analog input interface to the MDK-ADS8329 uses a SMA female/right angle connector for the analog output generated from the first DAC output chain.

DAC-2 Output Interface Description

The analog input interface to the MDK-ADS8329 uses a SMA female/right angle connector for the analog output generated from the second DAC output chain.

External Trigger and Clock Source Interface Description

Connector J3 includes TTL compliant inputs for external trigger signals and external clock sources for use by the electrically connected MityDSP FPGA (through the MDK-MB interconnects). The interface uses a 16 position latching connector using standard 0.100 inch spacing. AMP TBD connectors (or equivalent) should be used with interface cables.

Table 6 J2 Pin Assignments

Pin	Signal	I/O	Pin	Signal	I/O
1	FST_TRIG_CLK_P	I	2	FST_TRIG_CLK_N	I
3	GND	I	4	GND	-
5	CONFIG	I	6	SLW_TRIG	-
7	DIG_IN_1	I	8	DIG_OUT	O
9	DIG_IN_2	I	10	DIG_OUT	O
11	DIG_IN_3	I	12	DIG_OUT	O
13	DIG_IN_4	I	14	DIG_OUT	O
15	DIG_IN_5	I	16	DIG_OUT	O

Software API and Supported Modes

The MityDSP software and firmware development kit includes a core interface and C++ API for interfacing to the DAC904E part, essentially an arbitrary waveform generator core with latched outputs. Refer to the MDK Software User's Guide for more information. Use of the on-board MDK-MB TLV5610 DAC API is required in order to properly configure the offset. Use of the GPIO MDK-MB API is required in order to properly configure the gain and utilize the digital input and outputs signals available on J3. Example software is included in the appendix of this specification for configuration of the card.