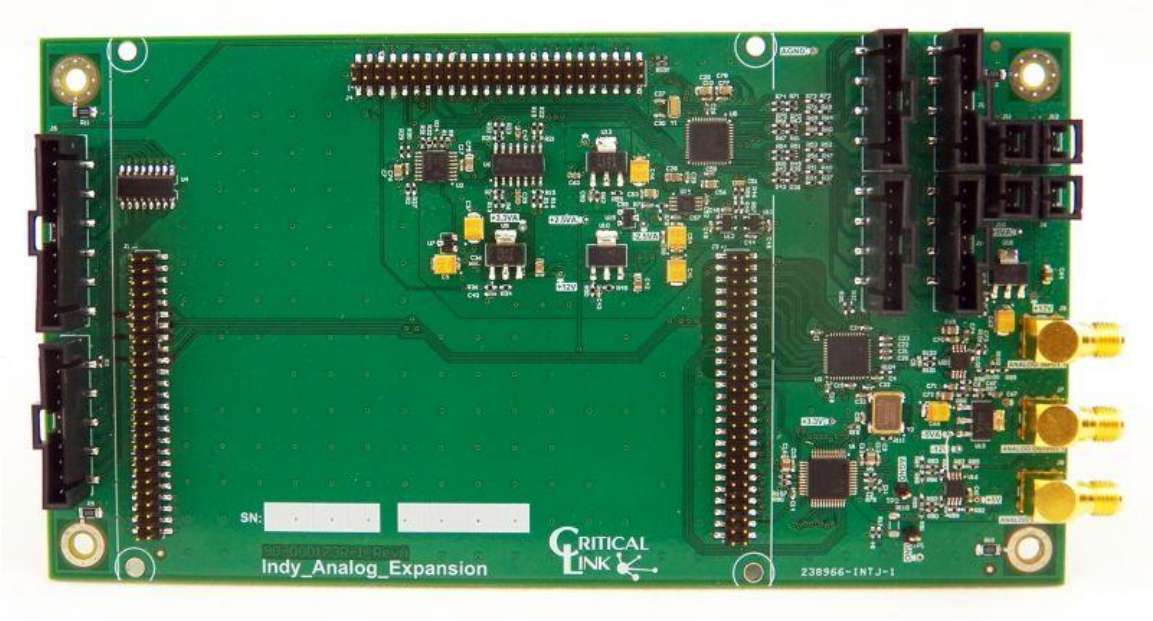
FEATURES

- Interfaces with MityDSP-L138F Industrial I/O Development Kit
- 16-Bit Digital-to-Analog Converter (DAC)
  - Quad-channel
  - Ultra-low glitch
- 14-Bit Digital-to-Analog Converter (DAC)
  - Dual-channel
  - 275 MSPS
- 16-Bit Analog-to-Digital Converter (ADC)
  - 16-channel (multiplexed)
  - 1.8-23.7 KSPS
  - Delta-Sigma (ΔΣ) ADC
  - Low-noise
- 16-Bit Analog-to-Digital Converter (ADC)
  - Single Channel
  - 40 MSPS DDR LVDS/CMOS outputs
- External Signals
  - 7 User GPIO Pins
  - I2C0 Interface
  - +12V, +3.3V and GND
- No external power supply required
- Example source code provided
- Expansion board design files provided
- Interface connector set provided

APPLICATIONS

- MityDSP-L138 Evaluation
- Embedded Signal Processing



DESCRIPTION

The Industrial I/O Analog Expansion provides both low-speed and high-speed digital-to-analog (DAC) and analog-to-digital (ADC) converters which expand the capabilities of the MityDSP-L138F Industrial I/O development kit.

The expansion board includes: one quad channel 16-bit low-speed DAC, one dual channel 14-bit high-speed (options up to 275MSPS) DAC, one 16 channel low speed (1.8K – 23.7K SPS) ADC, and one 16 bit single channel high speed (40MSPS) ADS5560 ADC. As an optional upgrade Critical Link can install the ADS5562 16 bit single channel ADC which is capable of up to 80MSPS, please contact Critical Link for further details. The expansion board also provides access to 7 GPIO pins which may be used in an open collector type output configuration or as direct 3.3V I/O. One I2C bus is also made available.

A block diagram of the expansion board is illustrated in Figure 1. Control of the on-board interface hardware requires proper configuration of the MityDSP-L138F FPGA, ARM and DSP. While not required, it is strongly recommended that the MityDSP-L138F software and firmware development kit and supplied API be used as a reference point to manage these interfaces.

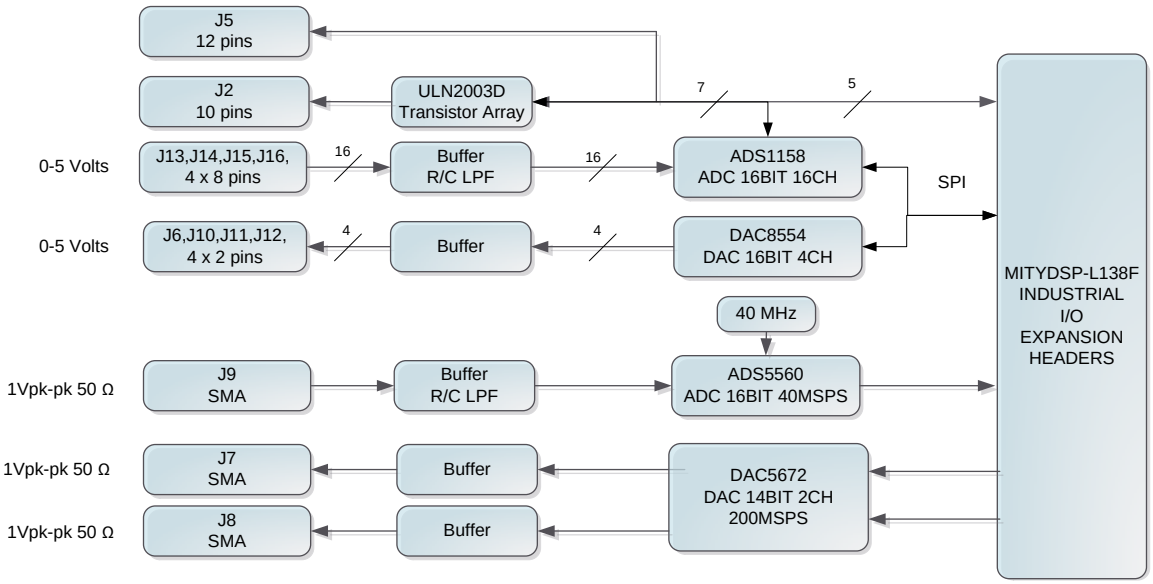


Figure 1: Expansion Board Block Diagram

DAC8554 Interface Description
The on-board DAC8554 interface provides 16-Bit, quad-channel, ultra-low glitch, low power consumption, and a flexible serial peripheral interface (SPI). Inputs are generated from OMAP processor IO pins and outputs are provided by four 2-pin connectors (J6/J10/J11/J12) on the board.

DAC5672 Interface Description
The on-board DAC8672 interface provides 14-bit, dual-channel, high-speed (275MSPS) digital-to-analog conversions. Inputs are generated from FPGA pins and outputs provided by two coaxial connectors (J7/J8) on the board.

ADS1158 Interface Description
The on-board ADS1158 interface provides a 16-channel, low noise, channel scan rates from 1.8k to 23.7k SPS per channel, a flexible input multiplexer to accept combinations of eight differential or 16 single-ended inputs, and a flexible serial host interface. Inputs are provided through four 8-pin connectors (J13/J14/J15/J16) and output is provided over SPI.

ADS5560 Interface Description
The on-board ADS5560 interface provides a 16-bit resolution, up to 40 MSPS, low noise, internal reference, and flexible features such as output interface (LVDS/CMOS) and fine gain. Input is provided through 1 coaxial connector (J9) and output is provided through FPGA IO.

As an optional upgrade the ADS5562 can be installed in place of the ADS5560 which supports up to an 80MSPS rate. Please contact your Critical Link representative for further details.

Expansion Board Interface Connectors

This expansion card provides three expansion IO connectors to mate with the MityDSP-L138F Industrial-IO board. Each connector includes one 50 position dual row receptacle. Mating connectors for these receptacles is a 2x25 2mm male header.

Table 1, Table 2 and Table 3provide signal descriptions for each pin of the Expansion Interface headers.

J1 of the Analog Expansion board Mates to J700 of the Industrial IO Board
J4 of the Analog Expansion board Mates to J701 of the Industrial IO Board
J3 of the Analog Expansion board Mates to J702 of the Industrial IO Board

Table 1: J1 Connector Pin Assignments (Mates to J700 of Industrial IO)

Pin	Signal	Type	Standard	Notes
1	GND	Power		
2	GND	Power		
3	GND	Power		
4	GND	Power		
5	+3.3V	Power		250mA Max (Per pin)
6	+3.3V	Power		250mA Max (Per pin)
7	+3.3V	Power		250mA Max (Per pin)
8	+3.3V	Power		250mA Max (Per pin)
9	NC	-		
10	NC	-		
11	DACSLCK/ ADCSCK	I – L138		DACSLCK(8554)/ADCSCK(ADS5560)
12	NC	-		
13	ADCDATA	I – L138		ADCDATA(ADS5560)
14	NC	-		
15	DACSDI	I –L138		DACSDI(8554)
16	NC	-		
17	NC	-		
18	NC	-		
19	ADCRESET	I – L138	3.3V LVCMOS	
20	DACSYNC	I – L138	3.3V LVCMOS	Chip Select for DAC8554
21	NC	-		
22	ADCCS	I – L138	3.3V LVCMOS	ADC Chip Select(ADS5560)
23	NC	-		
24	NC	-		
25	NC	-		
26	NC	-		
27	NC	-		
28	NC	-		
29	NC	-		
30	NC	-		
31	NC	-		
32	NC	-		
33	NC	-		
34	NC	-		
35	NC	-		
36	NC	-		
37	NC	-		
38	NC	-		
39	NC	-		
40	NC	-		
41	NC	-		
42	NC	-		
43	NC	-		
44	GND	Power		
45	NC	-		
46	GND	Power		
47	GND	Power		
48	GND	Power		
49	GND	Power		
50	GND	Power		

Table 2: J4 Connector Pin Assignments (Mates to J701 of Industrial IO)

Pin	Signal	Type	Standard	Notes
1	GND	Power		
2	GND	Power		
3	CS	I - FPGA	3.3V LVCMOS	ADC chip select (ADS1158)
4	CLK1	I - FPGA	3.3V LVCMOS	DAC write clock A (DAC5672)
5	START	I - FPGA	3.3V LVCMOS	ADC start conversion (ADS1158)
6	OVR	I - FPGA	3.3V LVCMOS	ADC OVR Output (ADS5560)
7	DRDY	O - FPGA	3.3V LVCMOS	ADC conversion ready signal (ADS1158)
8	DIN	I - FPGA	3.3V LVCMOS	ADC data input (ADS1158)
9	CLKIO	I/O - FPGA	3.3V LVCMOS	ADC System Clock (ADS1158)
10	DOUT	O - FPGA	3.3V LVCMOS	ADC data output (ADS1158)
11	CLKOUT P	O - FPGA	3.3V LVCMOS	ADC Positive Clock Output (ADS5560)
12	CLKOUT N	O - FPGA	3.3V LVCMOS	ADC Negative Clock Output (ADS5560)
13	SCLK	I - FPGA	3.3V LVCMOS	ADC SPI clock (ADS1158)
14	CLK2	I - FPGA	3.3V LVCMOS	DAC write clock B (DAC5672)
15	GND	Power		
16	GND	Power		
17	NC	-		
18	NC	-		
19	NC	-		
20	RESET	I – L138	3.3V LVCMOS	ADC active low reset (ADS1158)
21	GPIO 4	I/O – L138	3.3V LVCMOS	Software configurable GPIO
22	GPIO 1	I/O – L138	3.3V LVCMOS	Software configurable GPIO
23	GPIO 2	I/O – L138	3.3V LVCMOS	Software configurable GPIO
24	GPIO 3	I/O – L138	3.3V LVCMOS	Software configurable GPIO
25	NC	-		
26	GPIO 0	I/O – L138	3.3V LVCMOS	Software configurable GPIO
27	I2C0_SDA[1]	I/O – L138	3.3V LVCMOS	I2C0 to J5 Pin 9 Expansion Header
28	I2C0_SCL[1]	I/O – L138	3.3V LVCMOS	I2C0 to J5 Pin 10 Expansion Header
29	GND	Power		
30	GND	Power		
31	GND	Power		
32	GND	Power		
33	-12V[2]	Power		250mA Max (Per pin)
34	-12V[2]	Power		250mA Max (Per pin)
35	-12V[2]	Power		250mA Max (Per pin)
36	-12V[2]	Power		250mA Max (Per pin)
37	+3.3V[2]	Power		250mA Max (Per pin)
38	+3.3V[2]	Power		250mA Max (Per pin)
39	+3.3V[2]	Power		250mA Max (Per pin)
40	+3.3V[2]	Power		250mA Max (Per pin)
41	+5V[2]	Power		250mA Max (Per pin)
42	+5V[2]	Power		250mA Max (Per pin)
43	+5V[2]	Power		250mA Max (Per pin)
44	+5V[2]	Power		250mA Max (Per pin)
45	+12V[2]	Power		250mA Max (Per pin)
46	+12V[2]	Power		250mA Max (Per pin)
47	+12V[2]	Power		250mA Max (Per pin)
48	+12V[2]	Power		250mA Max (Per pin)
49	GND	Power		
50	GND	Power		

Notes:
[1] The I2C bus controlled by MityDSP-L138 hardware. Slave address 0x90 reserved for Power Management Controller IC. User should not attempt to write any data to this address as it will result in MityDSP-L138 damage.
[2] Maximum current per power bus should be limited to 1.0Amp, it is advised to have input fuses on expansion board.

Table 3: J3 Connector Pin Assignments (Mates to J702 of Industrial IO)

Pin	Signal	Type	Standard	Notes
1	GND	Power		
2	GND	Power		
3	D0 D1 N	O - FPGA	3.3V LVCMOS	ADC D0/D1 multiplexed, true (ADS5560)
4	D0 D1 P	O – FPGA	3.3V LVCMOS	ADC D1/D1 multiplexed, compliment
5	D2 D3 N	O – FPGA	3.3V LVCMOS	ADC D2/D3 multiplexed, true (ADS5560)
6	D2 D3 P	O – FPGA	3.3V LVCMOS	ADC D2/D3 multiplexed, compliment
7	D4 D5 N	O – FPGA	3.3V LVCMOS	ADC D4/D5 multiplexed, true (ADS5560)
8	D4 D5 P	O – FPGA	3.3V LVCMOS	ADC D4/D5 multiplexed, compliment
9	D6 D7 N	O – FPGA	3.3V LVCMOS	ADC D6/D7 multiplexed, true (ADS5560)
10	D6 D7 P	O – FPGA	3.3V LVCMOS	ADC D6/D7 multiplexed, compliment
11	D8 D9 N	O – FPGA	3.3V LVCMOS	ADC D8/D9 multiplexed, true (ADS5560)
12	D8 D9 P	O – FPGA	3.3V LVCMOS	ADC D8/D9 multiplexed, compliment
13	D10 D11N	O – FPGA	3.3V LVCMOS	ADC D10/D11 multiplexed, true (ADS5560)
14	D10 D11P	O – FPGA	3.3V LVCMOS	ADC D10/D11 multiplexed, compliment
15	DB 0	I – FPGA	3.3V LVCMOS	DAC channel B input <0> (DAC5672)
16	DB 1	I – FPGA	3.3V LVCMOS	DAC channel B input <1> (DAC5672)
17	DB 2	I – FPGA	3.3V LVCMOS	DAC channel B input <2> (DAC5672)
18	DB 3	I – FPGA	3.3V LVCMOS	DAC channel B input <3> (DAC5672)
19	D12 D13 N	O – FPGA	3.3V LVCMOS	ADC D12/D13 multiplexed, true (ADS5560)
20	D12 D13 P	O – FPGA	3.3V LVCMOS	ADC D12/D13 multiplexed, compliment
21	D14 D15N	O – FPGA	3.3V LVCMOS	ADC D14/D15 multiplexed, true (ADS5560)
22	D14 D15P	O – FPGA	3.3V LVCMOS	ADC D14/D15 multiplexed, compliment
23	DA 0	I – FPGA	3.3V LVCMOS	DAC channel A input <0> (DAC5672)
24	DA 1	I – FPGA	3.3V LVCMOS	DAC channel A input <1> (DAC5672)
25	DA 2	I – FPGA	3.3V LVCMOS	DAC channel A input <2> (DAC5672)
26	DA 3	I – FPGA	3.3V LVCMOS	DAC channel A input <3> (DAC5672)
27	DA 4	I – FPGA	3.3V LVCMOS	DAC channel A input <4> (DAC5672)
28	DA 5	I – FPGA	3.3V LVCMOS	DAC channel A input <5> (DAC5672)
29	DA 6	I - FPGA	3.3V LVCMOS	DAC channel A input <6> (DAC5672)
30	DA 7	I – FPGA	3.3V LVCMOS	DAC channel A input <7> (DAC5672)
31	DA 8	I – FPGA	3.3V LVCMOS	DAC channel A input <8> (DAC5672)
32	DA 9	I – FPGA	3.3V LVCMOS	DAC channel A input <9> (DAC5672)
33	DA 10	I – FPGA	3.3V LVCMOS	DAC channel A input <10> (DAC5672)
34	DA 11	I – FPGA	3.3V LVCMOS	DAC channel A input <11> (DAC5672)
35	DA 12	I – FPGA	3.3V LVCMOS	DAC channel A input <12> (DAC5672)
36	DA 13	I – FPGA	3.3V LVCMOS	DAC channel A input <13> (DAC5672)
37	NC	-		
38	NC	-		
39	DB 4	I - FPGA	3.3V LVCMOS	DAC channel B input <4> (DAC5672)
40	DB 5	I - FPGA	3.3V LVCMOS	DAC channel B input <5> (DAC5672)
41	DB 6	I - FPGA	3.3V LVCMOS	DAC channel B input <6> (DAC5672)
42	DB 7	I - FPGA	3.3V LVCMOS	DAC channel B input <7> (DAC5672)
43	DB 8	I - FPGA	3.3V LVCMOS	DAC channel B input <8> (DAC5672)
44	DB 9	I - FPGA	3.3V LVCMOS	DAC channel B input <9> (DAC5672)
45	DB 10	I - FPGA	3.3V LVCMOS	DAC channel B input <10> (DAC5672)
46	DB 11	I - FPGA	3.3V LVCMOS	DAC channel B input <11> (DAC5672)
47	DB 12	I - FPGA	3.3V LVCMOS	DAC channel B input <12> (DAC5672)
48	DB 13	I - FPGA	3.3V LVCMOS	DAC channel B input <13> (DAC5672)
49	GND	Power		
50	GND	Power		

GPIO Expansion Interfaces

The expansion card provides access to 7 additional GPIO pins through two separate connectors, J2 and J5.

J2 is a 1x10 pin, 2.54mm pitch, male connector that provides GPIO 0-6 output through a Darlington array for the driving of higher current circuits. These are the same GPIO signals as J5. Table 6 shows the signal description for each pin of J2.

J5 is a 1x12, 2.54mm pitch, male connector that provides access to GPIO 0-6 and I2C0 SCL/SDA signals. Table 7 shows the signal description for each pin of J5.

Table 4: J2 Connector Pin Assignments

Pin	Signal	Type	Standard	Notes
1	GND	Power		
2	COM	O		
3	+12V	Power		
4	GPIO OC 13	O	3.3V LVCMOS - HC	Software configurable GPIO
5	GPIO OC 15	O	3.3V LVCMOS - HC	Software configurable GPIO
6	GPIO OC 1	O	3.3V LVCMOS - HC	Software configurable GPIO
7	GPIO OC 2	O	3.3V LVCMOS - HC	Software configurable GPIO
8	GPIO OC 3	O	3.3V LVCMOS - HC	Software configurable GPIO
9	GPIO OC 4	O	3.3V LVCMOS - HC	Software configurable GPIO
10	RSV			Software configurable GPIO

Table 5: J5 Connector Pin Assignments

Pin	Signal	Type	Standard	Notes
1	GPIO_0	I/O - OMAP	3.3V LVCMOS	Software configurable GPIO
2	GPIO_1	I/O - OMAP	3.3V LVCMOS	Software configurable GPIO
3	GPIO_2	I/O - OMAP	3.3V LVCMOS	Software configurable GPIO
4	GPIO_3	I/O - OMAP	3.3V LVCMOS	Software configurable GPIO
5	GPIO_4	I/O - OMAP	3.3V LVCMOS	Software configurable GPIO
6	GPIO_5	I/O - OMAP	3.3V LVCMOS	Software configurable GPIO
7	GPIO_6	I/O - OMAP	3.3V LVCMOS	Software configurable GPIO
8	GND	Power		
9	SCL	I/O - OMAP	3.3V LVCMOS	I2C0 SCL
10	SDA	I/O - OMAP	3.3V LVCMOS	I2C0 SCL
11	+3.3V	Power		
12	GND	Power		

Analog Output Interfaces

The expansion card provides two methods for acquiring an analog signal; a DAC8554 and DAC5672.

DAC8554

When using the DAC8554, J6/J10/J11/J12 provides output differential voltage using four 1x2 pin, 2.54mm pitch, male Molex headers. Tables 6,7,8,9 provide signal descriptions for each pin.

Table 6: J6 Connector Pin Assignments

Pin	Signal	Type	Standard	Notes
1	VOUTA	O	0 to 5V	DAC8554 Ch. 1
2	AGND	Power		

Table 7: J10 Connector Pin Assignments

Pin	Signal	Type	Standard	Notes
1	VOUTB	O	0 to 5V	DAC8554 Ch. 2
2	AGND	Power		

Table 8: J11 Connector Pin Assignments

Pin	Signal	Type	Standard	Notes
1	VOUTC	O	0 to 5V	DAC8554 Ch. 3
2	AGND	Power		

Table 9: J12 Connector Pin Assignments

Pin	Signal	Type	Standard	Notes
1	VOUTD	O	0 to 5V	DAC8554 Ch. 4
2	AGND	Power		

DAC5672

When using the DAC5672, J7 and J8 provide differential voltage outputs using a coaxial connector. Tables 10 and 11 provide signal descriptions for each pin.

Table 10: J7 Connector Pin Assignments

Pin	Signal	Type	Standard	Notes
1	VOUTA	O	1V pk-pk / 50ohm	DAC5672 Ch. 1
housing	AGND	Power		

Table 11: J8 Connector Pin Assignments

Pin	Signal	Type	Standard	Notes
1	VOUTB	O	1V pk-pk / 50ohm	DAC5672 Ch. 2
housing	AGND	Power		

Analog Input Interfaces

The expansion card provides two methods for inputting an analog signal; an ADS1158 and ADS5560.

ADS1158

When using the ADS1158, J13/J14/J15/J16 provides output differential voltage using four 1x8 pin, 2.54mm pitch, male wire-to-board headers. Tables 12,13,14,15 provide signal descriptions for each pin.

Table 12: J13 Connector Pin Assignments

Pin	Signal	Type	Standard	Notes
1	AIN15	I	0 to 5 V	ADS1158 Input Ch 16
2	AGND	Power		
3	AIN14	I	0 to 5 V	ADS1158 Input Ch 15
4	AGND	Power		
5	AIN13	I	0 to 5 V	ADS1158 Input Ch 14
6	AGND	Power		
7	AIN12	I	0 to 5 V	ADS1158 Input Ch 13
8	AGND	Power		

Table 13: J14 Connector Pin Assignments

Pin	Signal	Type	Standard	Notes
1	AIN11	I	0 to 5 V	ADS1158 Input Ch 12
2	AGND	Power		
3	AIN10	I	0 to 5 V	ADS1158 Input Ch 11
4	AGND	Power		
5	AIN9	I	0 to 5 V	ADS1158 Input Ch 10
6	AGND	Power		
7	AIN8	I	0 to 5 V	ADS1158 Input Ch 9
8	AGND	Power		

Table 14: J15 Connector Pin Assignments

Pin	Signal	Type	Standard	Notes
1	AIN7	I	0 to 5 V	ADS1158 Input Ch 8
2	AGND	Power		
3	AIN6	I	0 to 5 V	ADS1158 Input Ch 7
4	AGND	Power		
5	AIN5	I	0 to 5 V	ADS1158 Input Ch 6
6	AGND	Power		
7	AIN4	I	0 to 5 V	ADS1158 Input Ch 5
8	AGND	Power		

Table 15: J16 Connector Pin Assignments

Pin	Signal	Type	Standard	Notes
1	AIN3	I	0 to 5 V	ADS1158 Input Ch 4
2	AGND	Power		
3	AIN2	I	0 to 5 V	ADS1158 Input Ch 3
4	AGND	Power		
5	AIN1	I	0 to 5 V	ADS1158 Input Ch 2
6	AGND	Power		
7	AIN0	I	0 to 5 V	ADS1158 Input Ch 1
8	AGND	Power		

ADS5560

When using the ADS5560, J9 provides differential voltage using a coaxial connector. Table 16 provides signal description for each pin.

Table 16: J9 Connector Pin Assignments

Pin	Signal	Type	Standard	Notes
1	IN_P/IN_N	I	1V pk-pk / 50 ohm	ADS5560 Input
housing	AGND	Power		

MECHANICAL INTERFACE DESCRIPTION

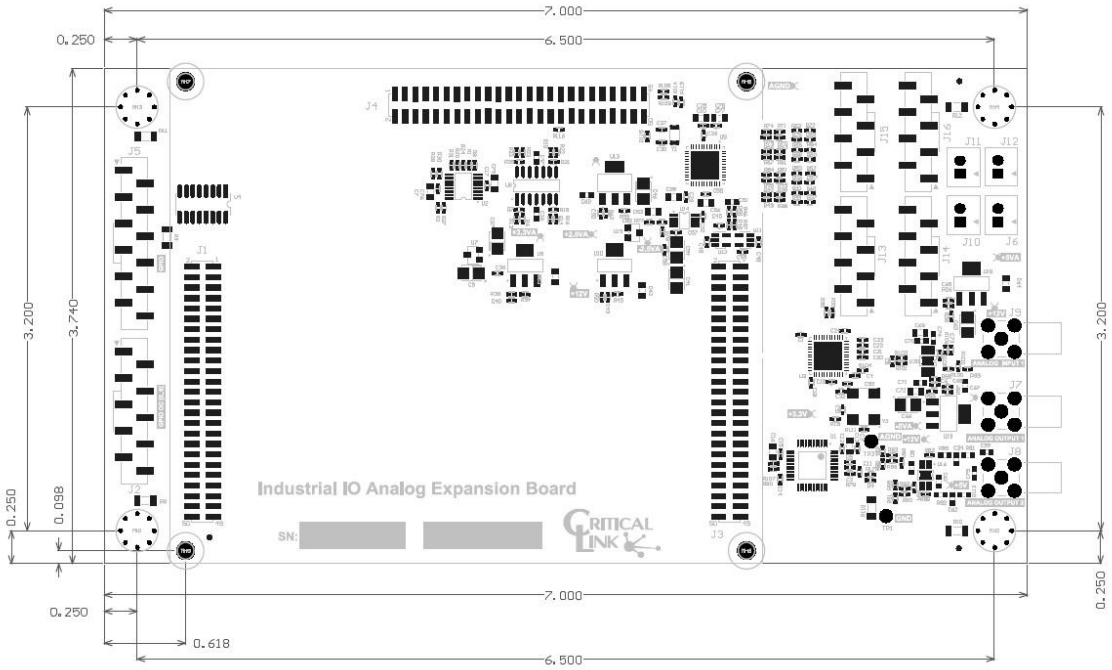


Table 17: Mechanical Dimensions

ORDERING INFORMATION

The following table lists the standard stock expansion kit part number. For shipping status, availability, and lead time of this expansion kit please contact your Critical Link representative.

Table 18: Standard Stock Expansion Kit Number

Part Number
80-000643

REVISION HISTORY

Date	Change Description
April 22, 2013	Initial preliminary specification based upon Rev A PCA
September 13, 2013	Preliminary update based upon Rev B PCA
January 22, 2014	Initial release
June 13, 2014	Clarification of ADS5560 capabilities and ADS5562 option