1 OVERVIEW

The information in this data sheet is for the MitySOM-iMX6 System on Module family from Critical Link. In addition to supplying these off the shelf solutions, Critical Link's embedded design team is able to provide systems engineering, software development, and hardware design services to support your project anywhere in the development lifecycle. Email info@criticallink.com with any questions.

2 INTRODUCTION

2.1 PRODUCT DESCRIPTION

The MitySOM-iMX6 is based on NXP Semiconductors iMX6 family of processors with ARM Cortex-A9 at speeds up to 1.2 GHz. It is an industrial computer platform in a compact form factor. The family includes a variety of options for RAM and Flash memory, interfaces and peripherals, and the possibility to have a 3D graphic accelerator.

Critical Link also provides a SMARC expansion board to complement the module and give developers a faster path to application and prototype development.

Highlights:

- Easy connectivity through the SMARC-314 connector
- Small form factor (82mm x 50mm)
- 1V8 I/O level signals
- JTAG interface available
- Based on NXP Semiconductors iMX6 processor with Cortex-A9 ARM Architecture
- The iMX6 processors include the NEON TM Media coprocessor
- Gigabit Ethernet Physical Layer Transceiver (PHY)
- WiFi IEEE 802.11 a/b/g/n with Access Point
- Bluetooth v4.0 (BLE)
- Flexible Memory of Flash Memory combinations (customized option)

2.2 MitySOM-iMX6 BENEFITS AND APPLICATIONS

Key benefits of the MitySOM-iMX6 modules include:

- Compact and powerful core for new products
- Robust and easy to mount due to the SMARC 314 connector
- Reduced time to market
- Low power consumption ≤ 6W
- Commercial and Industrial Temperature Range
- Long product lifespan

MitySOM-iMX6 is a fit for a broad range of industrial applications, including:

- Connected vending machines
- Home / Building automation
- Human Interface
- Industrial Control
- Test and Measurement

2.3 MitySOM-iMX6 SERIES

The MitySOM-iMX6 includes a number of standard models shown in Section 2.4 below. These models provide scalable options for the CPU, RAM memory, and storage memory. Section 3.3 details the main differences by processor model. To inquire about MOQs on these variants or additional variants not listed, contact Critical Link at info@criticallink.com.

2.4 ORDERING INFORMATION

Module P/N	Cores	CPU Speed	RAM	eMMC	SPI NOR	WiFi/BT	Ethernet	Temp
6Q-2G-8G-W-E-I	Quad	800MHz	2GB	8GB	N/A	Yes	Yes	-40C to 85C
6Q-1G-8GA-W-E-I	Quad	800MHz	1GB	8GB	512KB	Yes	Yes	-40C to 85C
6Q-1G-8G-W-E-I	Quad	800MHz	1GB	8GB	N/A	Yes	Yes	-40C to 85C
6D-2G-8G-W-E-I	Dual	800MHz	2GB	8GB	N/A	Yes	Yes	-40C to 85C
6DL-2G-8G-W-E-I	DualLite	800MHz	2GB	8GB	N/A	Yes	Yes	-40C to 85C
6DL-1G-4G-W-E-I	DualLite	800MHz	1GB	4GB	N/A	Yes	Yes	-40C to 85C
6S-512M-4G-W-E-I	Single	800MHz	512MB	4GB	N/A	Yes	Yes	-40C to 85C

Table 1 Ordering Information

2.5 EXPANSION BOARD

All of the MitySOM-iMX6 modules are compatible with the following SMARC expansion board. Development Kits for the MitySOM-iMX6 family include the SMARC expansion board, a SOM, and power supply. A list of available development kits is shown on https://www.criticallink.com/mitysom-imx6-dev-kit/.

Device	Orderable Part Number	Description
SMARC EXPANSION BOARD	93-900799	Designed for fast prototyping of user's projects

Table 2 Expansion Boards

3 OVERVIEW

3.1 MitySOM-iMX6

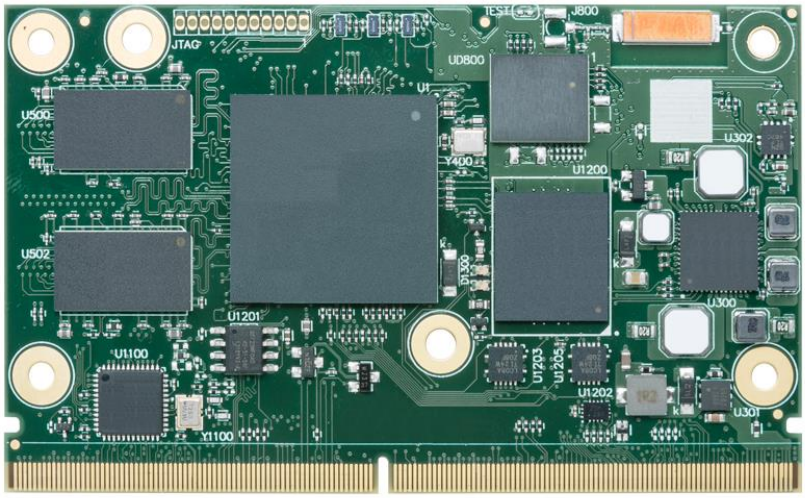


Figure 1 MitySOM-iMX6 Top View

Figure 2 MitySOM-iMX6 Bottom View

3.2 MitySOM-iMX6 FEATURES

Feature	iMX6Quad	iMX6Dual	iMX6DualLite	iMX6Solo
ARM CPU	4x NXP iMX6 ARM Cortex–A9TM up to 1.2GHz L1 Instruction cache: 32 KB per core L1 Data cache: 32 KB per core L2 cache: 1 MB NEON™ SIMD Coprocessor per core PTM per core	2x NXP iMX6 ARM Cortex–A9TM up to 1.2GHz L1 Instruction cache: 32 KB per core L1 Data cache: 32 KB per core L2 cache: 1 MB NEON™ SIMD Coprocessor per core PTM per core	2x NXP iMX6 ARM Cortex–A9TM up to 1GHz L1 Instruction cache: 32 KB per core L1 Data cache: 32 KB per core L2 cache: 512 KB NEON™ SIMD Coprocessor per core PTM per core	1x NXP iMX6 ARM Cortex–A9TM up to 1GHz L1 Instruction cache: 32 KB L1 Data cache: 32 KB L2 cache: 512 KB NEON™ SIMD Coprocessor PTM
2D/3D graphics acceleration	Vivante GC2000 GPU 3D Vivante GC320 GPU 2D (Composition) Vivante GC355 GPU 2D (Vector Graphics) OpenGL ES 3.0, OpenCL 1.1 EP and Open VG 1.1 support		Vivante GC880 GPU 3D Vivante GC320 GPU 2D (Composition) GPU 2D (Vector Graphics) emulated on GPU 3D OpenGL ES 2.0 support	
Video acceleration	Video acceleration: H.264, H.263, MPEG-2 and MPEG-4 Video encoder/decoder dual 1080p ® 60 fps 2x IPU		Video acceleration: H.264, H.263, MPEG-2 and MPEG-4 Video encoder/decoder 1080p ® 60 fps 1x IPU	
Camera Interface	MIPI CSI-2 (4 lanes)		MIPI CSI-2 (2 lanes)	

Table 3 iMX6 Processor Features

Feature	Specifications
RAM Memory	Up to 4 GB DDR3-1066 SDRAM
Flash Storage	Up to 64 GB eMMC, optional SPI NOR

Table 4 Memory and Storage

Feature	Specifications
Power to SMARC-314 connector	Supply Voltage (VIN) from 4.75 V to 5.25 V DC

Table 5 Power

Feature	Specifications
Interfaces	1 x SMARC-314 expansion interface 1 x JTAG interface
Device Features	1 x Double LED indicator: Red LED / Green LED for user application 1 x EEPROM
Device Options	1 x eMMC flash interface 1 x SPI NOR flash 1 x WiFi IEEE 802.11 a/b/g/n with Access Point 1 x Bluetooth v4.0 1 x 10/100/1000 Mbps Ethernet PHY interface

Table 6 On-Board Interfaces and Devices Options

3.3 iMX6 PROCESSOR VARIANTS

MitySOM-iMX6 modules are based on the NXP iMX6 family of processors which includes several processor options, each one with different characteristics. Figure 3 below shows the processor options with their differences. Standard models are listed in Section 2.4. Contact info@criticallink.com for more information.

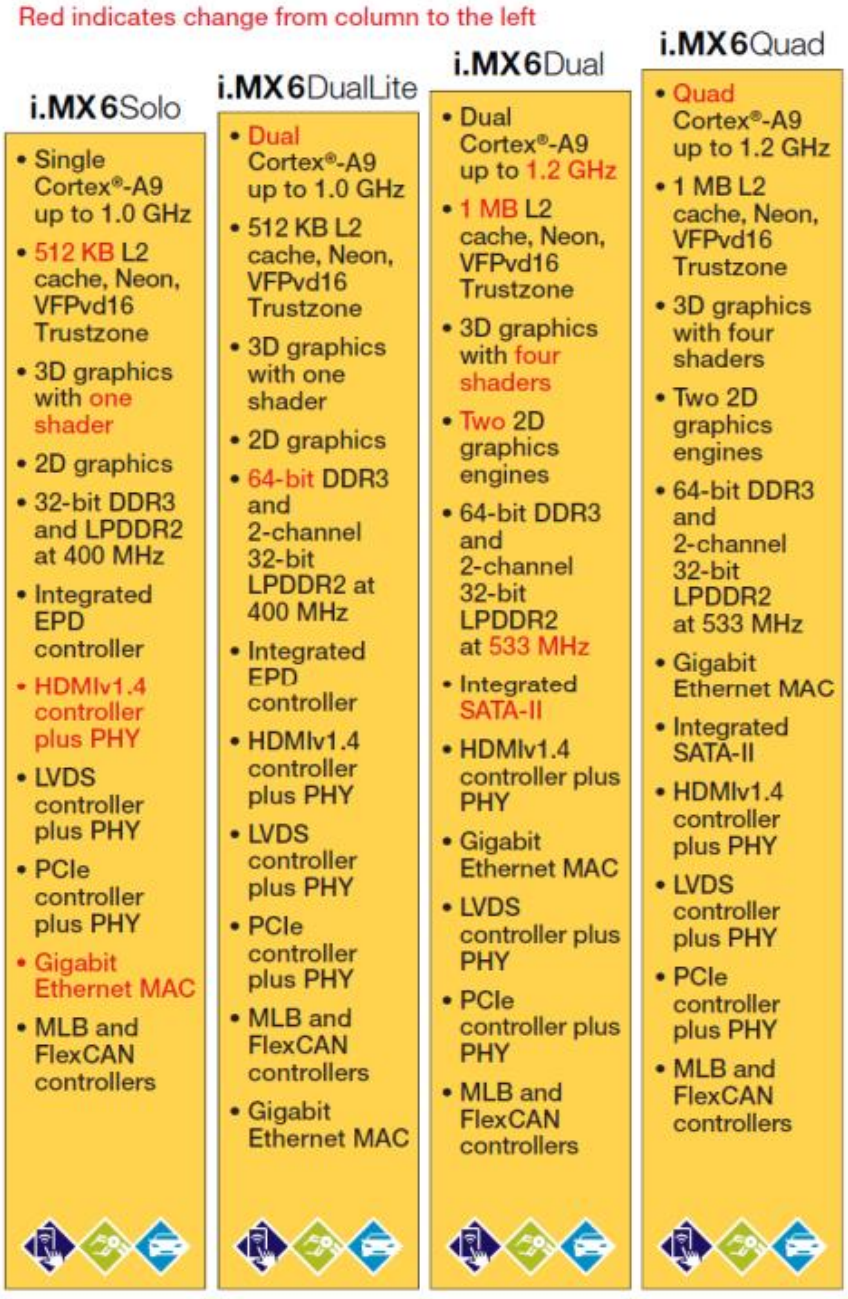


Figure 3 NXP iMX6 Family Features

3.4 iMX6 ARM CORTEX-A9 PROCESSORS

The iMX6 processor is a family of highly integrated microprocessors based on the ARM Cortex-A9 processor. They offer high performance at low cost and are delivered with 3D graphics acceleration and key peripherals. They also support multiple high-level operating systems (Linux and Android).

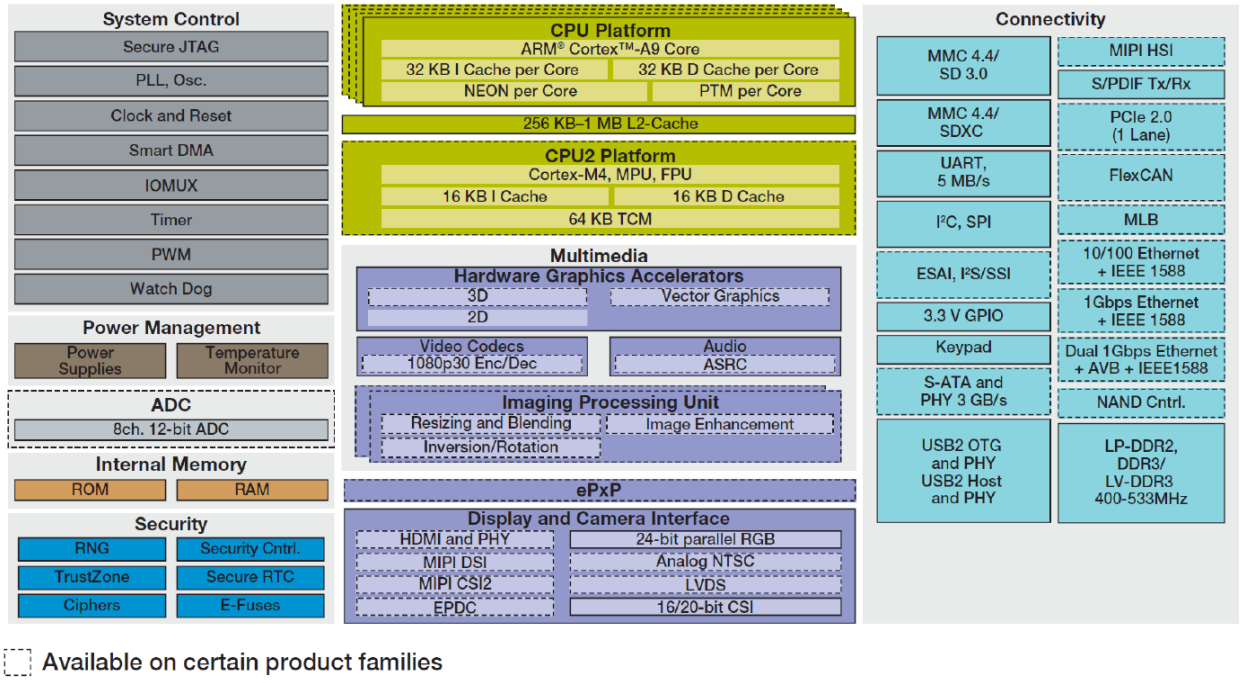


Figure 4 iMX6 Processor Block Diagram

4 PRODUCT SPECIFICATIONS

4.1 MitySOM-iMX6 BLOCK DIAGRAM

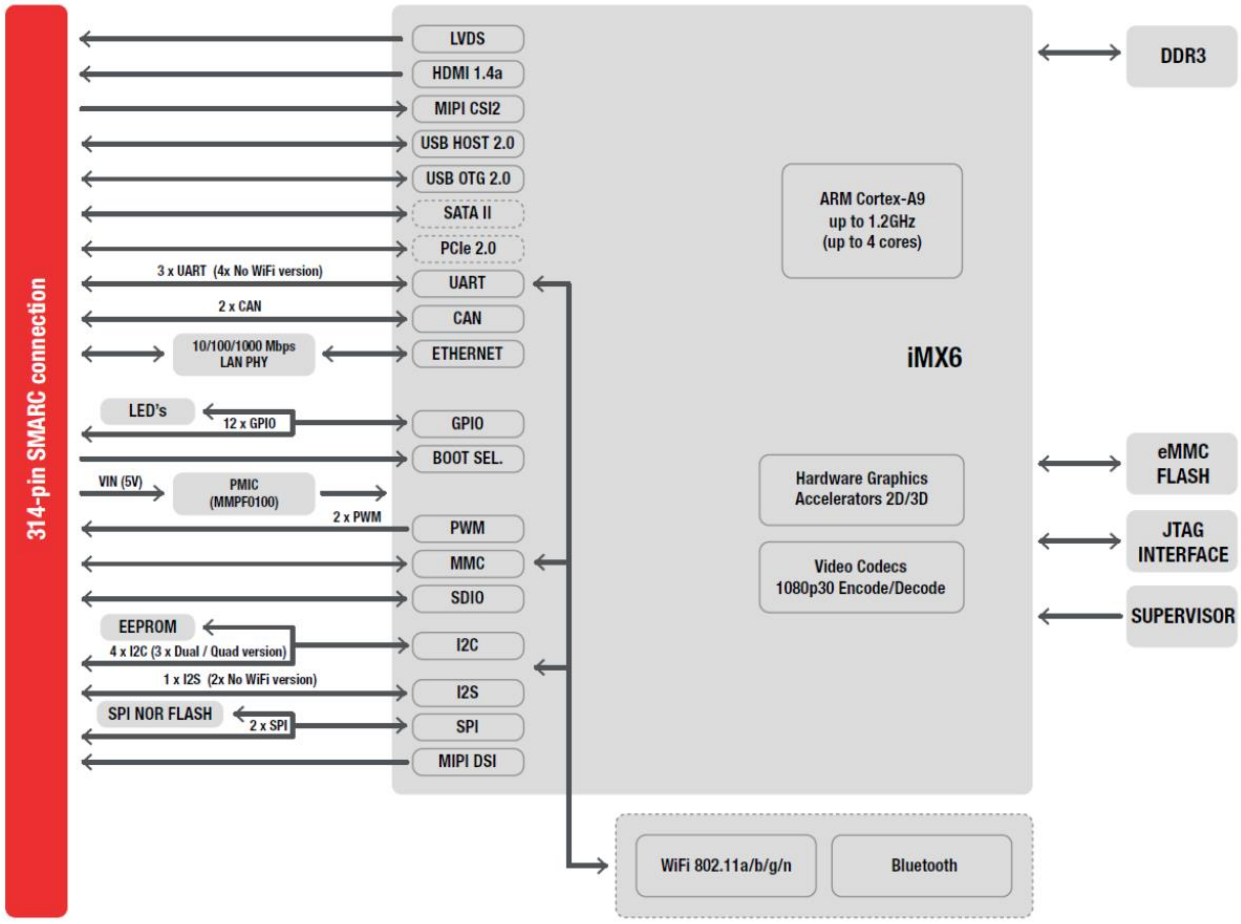


Figure 5 MitySOM-iMX6 Block Diagram

4.2 POWER SOURCES

4.2.1 Supply Voltage

The power supply of the module is made with a single standard voltage of 5V, using the defined inputs (pins P147 to P156, all the connections in this section are referred to the SMARC-314 connector, see Table 30 J900 SMARC-314 pinout description). This voltage can be from a minimum value of 4.75V to a maximum of 5.25V (see electrical characteristics in Section 7). The following figure shows a schematic example of this power signal (also discussed in the SMARC Design Guide).

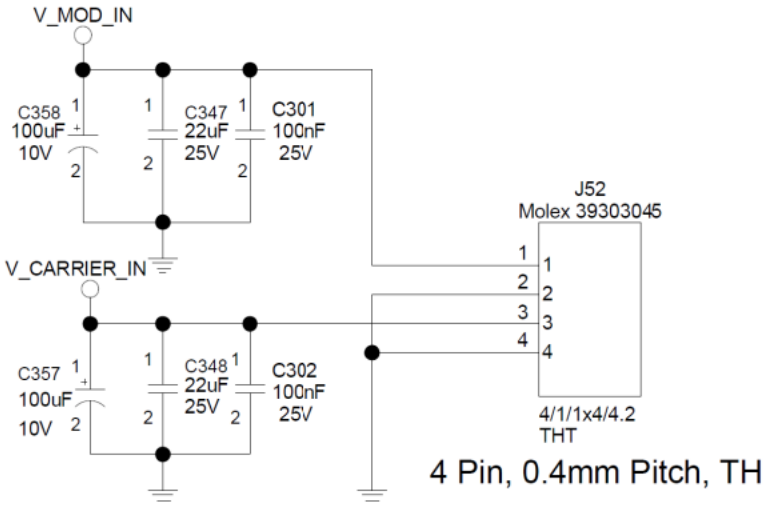


Figure 6 Power Supply Input Circuit

4.2.2 RTC Battery

The RTC Battery pin (S147) allows the connection of a battery. With this, in the case of a general power fail, the RTC circuit will be powered. The user has to be careful with the selection of battery capacity: depending on the current consumption, the activity duration will be drastically reduced. The following figure shows RTC Battery examples (also discussed in the SMARC Design Guide).

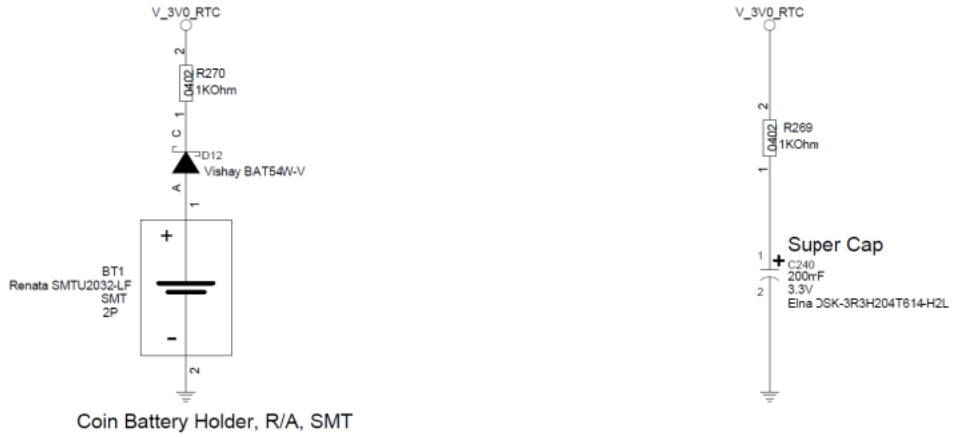


Figure 7 RTC Battery

4.2.3 GND Pins

All of the GND pins are internally connected together, so it is not necessary to connect all of them. However, the user has to consider how many of them connect according the total consumption of the complete circuit. At the same time, to make the routing of buses easier, the ground connection chosen will be the nearest to the function used.

4.3 CONTROL SIGNALS

There are different pins used as general control signals. They affect the Boot Mode, the management of the power supply, and resets.

4.3.1 Boot Mode

The Boot Mode can be fixed by user acting over the pins P125, P124 and P123. When the module is powered on, it reads these pins and boots as specified in the following table.

BOOT_SEL2# (P125)	BOOT_SEL2# (P124)	BOOT_SEL2# (P123)	Boot source
GND	GND	GND	Carrier SATA
GND	GND	Float	Carrier SD Card
GND	Float	GND	Carrier eMMC Flash
GND	Float	Float	Carrier SPI
Float	GND	GND	Module device
Float	GND	Float	Remote boot
Float	Float	GND	Module eMMC Fash
Float	Float	Float	Module SPI

Table 7 Boot Mode

It is recommended to use jumper headers to control these boot pins as shown in the following figure (also discussed in the SMARC Design Guide).

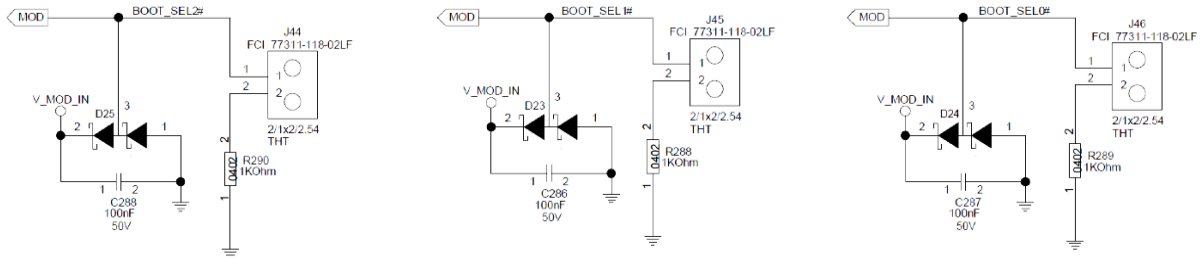


Figure 8 Boot Mode: Jumpers Selectors

4.3.2 Reset Pins

There are two Reset-IO possibilities. The first one is a General Reset RESET_IN# (P127) and the other is a RESET_OUT# (P126).

When the RESET_IN# is driven to Low state (with a delay configurable), the power supply from the Power Management IC, PMIC, is turned off.

The RESET_OUT# pin is an output signal for sending a Reset to external devices (carrier board peripherals).

The following two examples show how to implement each reset. Figure 10 shows how to make a reset to an external circuit, in this case a touch controller (also discussed in the SMARC Design Guide).

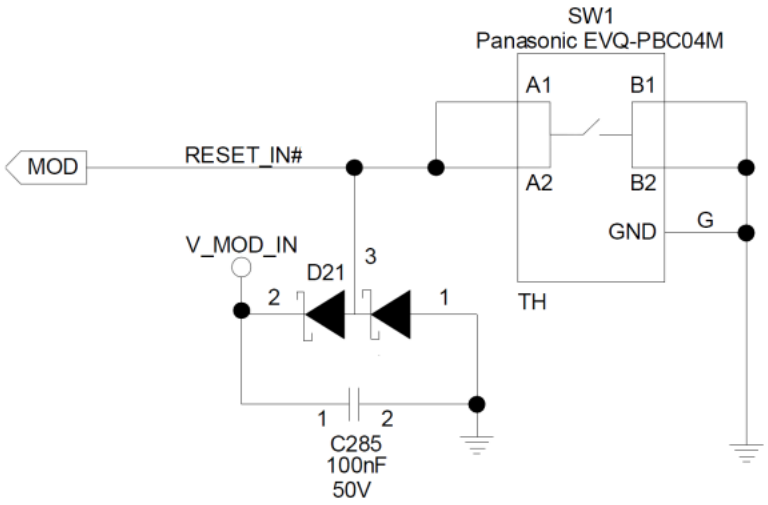


Figure 9 RESET_IN# Pushbutton

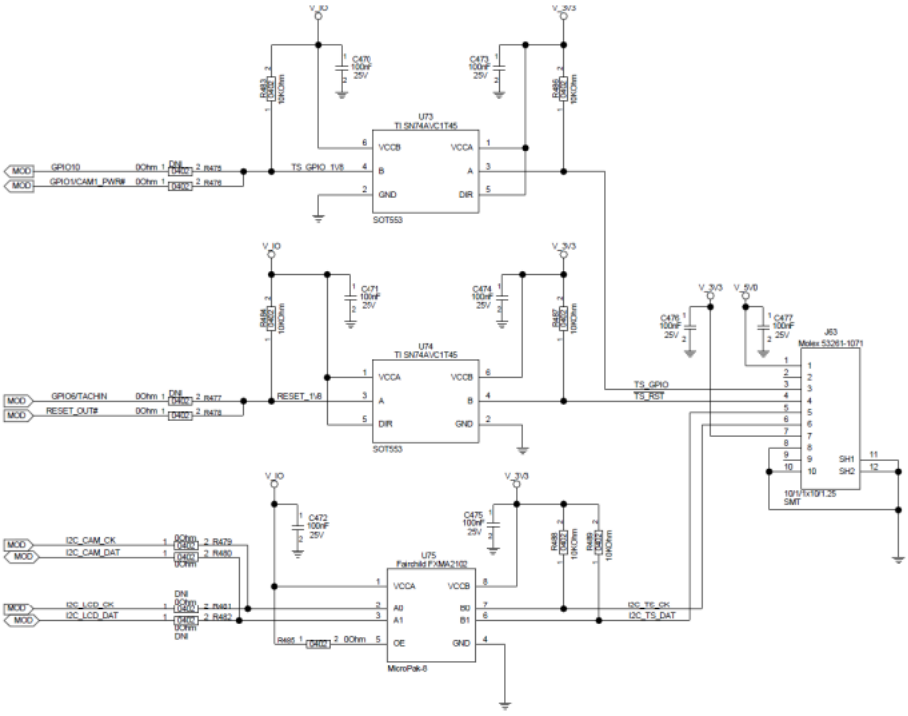


Figure 10 Reset Out Circuit Example

4.4 ETHERNET

The module can be connected to a standard 10/100/1000 Mbps Ethernet system. For this function, there is a block of pins in the SMARC-314 that can be connected directly to the Ethernet LAN. MDI lines are differential (in the pin function is indicated the Negative and Positive) and they should be connected to isolation magnetics. The data lines have to be equal length and symmetric, and respect a 100Ω differential impedance in the layout traces. The differential pairs must be isolated from nearby signals and circuitry to maintain the signal integrity.

Moreover, the magnetics module has a critical effect, so it has to be designed carefully. In order to obtain a smaller size, it is typical to use RJ45 connectors with the magnetics incorporated. If the magnetics are discrete components, they have to respect a separation under of 25mm between them and the RJ45 connector, and 20mm or greater between them and the SMARC-314 connector.

There are also two outputs to manage LEDs. These LEDs are used to indicate the good functioning of the Ethernet connection. The first one (output GBE_LINK100#, usually a yellow LED) gives an indication about the line link (LED off for no link and LED on for valid link). The other (output GBE_LINK_ACT#, usually a green LED) gives an indication about the line activity: LED on indicates a valid link; when LED is blinking there is data traffic.

The following figure (also in the SMARC Design Guide) shows an example of connection diagram, using a RJ45 jack with integrated magnetics.

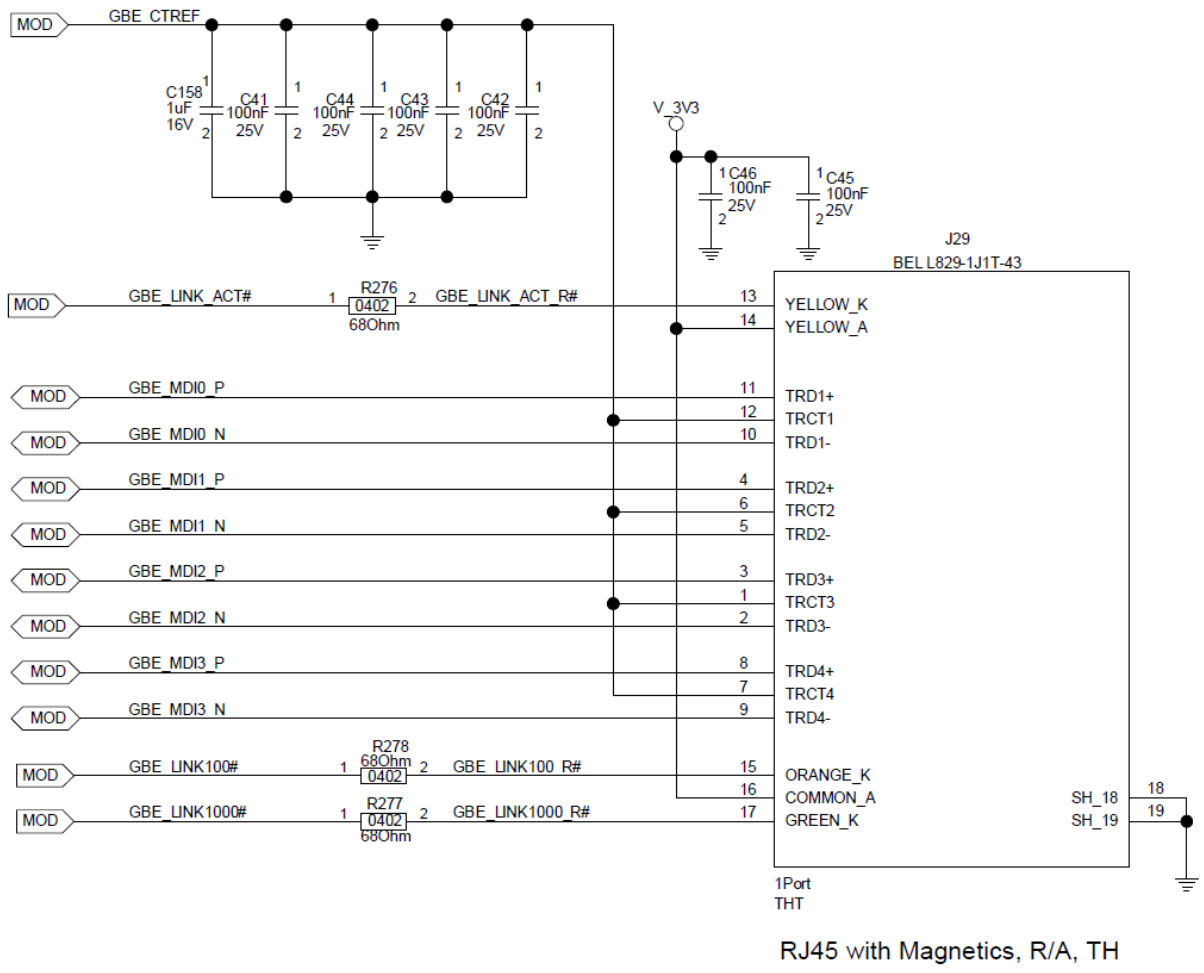


Figure 11 Ethernet Standard Circuit

Pin	Volt Level	Dev Pin	Main Function	Main MUX	Type	Fixed Function	Comments
P29	DIF	NC	GBE_MDI0-	NA	ETH	YES	Analog Transmit/Receive Data 0 Negative. Differential output to magnetics.
P30	DIF	NC	GBE_MDI0+	NA	ETH	YES	Analog Transmit/Receive Data 0 Positive. Differential output to magnetics.
P26	DIF	NC	GBE_MDI1-	NA	ETH	YES	Analog Transmit/Receive Data 1 Negative. Differential output to magnetics.
P27	DIF	NC	GBE_MDI1+	NA	ETH	YES	Analog Transmit/Receive Data 1 Positive. Differential output to magnetics.
P23	DIF	NC	GBE_MDI2-	NA	ETH	YES	Analog Transmit/Receive Data 2 Negative. Differential output to magnetics.
P24	DIF	NC	GBE_MDI2+	NA	ETH	YES	Analog Transmit/Receive Data 2 Positive. Differential output to magnetics.
P19	DIF	NC	GBE_MDI3-	NA	ETH	YES	Analog Transmit/Receive Data 3 Negative. Differential output to magnetics.
P20	DIF	NC	GBE_MDI3+	NA	ETH	YES	Analog Transmit/Receive Data 3 Positive. Differential output to magnetics.
P21	1V8	NC	GBE_LINK1 00#	NA	OUT	YES	Active Low. Means 1000/100 Mbps speed. Inactive if 10 Mbps.
P22	NC	NC	GBE_LINK1 000#	NA	NC	NC	No connected
P25	1V8	NC	GBE_LINK_ ACT#	NA	OU T	YES	Active Low. Indicates valid link and blinks when there is activity.
P28	NC	NC	GBE_CTREF	NA	NC	NC	No connected

Table 8 Ethernet Pins

4.5 USB CONNECTIONS

There are two possibilities to connect the module to other USB devices: with a standard Host base and with an OTG (On-The-Go) interface.

The USB 2.0 Host connection is provided for connecting other devices acting as Clients of the module (for example, an external HDD). The SMARC-314 connector lines referred to this function are adapted for a USB type A receptacle, see wiring example in the following figure (also in the SMARC Design Guide).

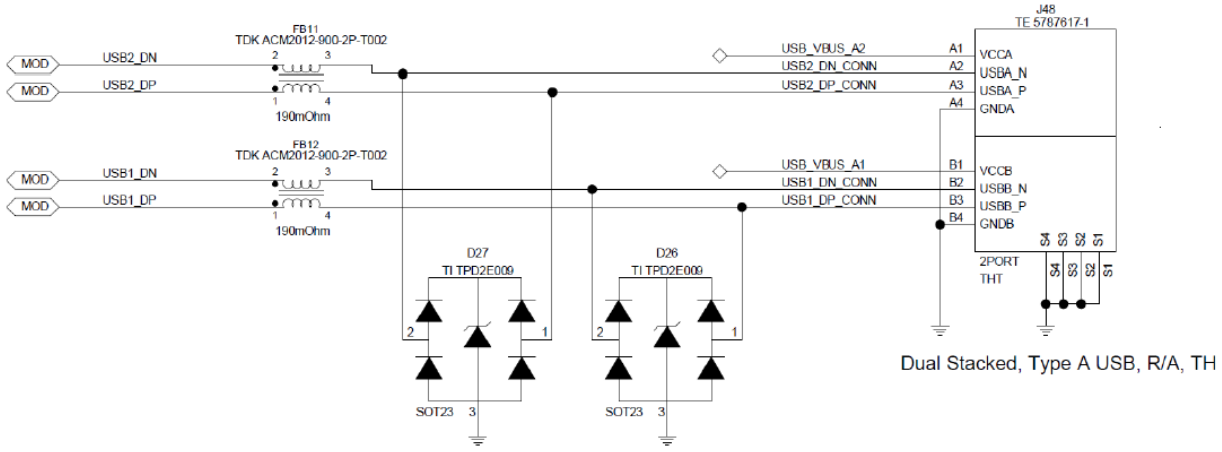


Figure 12 USB 2.0 Host Connections

The USB 2.0 OTG connection allows the configuration of the board as Host or Client in function of the wire of connection used for linking both devices (the module and the external device; adapting the SMARC-314 connector lines for an USB type AB). It is defined by the pin P64 (USB0_OTG_ID): when the board detects this pin connected at ground, it will be an A-device; if the pin is floating (NC) it will be a B-device. The following figure shows the connections (also in SMARC Design Guide).

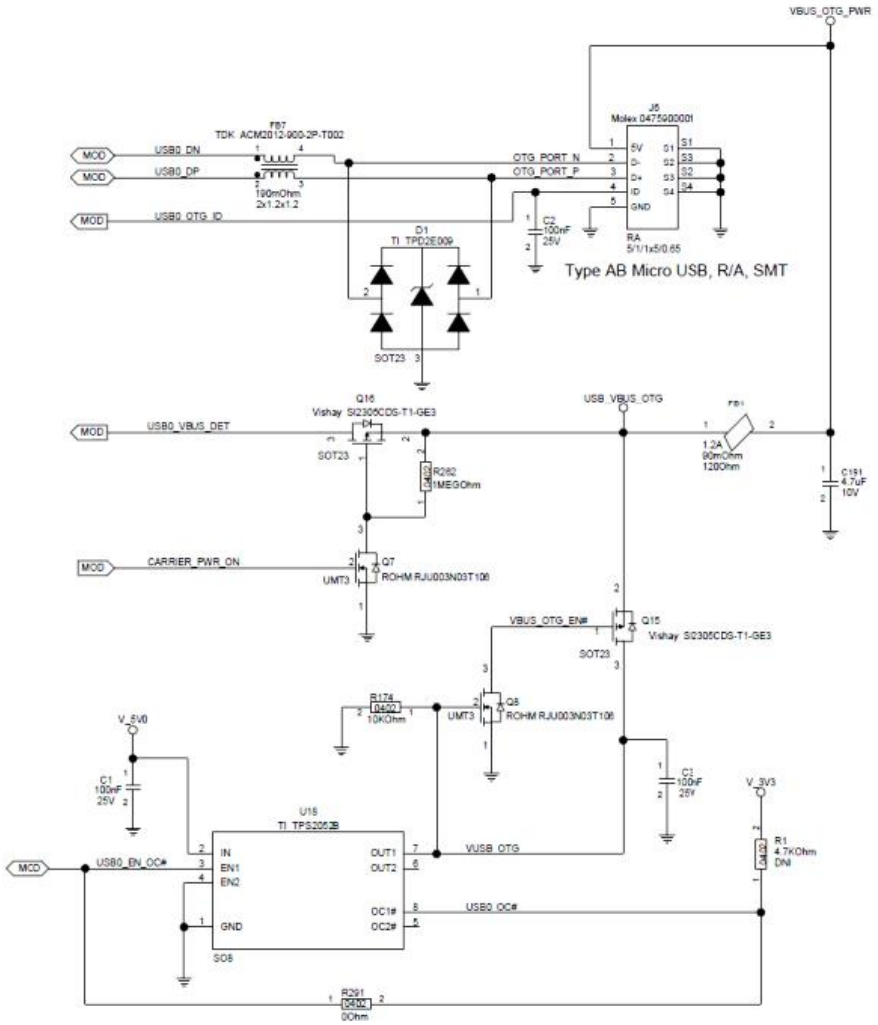


Figure 13 MicroUSB AB 2.0 OTG Connections

The USB0_EN_OC# (P62) and USB1_EN_OC# (P67) are, in both cases, optional pins used to detect if there has been an over-consumption (for example, a short-circuit). Although in the second example these references are used, it is possible to apply any other of the free GPIO pins to implement this feature.

It must be respected a 90Ω (+/-15%) differential impedance in the layout traces when the base board is designed. At the same time, the traces have to be equal length and symmetric, with regards to shape,

length, and via count. The differential pairs must be isolated from nearby signals and circuitry to maintain signal integrity.

To protect the VBUS against overcurrent, the USB power source current have to be less or equal than 500mA, and the user must provide a protection in the base board as it is shown in Figure 12 USB 2.0 Host connections and Figure 13 MicroUSB AB 2.0 OTG connections examples.

The following table shows the SMARC-314 related pins for both USB connections.

Pin	Volt Level	Dev Pin	Main Function	Main MUX	Type	Fixed Function	Comments
USB HOST							
P65	DIF	E10	USB1+	0	USB2.0	YES	Analog D+ data pin of the USB1
P66	DIF	F10	USB1-	0	USB2.0	YES	Analog D- data pin of the USB1
P67	3V3	R6	USB1_EN_OC#	5	IO	YES	Active Low. Over current Indication to module. This signal has a 3K3 PU resistor.
USB OTG							
P60	DIF	A6	USB0+	0	USB2.0	YES	Analog D+ data pin of the USB0
P61	DIF	B6	USB0-	0	USB2.0	YES	Analog D- data pin of the USB0
P62	3V3	R4	USB0_EN_OC#	5	IO	YES	Active Low. Over current Indication to module. This signal has a 3K3 PU resistor.
P63	5V	E9	USB0_VBUS_DET	0	USB	YES	USB host power detection, when this port is used as a device
P64	1V8	W23	USB0_OTG_ID	0	IN	YES	USB OTG ID input, active high

Table 9 USB Pins

4.6 I2C: INTER-INTEGRATED CIRCUIT INTERFACE

The MitySOM-iMX6 module can be connected to other peripheral devices by four I2C serial buses. There are eight pins in the SMARC-314 that may be used for this application: I2C_CAM_DAT, I2C_CAM_CK, I2C_GP_DAT, I2C_GP_CK, I2C_LCD_DAT, I2C_LCD_CK, I2C_PM_DAT and I2C_PM_CK.

The MitySOM-iMX6 uses a 1V8 voltage levels for I2C buses. In some cases, bidirectional voltage translators should be necessary to adapt voltage levels between ICs. It is important to note that an EEPROM is connected to I2C3 (address 0x50) and MMPF0100 is connected to I2C2 (address 0x08). See figure below (Also shown in SMARC Design Guide).

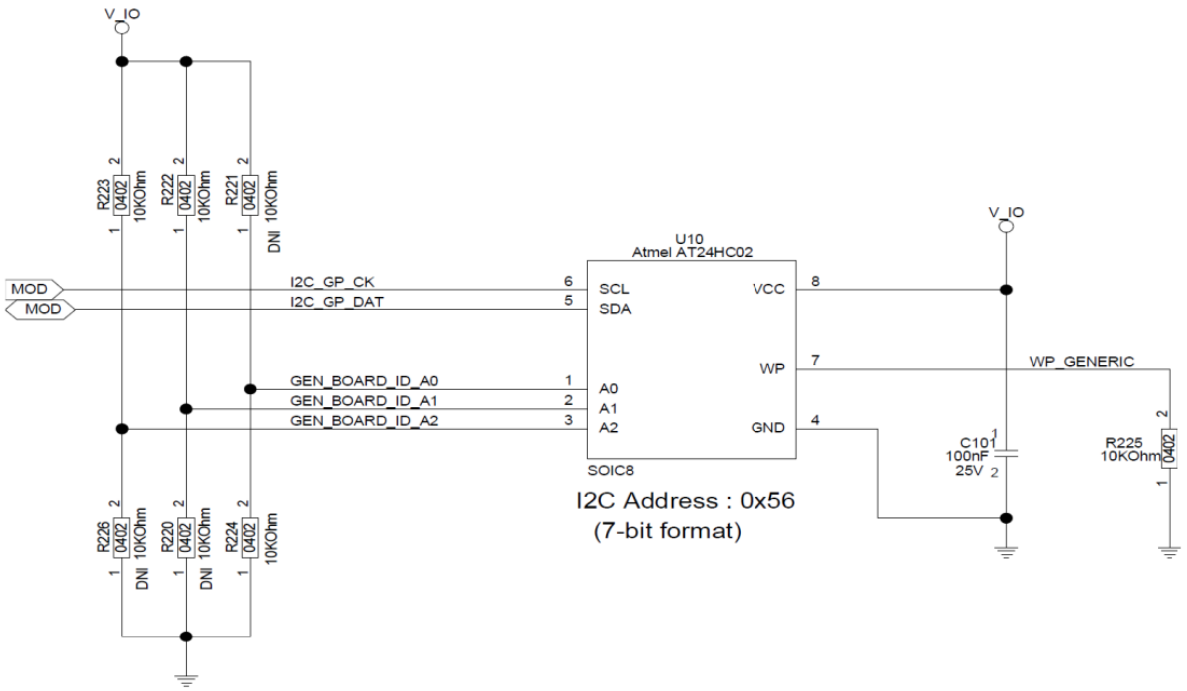


Figure 14 I2C Example: EEPROM Connection

Pin	Volt Level	Dev Pin	Main Function	Main MUX	Type	Fixed Function	Comments
1ST I2C							
S5	1V8	H20	I2C_CAM_CK	6	IO	YES	I2C1 bus clock. This signal has a 1K5 PU resistor.
S7	1V8	G23	I2C_CAM_DAT	1	IO	YES	I2C1 bus data. This signal has a 1K5 PU resistor.
2ND I2C							
S48	1V8	F21	I2C_GP_CK	6	IO	YES	I2C3 bus clock. This signal has a 1K5 PU resistor.
S49	1V8	D24	I2C_GP_DAT	6	IO	YES	I2C3 bus data. 0x50 is used. This signal has a 1K5 PU resistor.
3RD I2C							
P121	1V8	U5	I2C_PM_CK	4	IO	YES	I2C2 bus clock. This signal has a 1K5 PU resistor.
P122	1V8	T7	I2C_PM_DAT	4	IO	YES	I2C2 bus data. 0x08 is used. This signal has a 1K5 PU resistor.
4TH I2C							
S139	1V8	E15	I2C_LCD_CK	9	IO	YES	I2C4 bus clock. This signal has a 1K5 PU resistor. Solo/DualLite version.
		H20		6	IO	YES	I2C1 bus clock. This signal has a 1K5 PU resistor. Dual/Quad version.
S140	1V8	D16	I2C_LCD_DAT	9	IO	YES	I2C4 bus data. This signal has a 1K5 PU resistor. Solo/DualLite version.
		G23		1	IO	YES	I2C1 bus data. This signal has a 1K5 PU resistor. Dual/Quad version.

Table 10 I2C Pins

4.7 PWM: PULSE-WIDTH MODULATION

If control over other devices via a Pulse-Width Modulation (PWM) is needed, the module offers a PWM peripheral with 16 bits time-base with Period and Frequency control and two outputs.

Max PWM frequency is 66 MHz. More information can be found in Section 52 of the iMX6 Applications Processor Reference Manual. The following figure shows a simple example in which the PWM signal is sent to a RC-filter.

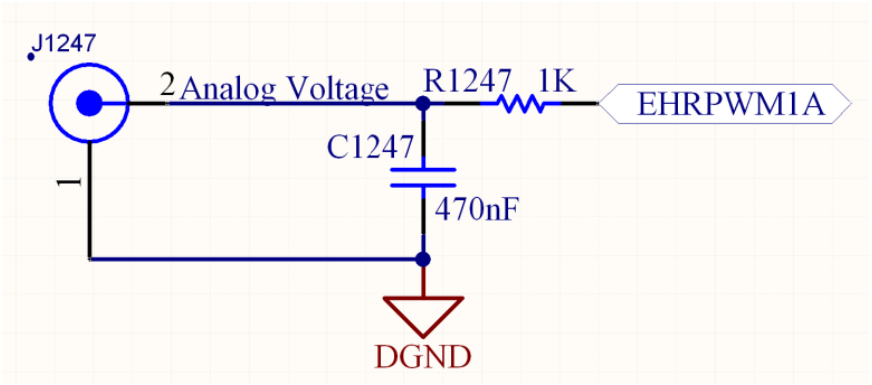


Figure 15 PWM Example: RC Filter

Pin	Volt Level	Dev Pin	Main Function	Main MUX	Type	Fixed Function	Comments
S18	1V8	B19	AFB1_OUT	2	OUT	NO	PWM output 3
P113	1V8	R22	PWM1_OUT	2	IO	NO	PMW Output 1 or General purpose input/output
S141	1V8	F17	LCD_BKLT_PWM	2	OUT	NO	Display Backlight. PMW output 4.

Table 11 PWM Pins

4.8 SPI: SERIAL PERIPHERAL INTERFACE

The Serial Peripheral Interface (SPI) is another possibility to connect the module to external peripherals. It is a full duplex synchronous bus, supporting a single master and up to two slave devices each SPI peripheral.

The MitySOM-iMX6 uses a 1V8 voltage levels for SPI buses. In some cases, voltage translators should be necessary to adapt voltage levels between ICs. It is important to note that a SPI NOR flash is connected through SPI3 and SPI3_CS0 (it is optional).

The next figure shows an example of how to connect the MitySOM-iMX6 module to a SPI Flash Socket (also shown in the SMARC Design Guide).

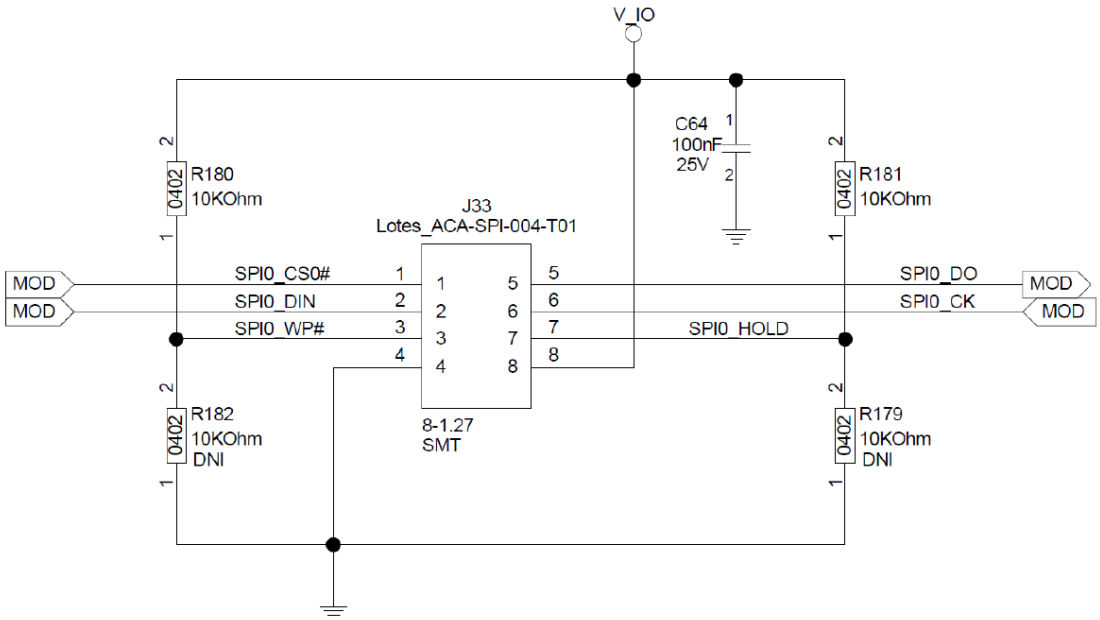


Figure 16 SPI example: SPI Flash Socket

Pin	Volt Level	Dev Pin	Main Function	Main MUX	Type	Fixed Function	Comments
P31	1V8	R25	SPI0_CS1#	2	OUT	NO	SPI3 chip select 2 signal
P43	1V8	P20	SPI0_CS0#	2	OUT	NO	SPI3 chip select 1 signal
P44	1V8	P24	SPI0_CK	2	OUT	YES	SPI3 clock
P45	1V8	P23	SPI0_DIN	2	IN	YES	SPI3 Master Input-Slave Output (MISO)
P46	1V8	P22	SPI0_DO	2	OUT	YES	SPI3 Master Output-Slave Input (MOSI)
P54	1V8	V25	SPI1_CS0#	2	OUT	NO	SPI2 chip select 0 signal
P55	1V8	T22	SPI1_CS1#	2	OUT	NO	SPI2 chip select 1 signal
P56	1V8	H24	SPI1_CK	2	OUT	NO	SPI2 clock
P57	1V8	J24	SPI1_DIN	2	IN	NO	SPI2 Master Input-Slave Output (MISO)
P58	1V8	J23	SPI1_DO	2	OUT	NO	SPI2 Master Output-Slave Input (MOSI)

Table 12 SPI Pins

4.9 MMC: MULTI MEDIA CARD INTERFACE

The MitySOM-iMX6 has three MMC (Multi Media Card) interfaces. The first one (MMC1) is connected to SDIO SMARC pins (as it is shown in Table 13 MMC pins), the second one (MMC2) is used for the on-board WiFi module and the third one (MMC3) is used in on-board eMMC flash.

The following example shows how to connect a uSD card reader to SDIO pins (also shown in SMARC Design Guide).

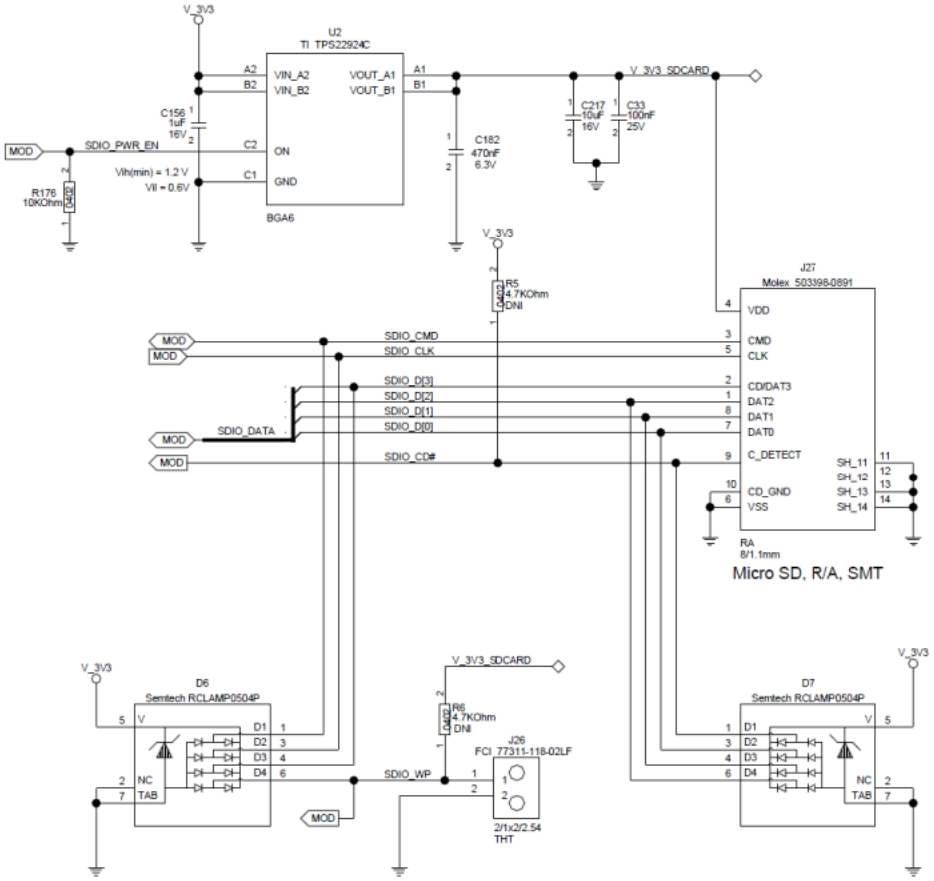


Figure 17 MMC Example: uSD Card Reader

Pin	Volt Level	Dev Pin	Main Function	Main MUX	Type	Fixed Function	Comments
P33	3V3	T2	SDIO_WP	6	IN	YES	MMC1 Write Protect. This signal has a 3K3 PU resistor.
P34	3V3	B21	SDIO_CMD	0	IO	NO	MMC1 Command
P35	3V3	T4	SDIO_CD#	6	IN	YES	MMC1 Card Detect. This signal has a 3K3 PU resistor.
P36	3V3	D20	SDIO_CK	0	IO	NO	MMC1 Clock
P37	3V3	F22	SDIO_PWR_EN	5	OUT	NO	MMC1 Card Power Enable
P39	3V3	A21	SDIO_D0	0	IO	NO	MMC1 Data Bus 0
P40	3V3	C20	SDIO_D1	0	IO	NO	MMC1 Data Bus 1
P41	3V3	E19	SDIO_D2	0	IO	NO	MMC1 Data Bus 2
P42	3V3	F18	SDIO_D3	0	IO	NO	MMC1 Data Bus 3

Table 13 MMC pins

4.10 UART: UNIVERSAL ASYNCHRONOUS RECEIVER-TRANSMITTER

There are three defined UART devices in the module in order to control serial devices or debug via serial. They are available in the SMARC-314 in three blocks of pins.

The MitySOM-iMX6 uses a 1V8 voltage levels for UART buses. In some cases, voltage translators are necessary to adapt voltage levels between ICs.

The MitySOM-iMX6 uses UART2 as a Kernel Debug Peripheral. This UART is an inexpensive method to detect and repair system issues. It is advisable to use another UART instead of UART2 to preserve this functionality. The next figure shows how to connect the UART SMARC pins (also shown in SMARC Design Guide).

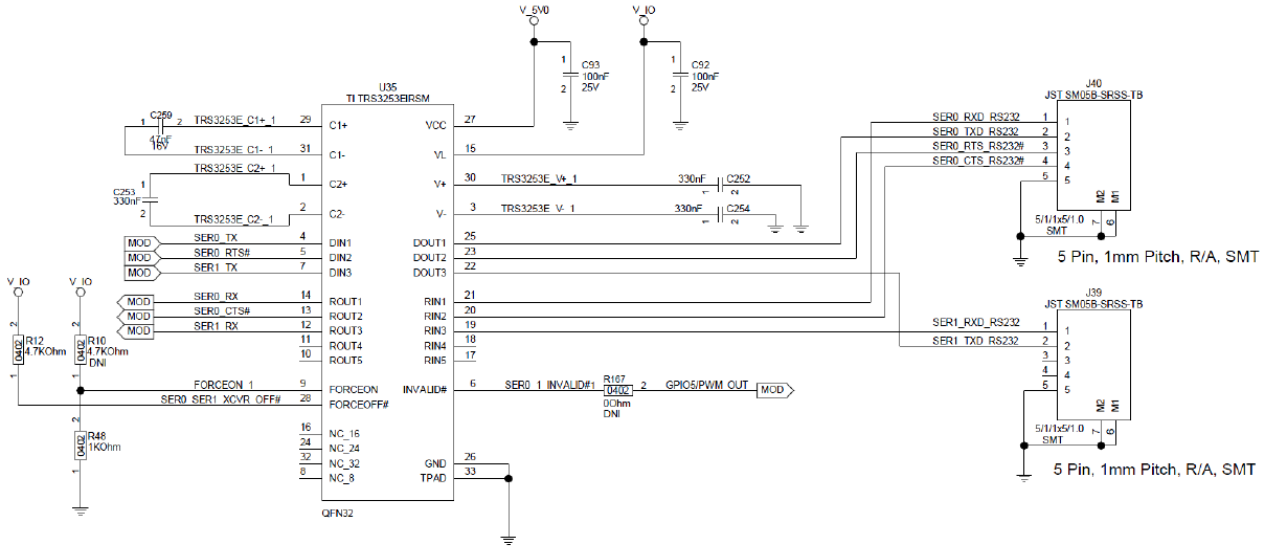
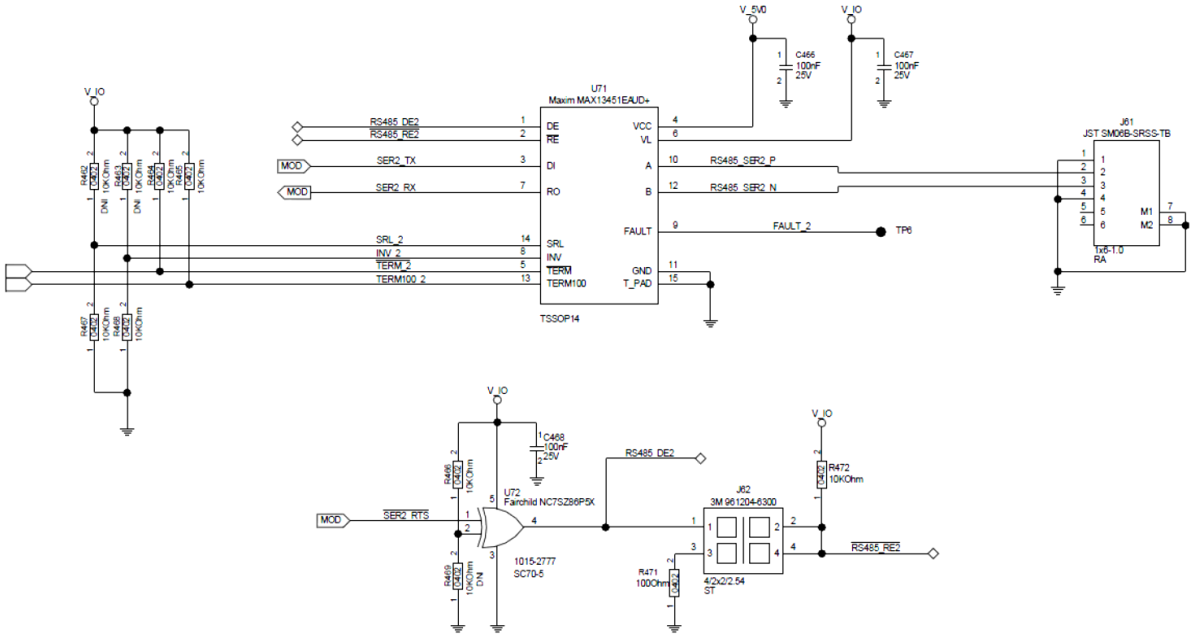


Figure 18 UART SMARC connections

The following figure shows another example of how to use the UART SMARC pins as RS485 bus (also shown in SMARC Design Guide).



Jumper 01-02	Jumper 03-04	State
Open	Open	RS485 reciever disabled
Open	Closed	RS485 reciever always enabled
Closed	Open	RS485 reciever enbled when transmitter disabled
Closed	Closed	Invalid

Figure 19 RS485 Example: RS485 Circuit

Pin	Volt Level	Dev Pin	Main Function	Main MUX	Type	Fixed Function	Comments
1ST UART							
P134	1V8	E24	SER1_TX	4	OUT	NO	Debug UART2 Transmit Data Output
P135	1V8	E25	SER1_RX	4	IN	NO	Debug UART2 Receive Data Input
2ND UART							
P136	1V8	B17	SER2_TX	2	OUT	NO	UART3 Transmit Data Output
P137	1V8	E16	SER2_RX	2	IN	NO	UART3 Receive Data Input
P138	1V8	H21	SER2_RTS#	4	OUT	NO	UART3 CTSn Output
P139	1V8	J20	SER2_CTS#	4	IN	NO	UART3 RTSn Input
3RD UART							
P140	1V8	M2	SER3_TX	3	OUT	NO	UART4 Transmit Data Output
P141	1V8	L1	SER3_RX	3	IN	NO	UART4 Receive Data Input

Table 14 UART Pins

4.11 CAN BUS: CONTROLLER AREA NETWORK

The module can be integrated in a global system using the serial standard CAN Bus. CAN Bus is a standard designed to allow microcontrollers and devices to communicate with each other without a host computer. It is a differential half duplex data bus, using shielded or unshielded twisted differential pair wiring, with an impedance termination of 120Ω at the endpoints of the bus. Nodes on the bus are arranged in daisy-chain fashion.

A CAN Transceiver is needed on the baseboard to connect the system to the CAN Bus. The following example (also shown in SMARC Design Guide) shows this application using the NCV7341 chip (a high-speed CAN Transceiver).

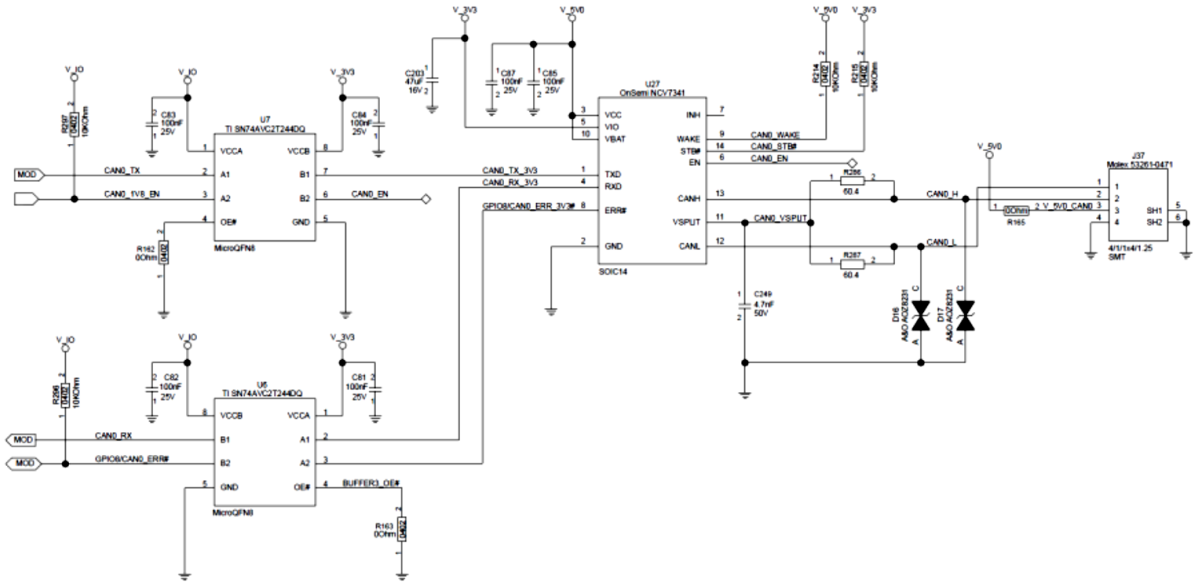


Figure 20 CAN Bus Circuit Example

Pin	Volt Level	Dev Pin	Main Function	Main MUX	Type	Fixed Function	Comments
P143	1V8	R3	CAN0_TX	3	OUT	NO	CAN1 Transmission Line
P144	1V8	W4	CAN0_RX	2	IN	NO	CAN1 Reception Line
P145	1V8	T6	CAN1_TX	0	OUT	NO	CAN2 Transmission Line
P146	1V8	V5	CAN1_RX	0	IN	NO	CAN2 Reception Line

Table 15 CAN Pins

4.12 I2S: SERIAL AUDIO PORT

I2S is a synchronous serial bus used for interfacing digital audio devices such as Audio CODECs and DSP chips. Generally, PCM audio data is transmitted over the I2S interface. The I2S bus may have a single bidirectional data line or two separate data lines. The signals constituting the I2S bus are a serial clock/bit clock (output from the master), a left right clock (output from the master) that indicates the channel being transmitted and a single bidirectional data line or two data lines - one input and one output. A SMARC module can generally be configured as I2S master or slave.

The following example is a depiction of a connected Stereo CODEC with Headphone AMP to the Serial Audio Port (also shown in SMARC Design Guide).

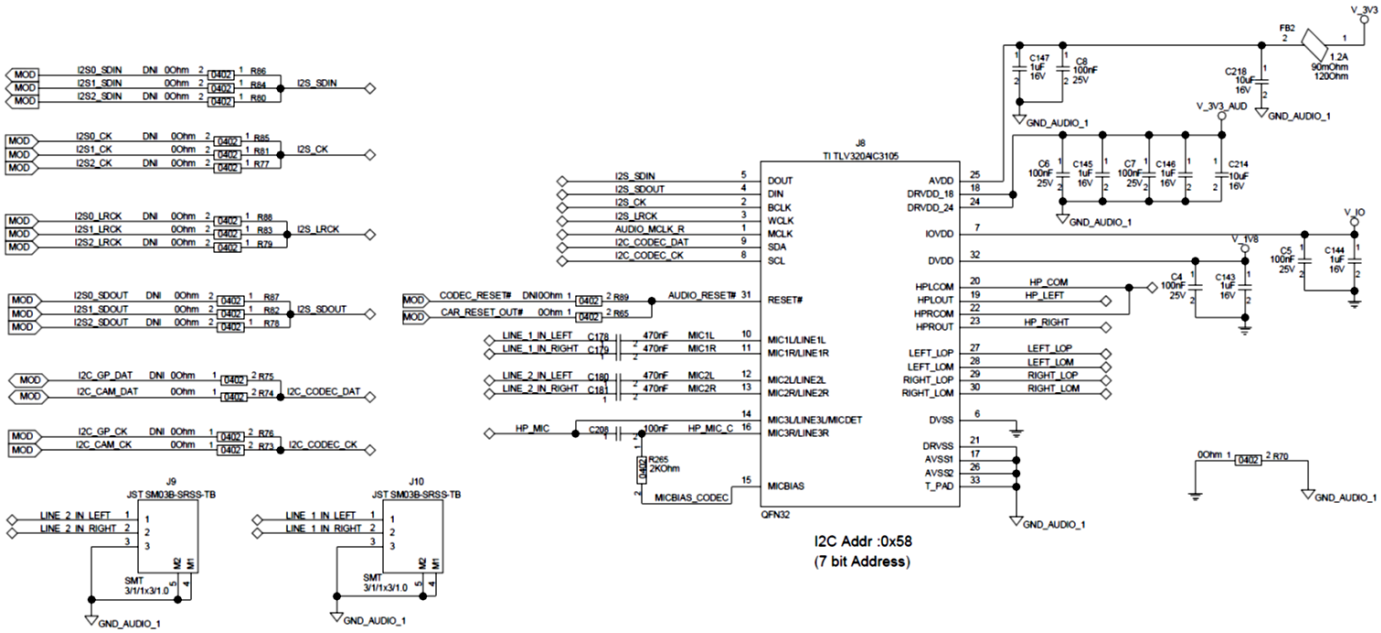


Figure 21 I2S Example: Stereo CODEC with Headphone AMP

Pin	Volt Level	Dev Pin	Main Function	Main MUX	Type	Fixed Function	Comments
S38	1V8	P4	AUDIO_MCK	3	OUT	NO	Master clock output to Audio codecs (CCM_CLKO1)
S39	1V8	V24	I2S0_LRCK	3	IO	NO	AUD4 Transmit Frame Sync signal
S40	1V8	T20	I2S0_SDOUT	3	OUT	NO	AUD4 Data Transmit signal
S41	1V8	W24	I2S0_SDIN	3	IN	NO	AUD4 Data Receive signal
S42	1V8	U22	I2S0_CK	3	IO	NO	AUD4 Transmit Clock signal

Table 20 MIPI-CSI Pins

4.13 GPIO: GENERAL PURPOSE INPUT OUTPUT

GPIOs are input/output (IO) general purpose pins used to control LEDs, relays, switch, etc. The following figure shows a basic circuit with an input pushbutton and two outputs to manage LED signals.

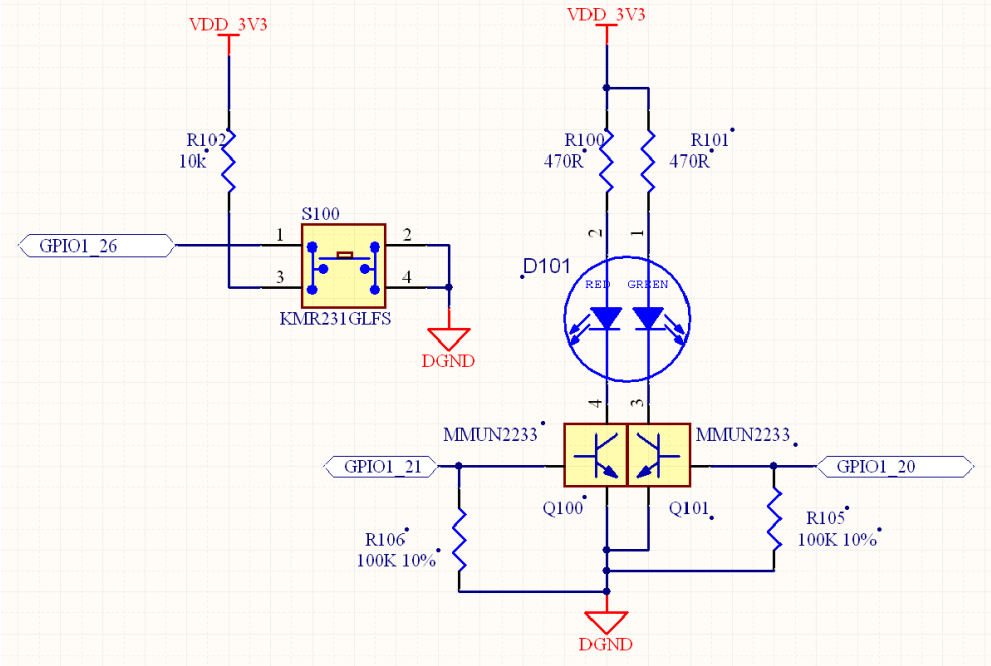


Figure 22 GPIOs Example: Control Circuit to Manage LEDs

Pin	Volt Level	Dev Pin	Main Function	Main MUX	Type	Fixed Function	Comments
P108	1V8	N1	GPIO0	5	IO	NO	General purpose input/output (GPIO5_IO22)
P109	1V8	P2	GPIO1	5	IO	NO	General purpose input/output (GPIO5_IO23)
P110	1V8	N4	GPIO2	5	IO	NO	General purpose input/output (GPIO5_IO24)
P111	1V8	N3	GPIO3	5	IO	NO	General purpose input/output (GPIO5_IO25)
P112	1V8	W6	GPIO4	5	IO	NO	General purpose input/output (GPIO4_IO10)
P113	1V8	R22	GPIO5 / PWM_OUT	2	IO	NO	PMW Output 1 or General purpose input/output
P114	1V8	R23	GPIO6	5	IO	NO	General purpose input/output (GPIO4_IO27)
P115	1V8	R24	GPIO7	5	IO	NO	General purpose input/output (GPIO4_IO28)
P116	1V8	N6	GPIO8	5	IO	NO	General purpose input/output (GPIO5_IO26)
P117	1V8	N5	GPIO9	5	IO	NO	General purpose input/output (GPIO5_IO27)
P118	1V8	R21	GPIO10	5	IO	NO	General purpose input/output (GPIO4_IO31)
P119	1V8	T23	GPIO11	5	IO	NO	General purpose input/output (GPIO5_IO05)

Table 21 GPIO Pins

4.14 SATA: Serial ATA

SATA is a high speed point to point serial interface that connects a host system to a mass storage device such as rotating hard drive, solid state drive, or an optical drive. Data and clock are serialized onto a single outbound differential pair and a single inbound pair. Data link rates of 1.5, 3.0, and 6.0 Gbps are defined by the SATA specification. A SATA link is AC coupled, but the coupling capacitors are defined in the SMARC specification to be on the module, for both SATA transmit and receive pairs.

The following figure shows how to connect SATA SMARC pins to mSATA connector (also shown in SMARC Design Guide).

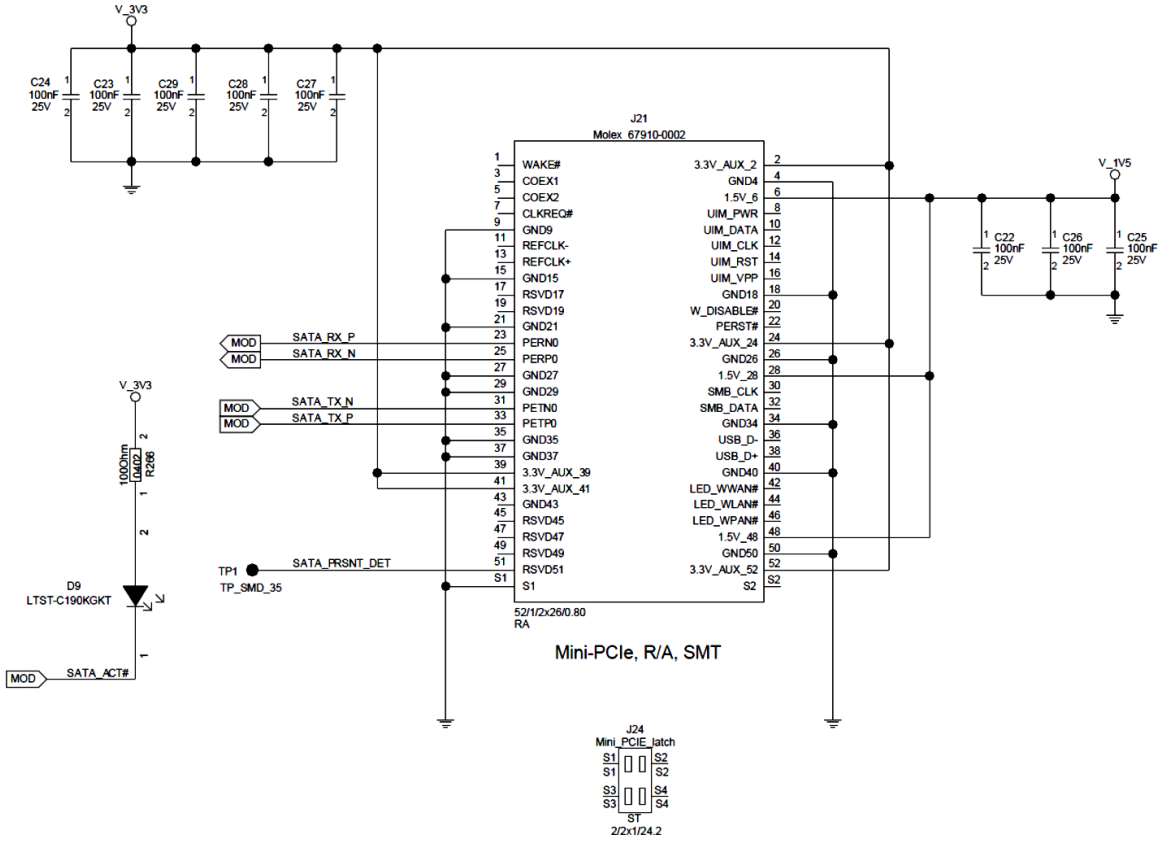


Figure 23 SATA Connection Example

Pin	Volt Level	Dev Pin	Main Function	Main MUX	Type	Fixed Function	Comments
P48	DIF	A12	SATA_TX+	0	SATA 3 Gb/s	YES	Differential SATA transmit data +. This signal has a 10 nF coupling capacitor.
P49	DIF	B12	SATA_TX-	0	SATA 3 Gb/s	YES	Differential SATA transmit data -. This signal has a 10 nF coupling capacitor.
P51	DIF	B14	SATA_RX+	0	SATA 3 Gb/s	YES	Differential SATA receive data +. This signal has a 10 nF coupling capacitor.
P52	DIF	A14	SATA_RX-	0	SATA 3 Gb/s	YES	Differential SATA receive data -. This signal has a 10 nF coupling capacitor.
S54	3V3	T24	SATA_ACT #	5	OUT	NO	Active low SATA activity indicator

Table 22 SATA Pins

4.15 PCIe

PCI Express (or PCIe) is a scalable, point-to-point serial bus interface commonly used for high speed data exchange between a PCIe host, or root, and a target device. It is scalable in the sense that there may be link widths, per the PCIe specification, that are x1, x2, x4, x8, x16 or x32. SMARC currently calls out only x1 operation. A PCIe link is AC coupled, but the coupling capacitors are defined in the SMARC specification to be on the Module, for only PCIe transmit pair.

The following figure shows how to connect PCIe SMARC pins to Mini-PCIe connector (also shown in SMARC Design Guide).

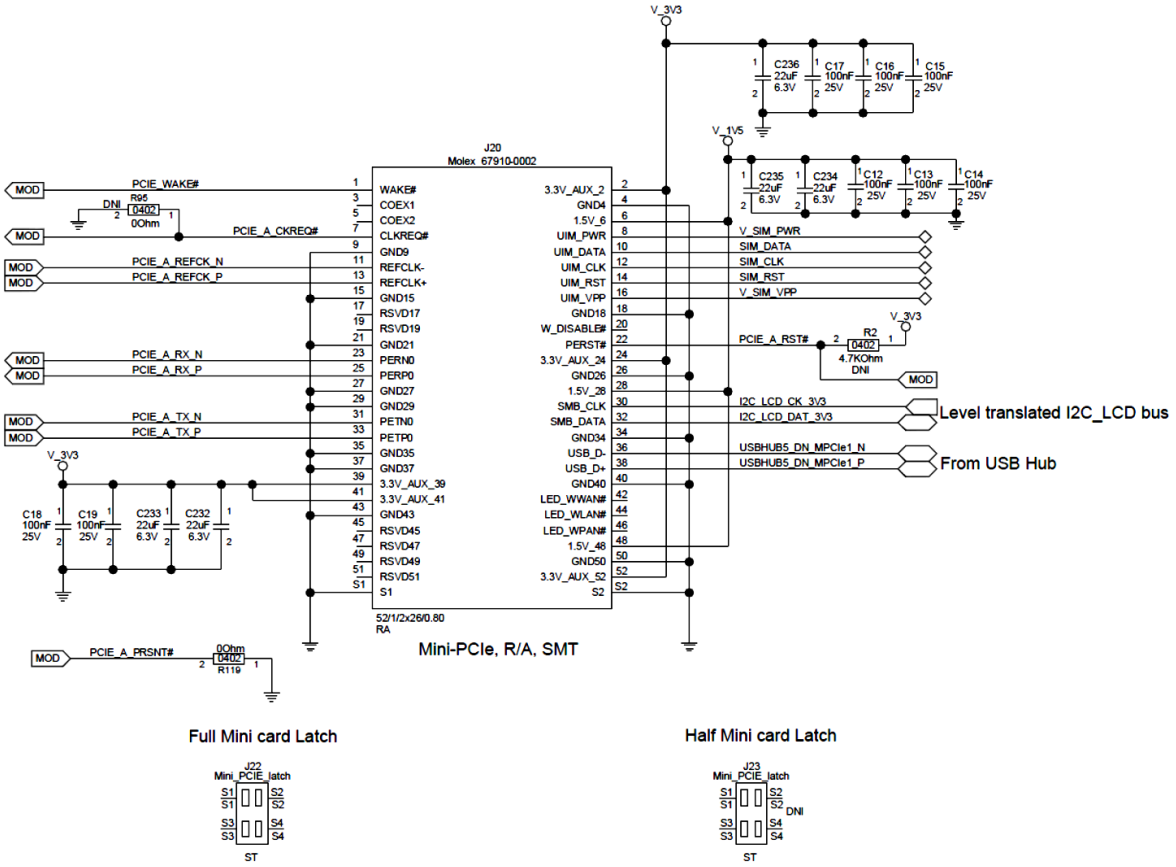


Figure 24 PCIe Connection Example

Pin	Volt Level	Dev Pin	Main Function	Main MUX	Type	Fixed Function	Comments
P83	DIF	D7	PCIE_A_REFCK +	0	LVDS TIA/EIA-644	YES	Differential PCIe Link A reference clock output DC coupled +
P84	DIF	C7	PCIE_A_REFCK-	0	LVDS TIA/EIA-644	YES	Differential PCIe Link A reference clock output DC coupled -
P86	DIF	B2	PCIE_A_RX+	0	LVDS TIA/EIA-644	YES	Differential PCIe Link A receive data pair 0 +
P87	DIF	B1	PCIE_A_RX-	0	LVDS TIA/EIA-644	YES	Differential PCIe Link A receive data pair 0 -
P89	DIF	B3	PCIE_A_TX+	0	LVDS TIA/EIA-644	YES	Differential PCIe Link A transmit data pair 0 +. This signal has a 0.1 uF coupling capacitor.
P90	DIF	A3	PCIE_A_TX-	0	LVDS TIA/EIA-644	YES	Differential PCIe Link A transmit data pair 0 -. This signal has a 0.1 uF coupling capacitor.
P74	3V3	U24	PCIE_A_PRSNT #	5	IN	YES	PCIe Port A present input. This signal has a 4K7 PU resistor.
P75	3V3	F15	PCIE_A_RST#	5	OUT	NO	PCIe Port A reset output
P78	3V3	T21	PCIE_A_CKREQ #	5	IN	YES	PCIe Port A clock request input. This signal has a 4K7 PU resistor.

Table 23 PCIe Pins

4.16 MIPI CSI

The Camera Serial Interface (CSI) is a specification of the Mobile Industry Processor Interface (MIPI) Alliance. It defines an interface between a camera and a host processor.

The following figure shows how to connect MIPI CSI signals to CSI camera (also shown in SMARC Design Guide). In this example OV3640 is used.

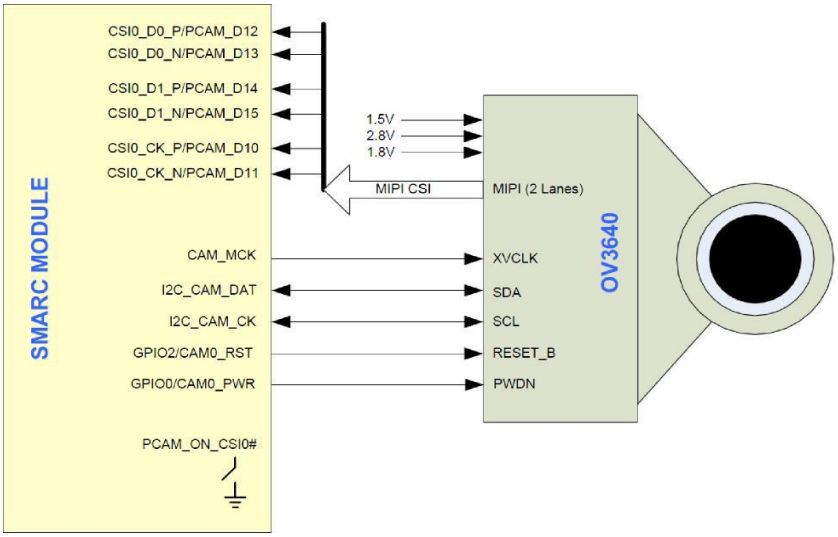


Figure 25 MIPI-CSI Connection Example

Pin	Volt Level	Dev Pin	Main Function	Main MUX	Type	Fixed Function	Comments
P3	DIF	F3	CSI1_CK+	0	MIPI CSI-2	YES	CSI1 differential clock input +
P4	DIF	F4	CSI1_CK-	0	MIPI CSI-2	YES	CSI1 differential clock input -
P7	DIF	E3	CSI1_D0+	0	MIPI CSI-2	YES	CSI1 differential data input D0 +
P8	DIF	E4	CSI1_D0-	0	MIPI CSI-2	YES	CSI1 differential data input D0 -
P10	DIF	D2	CSI1_D1+	0	MIPI CSI-2	YES	CSI1 differential data input D1 +
P11	DIF	D1	CSI1_D1-	0	MIPI CSI-2	YES	CSI1 differential data input D1 -
P13	DIF	E2	CSI1_D2+	0	MIPI CSI-2	YES	CSI1 differential data input D2 +
P14	DIF	E1	CSI1_D2-	0	MIPI CSI-2	YES	CSI1 differential data input D2 -
P16	DIF	F1	CSI1_D3+	0	MIPI CSI-2	YES	CSI1 differential data input D3 +
P17	DIF	F2	CSI1_D3-	0	MIPI CSI-2	YES	CSI1 differential data input D3 -
S6	1V8	R7	CAM_MCK	4	OUT	NO	Master clock output for CSI camera support

Table 24 MIPI CSI Pins

4.17 MIPI DSI

The Display Serial Interface (DSI) is a specification by the Mobile Industry Processor Interface (MIPI) Alliance aimed at reducing the cost of display controllers in a mobile device. It is commonly targeted at LCD and similar display technologies. It defines a serial bus and a communication protocol between the host (source of the image data) and the device (destination of the image data).

SMARC does not define MIPI DSI output, but in the MitySOM-iMX6 it is connected to S68, S69, S71, S72, S74 and S75 pins as shown in the next table.

Pin	Volt Level	Dev Pin	Main Function	Main MUX	Type	Fixed Function	Comments
S68	DIF	H4	AFB_DIFF2+	0	MIPI DSI 1.01	YES	DSI differential clock +
S69	DIF	H3	AFB_DIFF2-	0	MIPI DSI 1.01	YES	DSI differential clock -
S71	DIF	G1	AFB_DIFF3+	0	MIPI DSI 1.01	YES	DSI differential data D0 +
S72	DIF	G2	AFB_DIFF3-	0	MIPI DSI 1.01	YES	DSI differential data D0 -
S74	DIF	H1	AFB_DIFF4+	0	MIPI DSI 1.01	YES	DSI differential data D1 +
S75	DIF	H2	AFB_DIFF4-	0	MIPI DSI 1.01	YES	DSI differential data D1 -

Table 25 MIPI DSI Pins

4.18 LVDS

The following figure shows how to connect LVDS display signals to the connector (also shown in SMARC Design Guide).

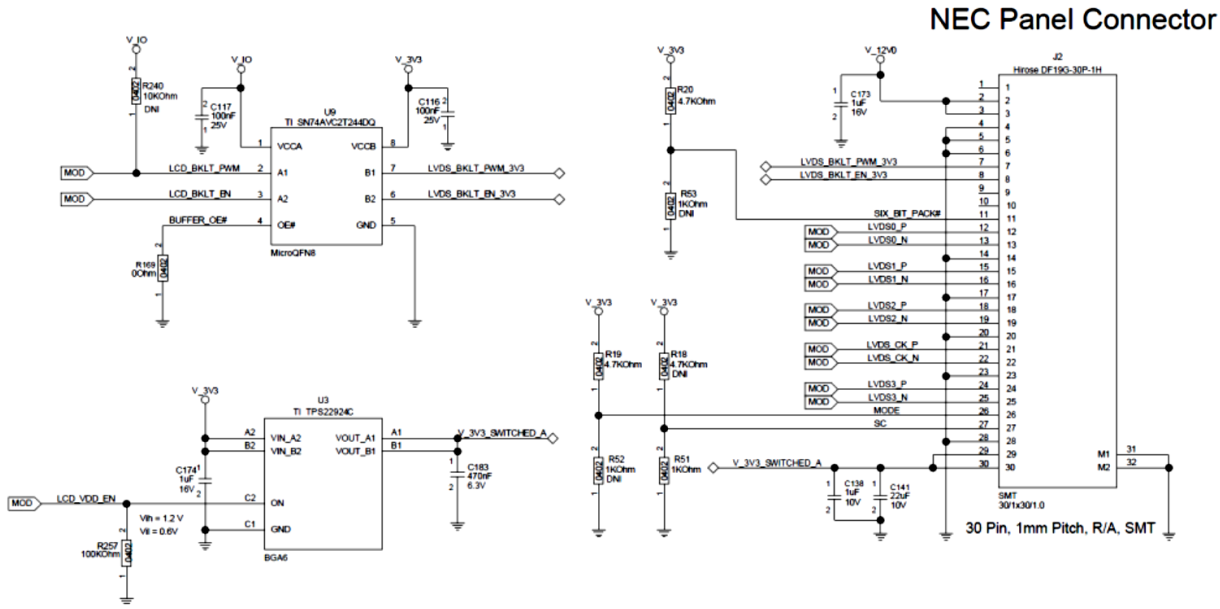


Figure 26 LVDS Connection Example

Pin	Volt Level	Dev Pin	Main Function	Main MUX	Type	Fixed Function	Comments
S125	DIF	U1	LVDS0+	0	LVDS TIA/EIA-644	YES	LVDS data channel differential pair D0 +
S126	DIF	U2	LVDS0-	0	LVDS TIA/EIA-644	YES	LVDS data channel differential pair D0 -
S128	DIF	U3	LVDS1+	0	LVDS TIA/EIA-644	YES	LVDS data channel differential pair D1 +
S129	DIF	U4	LVDS1-	0	LVDS TIA/EIA-644	YES	LVDS data channel differential pair D1 -
S131	DIF	V1	LVDS2+	0	LVDS TIA/EIA-644	YES	LVDS data channel differential pair D2 +
S132	DIF	V2	LVDS2-	0	LVDS TIA/EIA-644	YES	LVDS data channel differential pair D2 -
S134	DIF	V3	LVDS_CK+	0	LVDS TIA/EIA-644	YES	LVDS clock channel differential pair +
S135	DIF	V4	LVDS_CK-	0	LVDS TIA/EIA-644	YES	LVDS clock channel differential pair -
S137	DIF	W1	LVDS3+	0	LVDS TIA/EIA-644	YES	LVDS data channel differential pair D3 +
S138	DIF	W2	LVDS3-	0	LVDS TIA/EIA-644	YES	LVDS data channel differential pair D3 -

Table 26 LVDS Pins

4.19 HDMI

The SMARC HDMI data pairs may be routed directly from the SMARC Module pins to a suitable Carrier HDMI connector. Since HDMI is a hot-plug capable interface, it is important for the Carrier to implement ESD protection on all of the HDMI lines. The ESD protection on the data lines must be low capacitance so as not to degrade high speed signaling. The data lines must route through the ESD protection device pins in a no-stub fashion. The ESD protection should be located close to the HDMI connector.

The following figure shows how to connect SMARC HDMI pins to HDMI connector (also shown in SMARC Design Guide).

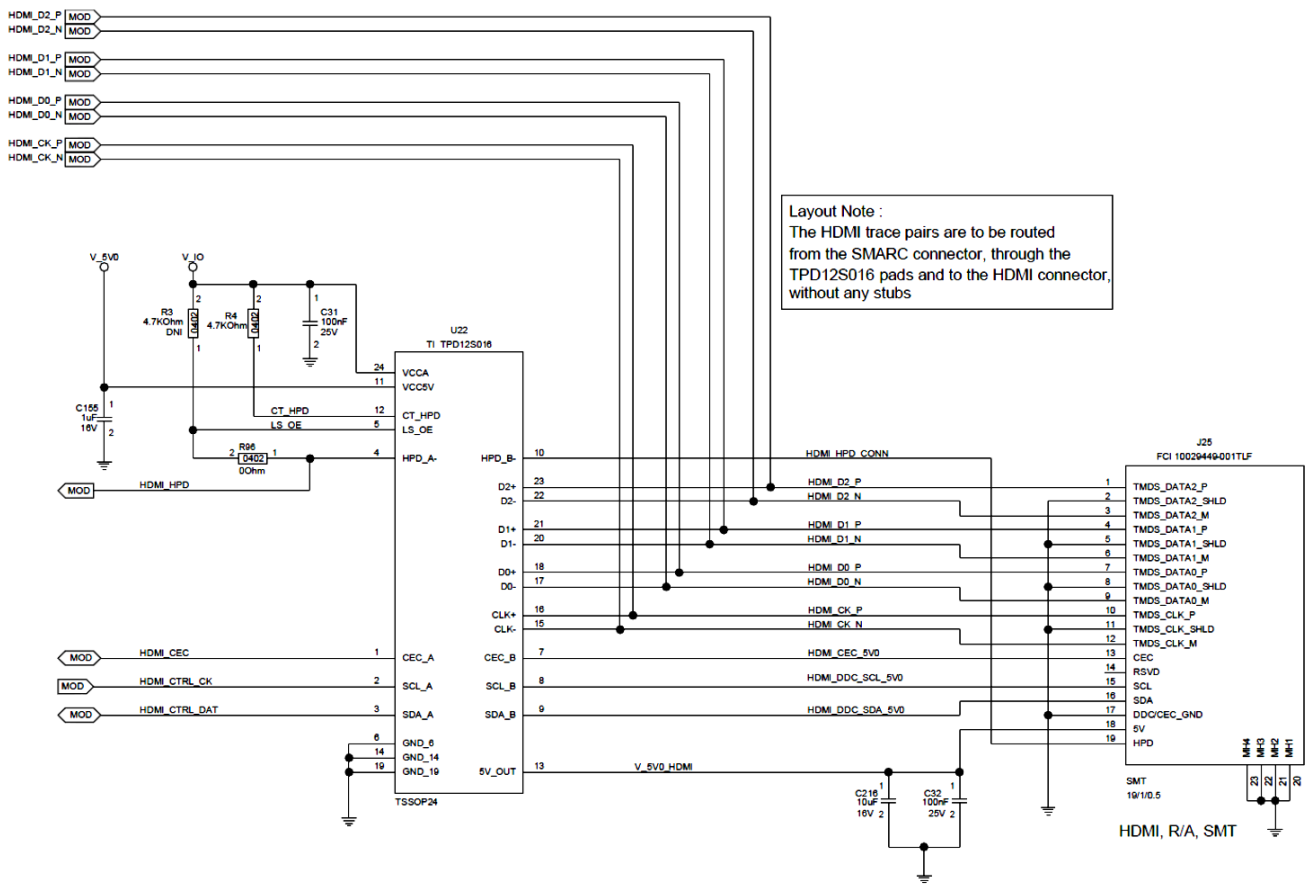


Figure 27 HDMI Connection Example

Pin	Volt Level	Dev Pin	Main Function	Main MUX	Type	Fixed Function	Comments
P92	DIF	K4	HDMI_D2+	0	HDMI 1.4a	YES	HDMI data differential pair D2 +
P93	DIF	K3	HDMI_D2-	0	HDMI 1.4a	YES	HDMI data differential pair D2 -
P95	DIF	J4	HDMI_D1+	0	HDMI 1.4a	YES	HDMI data differential pair D1 +
P96	DIF	J3	HDMI_D1-	0	HDMI 1.4a	YES	HDMI data differential pair D1 -
P98	DIF	K6	HDMI_D0+	0	HDMI 1.4a	YES	HDMI data differential pair D0 +
P99	DIF	K5	HDMI_D0-	0	HDMI 1.4a	YES	HDMI data differential pair D0 -
P101	DIF	J6	HDMI_CK+	0	HDMI 1.4a	YES	HDMI differential clock output pair +
P102	DIF	J5	HDMI_CK-	0	HDMI 1.4a	YES	HDMI differential clock output pair -
P104	1V8	K1	HDMI_HPD	0	HDMI 1.4a	YES	HDMI Hot Plug Detect input. This signal has a 47K PU resistor.
P105	1V8	U5	HDMI_CTRL_CK	4	HDMI 1.4a	YES	I2C2 bus clock. This signal has a 1K5 PU resistor.
P106	1V8	T7	HDMI_CTRL_DAT	4	HDMI 1.4a	YES	I2C2 bus data. 0x08 is used. This signal has a 1K5 PU resistor.
P107	1V8	H19	HDMI_CEC	6	HDMI 1.4a	YES	HDMI Consumer Electronics Control . This signal has a 47K PU resistor.

Table 27 HDMI Pins

4.20 SUPERVISOR

It is important to note that a supervisor is present in MitySOM-iMX6 sensing the 1V8 signal.

4.21 ENVIRONMENTAL SPECIFICATION

4.21.1 Temperature Specification

General _Specification	Operating	Non-operating
Commercial grade	0°C to +60°C	-30°C to +85°C
Industrial grade (E2)	-40°C to +85°C	-40°C to +85°C

Table 28 Temperature Specification

Standard modules are available for industrial grade temperature range.

The operating temperature is the maximum measurable temperature on any spot on the module's surface.

4.21.2 Humidity

- 93% relative Humidity at 40°C, non-condensing (according to IEC 60068-2-78).

4.22 STANDARDS AND CERTIFICATIONS

4.22.1 RoHS

The MitySOM-iMX6 is compliant to the directive 2002/95/EC on the restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment.

4.22.2 CE Marking

MitySOM-iMX6 is CE marked according to Low Voltage Directive 2006/95/EC – Test standard EN60950.

4.22.3 WEEE Directive

WEEE Directive 2002/96/EC is not applicable for SOMs.

4.22.4 Conformal Coating

Conformal Coating is available for SOMs and for validated SMARC-314 modules. Please contact info@criticallink.com for further details.

4.22.5 EMC

The MitySOM-iMX6 is designed and tested following EN55022 standard ("INFORMATION TECHNOLOGY EQUIPMENT. RADIO DISTURBANCE CHARACTERISTICS. LIMITS AND METHODS OF MEASUREMENT")

4.22.6 SMARC Form Factor Standard

SMARC ("Smart Mobility ARChitecture") is a versatile, small form factor computer module definition targeting applications that require low power, low costs, and high performance.

http://www.sget.org/standards/smarc.html

4.23 MTBF

The MitySOM-iMX6 has been designed with a predicted MTBF (Mean Time Before Failure) of >87,600 hours (>10 years)

All hardware components are selected with long time industrial reliability parameters. The MTBF prediction of hardware components and temperature stress could be estimated, but the newest devices are very software dependent. So, final software application has an important effect on MTBF.

4.24 MECHANICAL SPECIFICATION

4.24.1 Module Dimension

- 82 mm x 50 mm x 4 mm

4.24.2 Mechanical Drawing

The following figures show the MitySOM-iMX6 modules mechanical dimensions:

- All dimensions are in millimeters.
- 8 layer Printed Circuit Board size is 82x50x1.2mm.
- Mounting holes are provided, one on each corner.

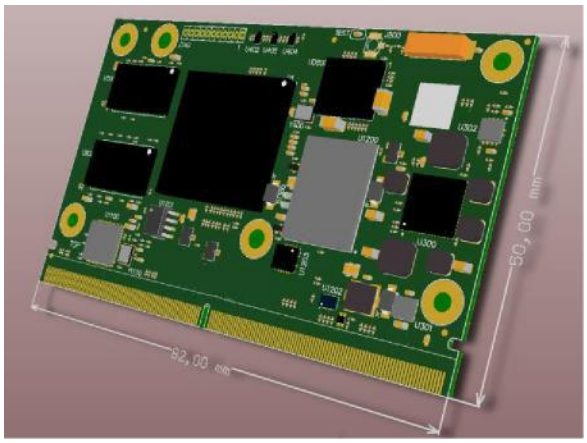


Figure 28 MitySOM-iMX6 Main Outline Dimensions

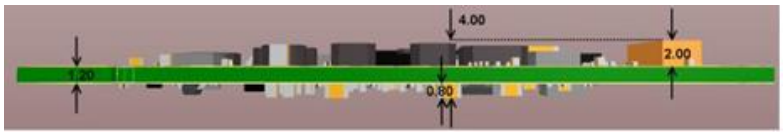


Figure 29 MitySOM-iMX6 Lateral View Widths Dimensions

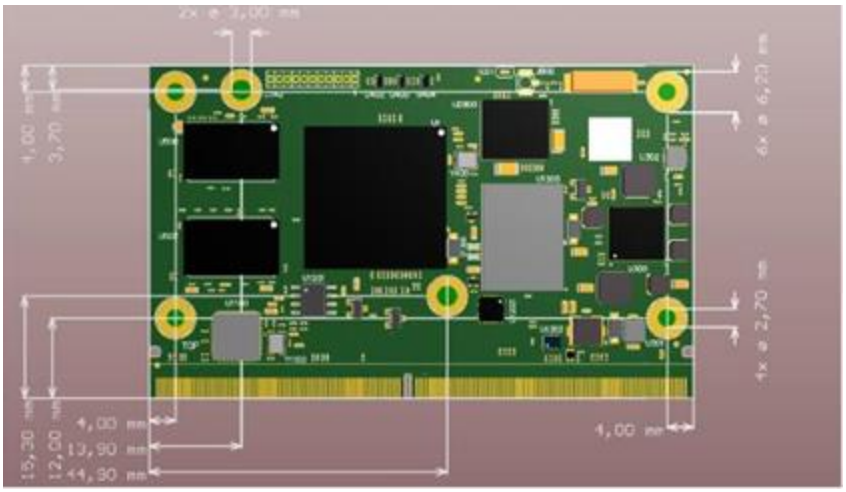


Figure 30 MitySOM-iMX6 Side View Detailed Mechanical Dimensions

5 ON-BOARD INTERFACES

5.1 SUMMARY

Device	Connector	Reference	Comments
LEDs	-	D1300 and D1301	GPIO controlled
JTAG	11pin 1.25mm pitch interface	J1300	
SMARC-314	314-pin SMARC interface	J900	Expand many functionalities from iMX6 processor

Table 29 Interface Summary

5.2 LEDs

The MitySOM-iMX6 module provides two bicolor LED indicator on the board. They can be controlled by the user.

Signal Name	LED Color	Description
DI0_PIN2	D1300 Red	DI0_PIN2 of iMX6
DI0_PIN3	D1300 Green	DI0_PIN3of iMX6
DI0_PIN4	D1301 Red	DI0_PIN4 of iMX6
DI0_PIN15	D1301 Green	DI0_PIN15 of iMX6

Table 30 LEDs

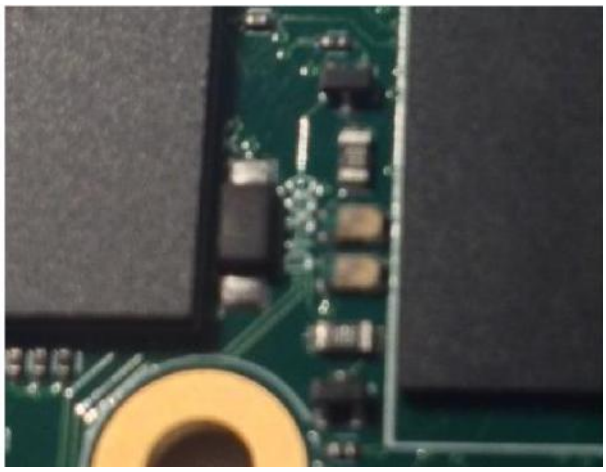


Figure 31 LEDs in the PCB

5.3 JTAG

The MitySOM-iMX6 provides a foot print JTAG interface to help you develop your code.

Figure 32 JTAG connector in the PCB

The following figure shows the pinout schematic and the corresponding metal contacts.

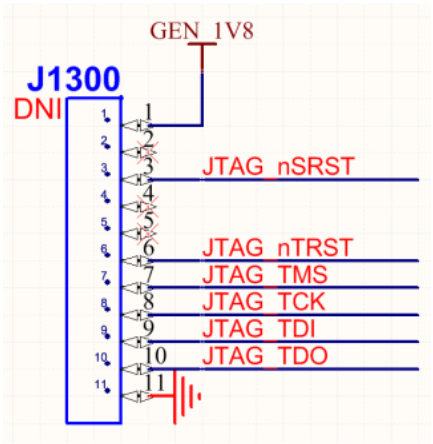


Figure 33 JTAG connector schematic

It is important to note that even pins are left unconnected but the footprint makes possible to use an 11 pin 1.27 mm pitch connector. The next table details the signals on each pin of J1300.

Signal Name	J1300 JTAG PIN	Description
GEN1V8	1	1.8V supply
NC	2	Not Connected
JTAGnSRST	3	System Reset Input Signal
NC	4	Not connected
NC	5	Not connected
JTAGnTRST	6	JTAG Test Reset Input Signal
JTAGTMS	7	JTAG Test Mode Select Input Signal
JTAGTCK	8	JTAG Test Clock Input Signal
JTAGTDI	9	JTAG Test Data Input Signal
JTAGTDO	10	JTAG Test Data Output Signal
GND	11	Ground

Table 31 JTAG pinout

For additional details about JTAG, please refer to iMX6 Applications Processor Reference Manual.

6 SMARC-314 EXPANSION CONNECTOR INTERFACE

The MitySOM-iMX6 has 1 SMARC-314 interface (J900) composed by 314 metal contacts, 156 on the TOP side and 158 on the BOTTOM side, providing source power and 1V8 CMOS signals to support lots of features of iMX6 processor that can be used in your custom baseboard. The next figure shows the area and pin numbering of the SMARC-314 interface:

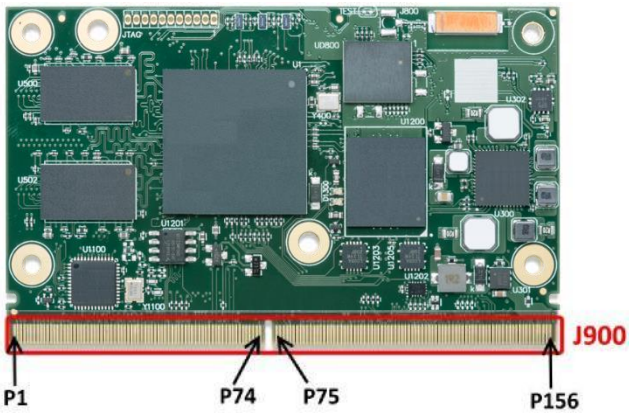


Figure 34 J900 SMARC-314 Interface Area (TOP SIDE)

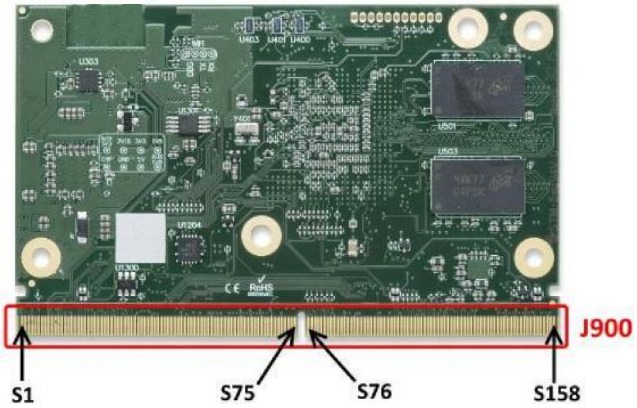


Figure 35 J900 SMARC-314 Interface Area (BOTTOM SIDE)

The MitySOM-iMX6 modules can be inserted like a target through this SMARC-314 interface to any of the standard SMARC-314 connectors existing on the market. Some valid references are:

MANUFACTURER	PART NUMBER	HEIGHT
FOXCONN	AS0B821-S55B-7H	5.5mm
FOXCONN	AS0B821-S78B-7H	7.8mm

Table 32 Valid SMARC-314 Connectors Part Numbers

You must consider the SMARC-314 connector height depending on your base board needs.

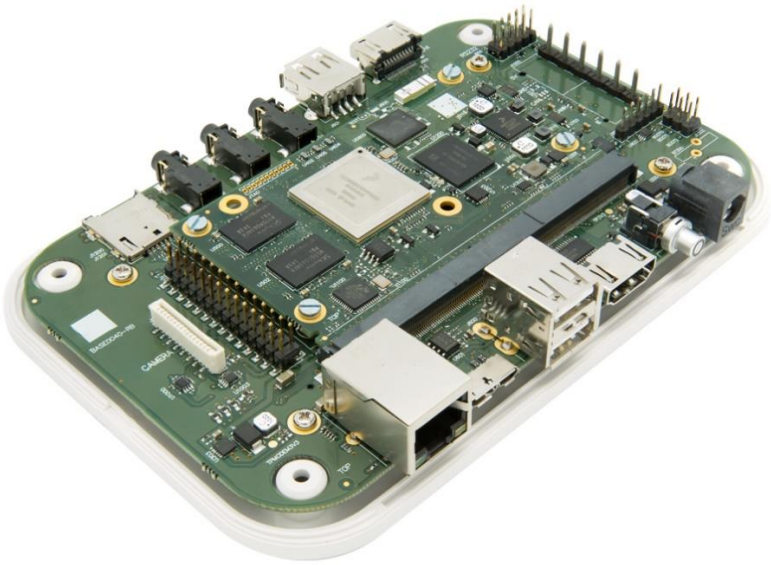


Figure 36 SMARC EXPANSION

6.1 PINOUT TABLE OF SMARC-314 EXPANSION INTERFACE

The following table provides pinout details for the SMARC-314 expansion interface. The meaning of each column and the colors used in rows are explained in Table 33 below.

COLUMN	INFORMATION PROVIDED	
PIN	Indicates the pin number of the SMARC-314 interface.	
VOLTAGE LEVEL	Signal level voltage.	
	5V	5V signal
	3V3	3.3 V signal
	1V8	1.8 V signal
	VBAT	Battery power
	DIF	Differential pair signal
	ANALOG	Analog signal
	GND	Digital ground
	AGND	Analog ground
	NC	No connected. This pin should be floating
DEV PIN	Internal main device pin number related to the iMX6 processor.	
MAIN FUNCTION	Main or suggested function.	
MAIN MUX	Mode number for the main function.	
TYPE	Indicates pin type.	
	POWER	Power signal
	IN	CMOS input pin
	OUT	CMOS output pin
	IO	CMOS input and output pin
	ETH	Ethernet physical pin
	USB	USB line
	NC	No connected. This pin should be floating
	VK	Power supply from battery
FIXED FUNCTION	Indicates if the pin function is configurable or not.	
	YES	Pin functionality or mux configuration can't be changed
	NO	Pin can be configured as another peripheral (mux configurable). See MUX chapter for more information.
COMMENTS	Clarifications for the related SMARC-314 pin. See Device chapter for more information.	

ROW COLOR	INFORMATION PROVIDED	
GREY	NC	No connected
LIGHT BLUE	VIN	Input power
VIOLET	SPI	SPI signals
CINNAMON	RTC	RTC battery positive signal
LIGHT GREEN	DGND	Digital ground
DARK GREEN	I2C	I2C signals
YELLOW	ETH	Ethernet group
LIGHT BROWN	USB0	USB OTG signals
DARK BROWN	USB1	USB HOST signals
RED	BOOT	Boot signals
WHITE	GPIO	GPIO signals
LIGHT YELLOW	UART	UART signals
CYAN	CAN	CAN signals
BLUE	MMC	MMC signals
DARK GREY	HDMI	HDMI signals
ORANGE	LVDS	LVDS signals
DARK BLUE	CSI	MIPI CSI 2 signals
PINK	PCIe	PCIe signals
BAYOU	SATA	SATA signals
GREEN	DSI	MIPI DSI 2 signals
BLACK	I2S	I2S signals

Table 33 SMARC-314 Expansion Interface Information

SMARC-314			INTERNAL DEVICE					COMMENTS
Pin	Pin name	Voltage level	Dev Pin	Main function	Main MUX	Type	Fixed function	
P1	PCAM_PXL_ CK1	NC	NC	No connected	NA	NC	NC	No connected
P2	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
P3	CSI1_CK+ / PCAM_D0	DIF	F3	CSI_CLK0_P	0	MIPI CSI-2	YES	CSI1 differential clock input +
P4	CSI1_CK- / PCAM_D1	DIF	F4	CSI_CLK0_N	0	MIPI CSI-2	YES	CSI1 differential clock input -
P5	PCAM_DE	NC	NC	No connected	NA	NC	NC	No connected
P6	PCAM_MCK	NC	NC	No connected	NA	NC	NC	No connected
P7	CSI1_D0+ / PCAM_D2	DIF	E3	CSI_DATA0_P	0	MIPI CSI-2	YES	CSI1 differential data input D0 +
P8	CSI1_D0- / PCAM_D3	DIF	E4	CSI_DATA0_N	0	MIPI CSI-2	YES	CSI1 differential data input D0 -
P9	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
P10	CSI1_D1+ / PCAM_D4	DIF	D2	CSI_DATA1_P	0	MIPI CSI-2	YES	CSI1 differential data inputs D1 +
P11	CSI1_D1- / PCAM_D5	DIF	D1	CSI_DATA1_N	0	MIPI CSI-2	YES	CSI1 differential data inputs D1 -
P12	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
P13	CSI1_D2+ / PCAM_D6	DIF	E2	CSI_DATA2_P	0	MIPI CSI-2	YES	CSI1 differential data input D2 +
P14	CSI1_D2- / PCAM_D7	DIF	E1	CSI_DATA2_M	0	MIPI CSI-2	YES	CSI1 differential data input D2 -
P15	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
P16	CSI1_D3+ / PCAM_D8	DIF	F1	CSI_DATA3_P	0	MIPI CSI-2	YES	CSI1 differential data input D3 +
P17	CSI1_D3- / PCAM_D9	DIF	F2	CSI_DATA3_N	0	MIPI CSI-2	YES	CSI1 differential data input D3 -
P18	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
P19	GBE_MDI3-	DIF	NC	MDIN[3]	NA	ETH	YES	Analog Transmit/Receive Data 3 Negative. Differential output to magnetics.
P20	GBE_MDI3+	DIF	NC	MDIP[3]	NA	ETH	YES	Analog Transmit/Receive Data 3 Positive. Differential output to magnetics.
P21	GBE_LINK1 00#	1V8	NC	LED[1]	NA	OUT	YES	Active Low. Means 1000/100 Mbps speed. Inactive if 10 Mbps.
P22	GBE_LINK1 000#	NC	NC	No connected	NA	NC	NC	No connected
P23	GBE_MDI2-	DIF	NC	MDIN[2]	NA	ETH	YES	Analog Transmit/Receive Data 2 Negative. Differential output to magnetics.
P24	GBE_MDI2+	DIF	NC	MDIP[2]	NA	ETH	YES	Analog Transmit/Receive Data 2 Positive. Differential output to magnetics.
P25	GBE_LINK_ ACT#	1V8	NC	LED[0]	NA	OUT	YES	Active Low. Indicates valid link and blinks when there is activity.
P26	GBE_MDI1-	DIF	NC	MDIN[1]	NA	ETH	YES	Analog Transmit/Receive Data 1 Negative. Differential output to magnetics.
P27	GBE_MDI1+	DIF	NC	MDIP[1]	NA	ETH	YES	Analog Transmit/Receive Data 1 Positive. Differential output to magnetics.
P28	GBE_CTREF	NC	NC	No connected	NA	NC	NC	No connected
P29	GBE_MDI0-	DIF	NC	MDIN[0]	NA	ETH	YES	Analog Transmit/Receive Data 0 Negative. Differential output to magnetics.
P30	GBE_MDI0+	DIF	NC	MDIP[0]	NA	ETH	YES	Analog Transmit/Receive Data 0 Positive. Differential output to magnetics.
P31	SPI0_CS1#	1V8	R25	ECSPI3_SS2	2	OUT	NO	SPI3 chip select 2 signal
P32	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
P33	SDIO_WP	3V3	T2	SD1_WP	6	IN	YES	MMC1 Write Protect. This signal has a 3K3 PU resistor.
P34	SDIO_CMD	3V3	B21	SD1_CMD	0	IO	NO	MMC1 Command
P35	SDIO_CD#	3V3	T4	SD1_CD_B	6	IN	YES	MMC1 Card Detect. This signal has a 3K3 PU resistor.
P36	SDIO_CK	3V3	D20	SD1_CLK	0	IO	NO	MMC1 Clock
P37	SDIO_PWR_ EN	3V3	F22	GPIO3_IO24	5	OUT	NO	MMC1 Card Power Enable
P38	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
P39	SDIO_D0	3V3	A21	SD1_DATA0	0	IO	NO	MMC1 Data Bus 0
P40	SDIO_D1	3V3	C20	SD1_DATA1	0	IO	NO	MMC1 Data Bus 1
P41	SDIO_D2	3V3	E19	SD1_DATA2	0	IO	NO	MMC1 Data Bus 2
P42	SDIO_D3	3V3	F18	SD1_DATA3	0	IO	NO	MMC1 Data Bus 3
P43	SPI0_CS0#	1V8	P20	ECSPI3_SS1	2	OUT	NO	SPI3 chip select 1 signal

SMARC-314			INTERNAL DEVICE					COMMENTS
P44	SPI0_CK	1V8	P24	ECSPI3_SCLK	2	OUT	YES	SPI3 clock
P45	SPI0_DIN	1V8	P23	ECSPI3_MISO	2	IN	YES	SPI3 Master Input-Slave Output (MISO)
P46	SPI0_DO	1V8	P22	ECSPI3_MOSI	2	OUT	YES	SPI3 Master Output-Slave Input (MOSI)
P47	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
P48	SATA_TX+	DIF	A12	SATA_PHY_TX_P	0	SATA 3 Gb/s	YES	Differential SATA transmit data +. This signal has a 10 nF coupling capacitor.
P49	SATA_TX-	DIF	B12	SATA_PHY_TX_N	0	SATA 3 Gb/s	YES	Differential SATA transmit data -. This signal has a 10 nF coupling capacitor.
P50	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
P51	SATA_RX+	DIF	B14	SATA_PHY_RX_P	0	SATA 3 Gb/s	YES	Differential SATA receive data +. This signal has a 10 nF coupling capacitor.
P52	SATA_RX-	DIF	A14	SATA_PHY_RX_N	0	SATA 3 Gb/s	YES	Differential SATA receive data -. This signal has a 10 nF coupling capacitor.
P53	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
P54	SPI1_CS0#	1V8	V25	ECSPI2_SS0	2	OUT	NO	SPI2 chip select 0 signal
P55	SPI1_CS1#	1V8	T22	ECSPI2_SS1	3	OUT	NO	SPI2 chip select 1 signal
P56	SPI1_CK	1V8	H24	ECSPI2_SCLK	2	OUT	NO	SPI2 clock
P57	SPI1_DIN	1V8	J24	ECSPI2_MISO	2	IN	NO	SPI2 Master Input-Slave Output (MISO)
P58	SPI1_DO	1V8	J23	ECSPI2_MOSI	2	OUT	NO	SPI2 Master Output-Slave Input (MOSI)
P59	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
P60	USB0+	DIF	A6	USB_OTG_DP	0	USB 2.0	YES	Analog D+ data pin of the USB0
P61	USB0-	DIF	B6	USB_OTG_DN	0	USB 2.0	YES	Analog D- data pin of the USB0
P62	USB0_EN_O C#	3V3	R4	GPIO1_IO05	5	IO	YES	Active Low. Over current Indication to module. This signal has a 3K3 PU resistor.
P63	USB0_VBUS _DET	5V	E9	USB_OTG_VBUS	0	USB	YES	USB host power detection, when this port is used as a device
P64	USB0_OTG_ ID	1V8	W23	USB_OTG_ID	0	IN	YES	USB OTG ID input, active high
P65	USB1+	DIF	E10	USB_H1_DP	0	USB 2.0	YES	Analog D+ data pin of the USB1
P66	USB1-	DIF	F10	USB_H1_DN	0	USB 2.0	YES	Analog D- data pin of the USB1
P67	USB1_EN_O C#	3V3	R6	GPIO1_IO04	5	IO	YES	Active Low. Over current Indication to module. This signal has a 3K3 PU resistor.
P68	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
P69	USB2+	NC	NC	No connected	NA	NC	NC	No connected
P70	USB2-	NC	NC	No connected	NA	NC	NC	No connected
P71	USB2_EN_O C#	NC	NC	No connected	NA	NC	NC	No connected

P72	PCIE_C_PRS NT#	NC	NC	No connected	NA	NC	NC	No connected
P73	PCIE_B_PRS NT#	NC	NC	No connected	NA	NC	NC	No connected
P74	PCIE_A_PRS NT#	3V3	U24	GPIO5_IO05	5	IN	YES	PCIe Port A present input. This signal has a 4K7 PU resistor.
P75	PCIE_A_RST #	3V3	F15	GPIO6_IO11	5	OUT	NO	PCIe Port A reset output
P76	PCIE_C_CKR EQ#	NC	NC	No connected	NA	NC	NC	No connected
P77	PCIE_B_CKR EQ#	NC	NC	No connected	NA	NC	NC	No connected
P78	PCIE_A_CK REQ#	3V3	T21	GPIO5_IO10	5	IN	YES	PCIe Port A clock request input. This signal has a 4K7 PU resistor.
P79	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
P80	PCIE_C_REF CK+	NC	NC	No connected	NA	NC	NC	No connected
P81	PCIE_C_REF CK-	NC	NC	No connected	NA	NC	NC	No connected
P82	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
P83	PCIE_A_REF CK+	DIF	D7	XTALOSC_CLK1_P	0	LVDS TIA/EIA-644	YES	Differential PCIe Link A reference clock output DC coupled +
P84	PCIE_A_REF CK-	DIF	C7	XTALOSC_CLK1_N	0	LVDS TIA/EIA-644	YES	Differential PCIe Link A reference clock output DC coupled -
P85	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
P86	PCIE_A_RX+	DIF	B2	PCIE_RX_P	0	LVDS TIA/EIA-644	YES	Differential PCIe Link A receive data pair 0 +
P87	PCIE_A_RX-	DIF	B1	PCIE_RX_N	0	LVDS TIA/EIA-644	YES	Differential PCIe Link A receive data pair 0 -
P88	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
P89	PCIE_A_TX+	DIF	B3	PCIE_TX_P	0	LVDS TIA/EIA-644	YES	Differential PCIe Link A transmit data pair 0 +. This signal has a 0.1 uF coupling capacitor.
P90	PCIE_A_TX-	DIF	A3	PCIE_TX_N	0	LVDS TIA/EIA-644	YES	Differential PCIe Link A transmit data pair 0 -. This signal has a 0.1 uF coupling capacitor.
P91	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
P92	HDMI_D2+	DIF	K4	HDMI_TX_DATA2_P	0	HDMI 1.4a	YES	HDMI data differential pair D2 +
P93	HDMI_D2-	DIF	K3	HDMI_TX_DATA2_N	0	HDMI 1.4a	YES	HDMI data differential pair D2 -
P94	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
P95	HDMI_D1+	DIF	J4	HDMI_TX_DATA1_P	0	HDMI 1.4a	YES	HDMI data differential pair D1 +
P96	HDMI_D1-	DIF	J3	HDMI_TX_DATA1_N	0	HDMI 1.4a	YES	HDMI data differential pair D1 -
P97	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
P98	HDMI_D0+	DIF	K6	HDMI_TX_DATA0_P	0	HDMI 1.4a	YES	HDMI data differential pair D0 +
P99	HDMI_D0-	DIF	K5	HDMI_TX_DATA0_N	0	HDMI 1.4a	YES	HDMI data differential pair D0 -
P100	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
P101	HDMI_CK+	DIF	J6	HDMI_TX_CLK_P	0	HDMI 1.4a	YES	HDMI differential clock output pair +
P102	HDMI_CK-	DIF	J5	HDMI_TX_CLK_N	0	HDMI 1.4a	YES	HDMI differential clock output pair -
P103	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
P104	HDMI_HPD	1V8	K1	HDMI_TX_HPD	0	HDMI 1.4a	YES	HDMI Hot Plug Detect input. This signal has a 47K PU resistor.

P105	HDMI_CTRL _CK	1V8	U5	I2C2_SCL	4	HDMI u.4a	YES	I2C2 bus clock. This signal has a 1K5 PU resistor.
P106	HDMI_CTRL _DAT	1V8	T7	I2C2_SDA	4	HDMI u.4a	YES	I2C2 bus data. 0x08 is used. This signal has a 1K5 PU resistor.
P107	HDMI_CEC	1V8	H19	HDMI_TX_CEC_LINE	6	HDMI u.4a	YES	HDMI Consumer Electronics Control . This signal has a 47K PU resistor.
P108	GPIO0 / CAM0_PWR #	1V8	N1	GPIO5_IO22	5	IO	NO	General purpose input/output
P109	GPIO1 / CAM1_PWR #	1V8	P2	GPIO5_IO23	5	IO	NO	General purpose input/output
P110	GPIO2 / CAM0_RST #	1V8	N4	GPIO5_IO24	5	IO	NO	General purpose input/output
P111	GPIO3 / CAM1_RST #	1V8	N3	GPIO5_IO25	5	IO	NO	General purpose input/output
P112	GPIO4 / HDA_RST#	1V8	W6	GPIO4_IO10	5	IO	NO	General purpose input/output
P113	GPIO5 / PWM_OUT	1V8	R22	PWM1_OUT	2	IO	NO	PMW Output 1 or General purpose input/output
P114	GPIO6 / TACHIN	1V8	R23	GPIO4_IO27	5	IO	NO	General purpose input/output
P115	GPIO7 / PCAM_FLD	1V8	R24	GPIO4_IO28	5	IO	NO	General purpose input/output
P116	GPIO8 / CAN0_ERR#	1V8	N6	GPIO5_IO26	5	IO	NO	General purpose input/output
P117	GPIO9 / CAN1_ERR#	1V8	N5	GPIO5_IO27	5	IO	NO	General purpose input/output
P118	GPIO10	1V8	R21	GPIO4_IO31	5	IO	NO	General purpose input/output
P119	GPIO11	1V8	T23	GPIO5_IO005	5	IO	NO	General purpose input/output
P120	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
P121	I2C_PM_CK	1V8	U5	I2C2_SCL	4	IO	YES	I2C2 bus clock. This signal has a 1K5 PU resistor.
P122	I2C_PM_DA T	1V8	T7	I2C2_SDA	4	IO	YES	I2C2 bus data. 0x08 is used. This signal has a 1K5 PU resistor.
P123	BOOT_SEL0 #	1V8	NC	BOOT 0	NA	IN	YES	Boot select 0. See table Table 7. This signal has a 47K PU resistor.
P124	BOOT_SEL1#	1V8	NC	BOOT 1	NA	IN	YES	Boot select 1. See table Table 7. This signal has a 47K PU resistor.
P125	BOOT_SEL2 #	1V8	NC	BOOT 2	NA	IN	YES	Boot select 2. See table Table 7. This signal has a 47K PU resistor.
P126	RESET_OUT #	1V8	L6	GPIO6_IO005	5	OUT	NO	General purpose reset output to Carrier board.
P127	RESET_IN#	1V8	NC	PWRON	NA	IN	YES	Reset input from Carrier board. This signal has a 3K3 PU resistor.
P128	POWER_BT N#	1V8	M4	GPIO6_IO00	5	IN	YES	Power-button input from Carrier board.This signal has a 3K3 PU resistor.
P129	SER0_TX	NC	NC	No connected	NA	NC	NC	No connected
P130	SER0_RX	NC	NC	No connected	NA	NC	NC	No connected
P131	SER0_RTS#	NC	NC	No connected	NA	NC	NC	No connected
P132	SER0_CTS#	NC	NC	No connected	NA	NC	NC	No connected
P133	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
P134	SER1_TX	1V8	E24	UART2_TX_DATA	4	OUT	NO	Debug UART2 Transmit Data Output
P135	SER1_RX	1V8	E25	UART2_RX_DATA	4	IN	NO	Debug UART2 Receive Data Input
P136	SER2_TX	1V8	B17	UART3_TX_DATA	2	OUT	NO	UART3 Transmit Data Output
P137	SER2_RX	1V8	E16	UART3_RX_DATA	2	IN	NO	UART3 Receive Data Input

P138	SER2_RTS#	1V8	H21	UART3_RTS_B	4	OUT	NO	UART3 CTSn Output
P139	SER2_CTS#	1V8	J20	UART3_CTS_B	4	IN	NO	UART3 RTSn Input
P140	SER3_TX	1V8	M2	UART4_TX_DATA	3	OUT	NO	UART4 Transmit Data Output
P141	SER3_RX	1V8	L1	UART4_RX_DATA	3	IN	NO	UART4 Receive Data Input
P142	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
P143	CAN0_TX	1V8	R3	FLEXCAN1_TX	3	OUT	NO	CAN1 Transmission line
P144	CAN0_RX	1V8	W4	FLEXCAN1_RX	2	IN	NO	CAN1 Reception line
P145	CAN1_TX	1V8	T6	FLEXCAN2_TX	0	OUT	NO	CAN2 Transmission line
P146	CAN1_RX	1V8	V5	FLEXCAN2_RX	0	IN	NO	CAN2 Reception line
P147	VDD_IN	5V	NC	VIN	NA	POWER	YES	Pins used to power up the module . Source voltage should be between 4.75V-5.25V (UP TO 6W)
P148	VDD_IN	5V	NC	VIN	NA	POWER	YES	
P149	VDD_IN	5V	NC	VIN	NA	POWER	YES	
P150	VDD_IN	5V	NC	VIN	NA	POWER	YES	
P151	VDD_IN	5V	NC	VIN	NA	POWER	YES	
P152	VDD_IN	5V	NC	VIN	NA	POWER	YES	
P153	VDD_IN	5V	NC	VIN	NA	POWER	YES	
P154	VDD_IN	5V	NC	VIN	NA	POWER	YES	
P155	VDD_IN	5V	NC	VIN	NA	POWER	YES	
P156	VDD_IN	5V	NC	VIN	NA	POWER	YES	
S1	PCAM_VSY NC	NC	NC	No connected	NA	NC	NC	No connected
S2	PCAM_HSY NC	NC	NC	No connected	NA	NC	NC	No connected
S3	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
S4	PCAM_PXL_ CK0	NC	NC	No connected	NA	NC	NC	No connected
S5	I2C_CAM_C K	1V8	H20	I2C1_SCL	6	IO	YES	I2C1 bus clock. This signal has a 1K5 PU resistor.
S6	CAM_MCK	1V8	R7	CCM_CLKO2	4	OUT	NO	Master clock output for CSI camera support
S7	I2C_CAM_D AT	1V8	G23	I2C1_SDA	1	IO	YES	I2C1 bus data. This signal has a 1K5 PU resistor.
S8	CSI0_CK+ / PCAM_D10	NC	NC	No connected	NA	NC	NC	No connected
S9	CSI0_CK- / PCAM_D11	NC	NC	No connected	NA	NC	NC	No connected
S10	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
S11	CSI0_D0+ / PCAM_D12	NC	NC	No connected	NA	NC	NC	No connected
S12	CSI0_D0- / PCAM_D13	NC	NC	No connected	NA	NC	NC	No connected
S13	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
S14	CSI0_D1+ / PCAM_D14	NC	NC	No connected	NA	NC	NC	No connected
S15	CSI0_D1- / PCAM_D15	NC	NC	No connected	NA	NC	NC	No connected
S16	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
S17	AFB0_OUT	NC	NC	No connected	NA	NC	NC	No connected
S18	AFB1_OUT	1V8	B19	PWM3_OUT	2	OUT	NO	PWM output 3
S19	AFB2_OUT	NC	NC	No connected	NA	NC	NC	No connected
S20	AFB3_IN	NC	NC	No connected	NA	NC	NC	No connected
S21	AFB4_IN	NC	NC	No connected	NA	NC	NC	No connected

S22	AFB5_IN	NC	NC	No connected	NA	NC	NC	No connected
S23	AFB6_PTIO	NC	NC	No connected	NA	NC	NC	No connected
S24	AFB7_PTIO	NC	NC	No connected	NA	NC	NC	No connected
S25	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
S26	SDMMC_D0	NC	NC	No connected	NA	NC	NC	No connected
S27	SDMMC_D1	NC	NC	No connected	NA	NC	NC	No connected
S28	SDMMC_D2	NC	NC	No connected	NA	NC	NC	No connected
S29	SDMMC_D3	NC	NC	No connected	NA	NC	NC	No connected
S30	SDMMC_D4	NC	NC	No connected	NA	NC	NC	No connected
S31	SDMMC_D5	NC	NC	No connected	NA	NC	NC	No connected
S32	SDMMC_D6	NC	NC	No connected	NA	NC	NC	No connected
S33	SDMMC_D7	NC	NC	No connected	NA	NC	NC	No connected
S34	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
S35	SDMMC_CK	NC	NC	No connected	NA	NC	YES	No connected
S36	SDMMC_C MD	NC	NC	No connected	NA	NC	YES	No connected
S37	SDMMC_RS T#	NC	NC	No connected	NA	NC	YES	No connected
S38	AUDIO_MC K	1V8	P4	CCM_CLKO1	3	OUT	NO	Master clock output to Audio codecs
S39	I2S0_LRCK	1V8	V24	AUD4_TXFS	3	IO	NO	AUD4 Transmit Frame Sync signal
S40	I2S0_SDOU T	1V8	T20	AUD4_TXD	3	OUT	NO	AUD4 Data Transmit signal
S41	I2S0_SDIN	1V8	W24	AUD4_RXD	3	IN	NO	AUD4 Data Receive signal
S42	I2S0_CK	1V8	U22	AUD4_TXC	3	IO	NO	AUD4 Transmit Clock signal
S43	I2S1_LRCK	NC	NC	No connected	NA	NC	NC	No connected
S44	I2S1_SDOU T	NC	NC	No connected	NA	NC	NC	No connected
S45	I2S1_SDIN	NC	NC	No connected	NA	NC	NC	No connected
S46	I2S1_CK	NC	NC	No connected	NA	NC	NC	No connected
S47	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
S48	I2C_GP_CK	1V8	F21	I2C3_SCL	6	IO	YES	I2C3 bus clock. This signal has a 1K5 PU resistor.
S49	I2C_GP_DA T	1V8	D24	I2C3_SDA	6	IO	YES	I2C3 bus data. 0x50 is used. This signal has a 1K5 PU resistor.
S50	I2S2_LRCK	NC	NC	No connected	NA	NC	NC	No connected
S51	I2S2_SDOU T	NC	NC	No connected	NA	NC	NC	No connected
S52	I2S2_SDIN	NC	NC	No connected	NA	NC	NC	No connected
S53	I2S2_CK	NC	NC	No connected	NA	NC	NC	No connected
S54	SATA_ACT#	3V3	T24	GPIO5_IO06	5	OUT	NO	Active low SATA activity indicator
S55	AFB8_PTIO	NC	NC	No connected	NA	NC	NC	No connected
S56	AFB9_PTIO	NC	NC	No connected	NA	NC	NC	No connected
S57	PCAM_ON_ CSI0#	NC	NC	No connected	NA	NC	NC	No connected
S58	PCAM_ON_ CSI1#	NC	NC	No connected	NA	NC	NC	No connected
S59	SPDIF_OUT	NC	NC	No connected	NA	NC	NC	No connected
S60	SPDIF_IN	NC	NC	No connected	NA	NC	NC	No connected
S61	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
S62	AFB_DIFF0+	NC	NC	No connected	NA	NC	NC	No connected
S63	AFB_DIFF0-	NC	NC	No connected	NA	NC	NC	No connected
S64	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
S65	AFB_DIFF1+	NC	NC	No connected	NA	NC	NC	No connected

S66	AFB_DIFF1-	NC	NC	No connected	NA	NC	NC	No connected
S67	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
S68	AFB_DIFF2+	DIF	H4	DSI_CLK0_P	0	MIPI DSI 1.01	YES	DSI differential clock +
S69	AFB_DIFF2-	DIF	H3	DSI_CLK0_N	0	MIPI DSI 1.01	YES	DSI differential clock -
S70	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
S71	AFB_DIFF3+	DIF	G1	DSI_DATA0_P	0	MIPI DSI 1.01	YES	DSI differential data D0 +
S72	AFB_DIFF3-	DIF	G2	DSI_DATA0_N	0	MIPI DSI 1.01	YES	DSI differential data D0 -
S73	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
S74	AFB_DIFF4+	DIF	H1	DSI_DATA1_P	0	MIPI DSI 1.01	YES	DSI differential data D1 +
S75	AFB_DIFF4-	DIF	H2	DSI_DATA1_N	0	MIPI DSI 1.01	YES	DSI differential data D1 -
S76	PCIE_B_RST #	NC	NC	No connected	NA	NC	NC	No connected
S77	PCIE_C_RST #	NC	NC	No connected	NA	NC	NC	No connected
S78	PCIE_C_RX+	NC	NC	No connected	NA	NC	NC	No connected
S79	PCIE_C_RX-	NC	NC	No connected	NA	NC	NC	No connected
S80	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
S81	PCIE_C_TX+	NC	NC	No connected	NA	NC	NC	No connected
S82	PCIE_C_TX-	NC	NC	No connected	NA	NC	NC	No connected
S83	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
S84	PCIE_B_REF CK+	NC	NC	No connected	NA	NC	NC	No connected
S85	PCIE_B_REF CK-	NC	NC	No connected	NA	NC	NC	No connected
S86	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
S87	PCIE_B_RX+	NC	NC	No connected	NA	NC	NC	No connected
S88	PCIE_B_RX-	NC	NC	No connected	NA	NC	NC	No connected
S89	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
S90	PCIE_B_TX+	NC	NC	No connected	NA	NC	NC	No connected
S91	PCIE_B_TX-	NC	NC	No connected	NA	NC	NC	No connected
S92	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
S93	LCD_D0	NC	NC	No connected	NA	NC	NC	No connected
S94	LCD_D1	NC	NC	No connected	NA	NC	NC	No connected
S95	LCD_D2	NC	NC	No connected	NA	NC	NC	No connected
S96	LCD_D3	NC	NC	No connected	NA	NC	NC	No connected
S97	LCD_D4	NC	NC	No connected	NA	NC	NC	No connected
S98	LCD_D5	NC	NC	No connected	NA	NC	NC	No connected
S99	LCD_D6	NC	NC	No connected	NA	NC	NC	No connected
S100	LCD_D7	NC	NC	No connected	NA	NC	NC	No connected
S101	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
S102	LCD_D8	NC	NC	No connected	NA	NC	NC	No connected
S103	LCD_D9	NC	NC	No connected	NA	NC	NC	No connected
S104	LCD_D10	NC	NC	No connected	NA	NC	NC	No connected
S105	LCD_D11	NC	NC	No connected	NA	NC	NC	No connected
S106	LCD_D12	NC	NC	No connected	NA	NC	NC	No connected
S107	LCD_D13	NC	NC	No connected	NA	NC	NC	No connected
S108	LCD_D14	NC	NC	No connected	NA	NC	NC	No connected
S109	LCD_D15	NC	NC	No connected	NA	NC	NC	No connected

S110	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
S111	LCD_D16	NC	NC	No connected	NA	NC	NC	No connected
S112	LCD_D17	NC	NC	No connected	NA	NC	NC	No connected
S113	LCD_D18	NC	NC	No connected	NA	NC	NC	No connected
S114	LCD_D19	NC	NC	No connected	NA	NC	NC	No connected
S115	LCD_D20	NC	NC	No connected	NA	NC	NC	No connected
S116	LCD_D21	NC	NC	No connected	NA	NC	NC	No connected
S117	LCD_D22	NC	NC	No connected	NA	NC	NC	No connected
S118	LCD_D23	NC	NC	No connected	NA	NC	NC	No connected
S119	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
S120	LCD_DE	NC	NC	No connected	NA	NC	NC	No connected
S121	LCD_VS	NC	NC	No connected	NA	NC	NC	No connected
S122	LCD_HS	NC	NC	No connected	NA	NC	NC	No connected
S123	LCD_PCK	NC	NC	No connected	NA	NC	NC	No connected
S124	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
S125	LVDS0+	DIF	U1	LVDS0_DATA0_P	0	LVDS TIA/EIA-644	YES	LVDS data channel differential pair D0 +
S126	LVDS0-	DIF	U2	LVDS0_DATA0_N	0	LVDS TIA/EIA-644	YES	LVDS data channel differential pair D0 -
S127	LCD_BKLT_ EN	1V8	M6	GPIO6_IO04	5	IO	NO	High enables panel backlight
S128	LVDS1+	DIF	U3	LVDS0_DATA1_P	0	LVDS TIA/EIA-644	YES	LVDS data channel differential pair D1+
S129	LVDS1-	DIF	U4	LVDS0_DATA1_N	0	LVDS TIA/EIA-644	YES	LVDS data channel differential pair D1 -
S130	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
S131	LVDS2+	DIF	V1	LVDS0_DATA2_P	0	LVDS TIA/EIA-644	YES	LVDS data channel differential pair D2 +
S132	LVDS2-	DIF	V2	LVDS0_DATA2_N	0	LVDS TIA/EIA-644	YES	LVDS data channel differential pair D2 -
S133	LCD_VDD_E N	1V8	N2	GPIO5_IO21	5	IO	NO	High enables panel VDD
S134	LVDS_CK+	DIF	V3	LVDS0_CLK_P	0	LVDS TIA/EIA-644	YES	LVDS clock channel differential pair +
S135	LVDS_CK-	DIF	V4	LVDS0_CLK_N	0	LVDS TIA/EIA-644	YES	LVDS clock channel differential pair -
S136	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
S137	LVDS3+	DIF	W1	LVDS0_DATA3_P	0	LVDS TIA/EIA-644	YES	LVDS data channel differential pair D3 +
S138	LVDS3-	DIF	W2	LVDS0_DATA3_N	0	LVDS TIA/EIA-644	YES	LVDS data channel differential pair D3 -
S139	I2C_LCD_CK	1V8	E15	I2C4_SCL	9	IO	YES	I2C4 bus clock. This signal has a 1K5 PU resistor. Solo/DualLite version.
			H20	I2C1_SCL	6	IO	YES	I2C1 bus clock. This signal has a 1K5 PU resistor. Dual/Quad version.
S140	I2C_LCD_DAT	1V8	D16	I2C4_SDA	9	IO	YES	I2C4 bus data. This signal has a 1K5 PU resistor. Solo/DualLite version.
			G23	I2C1_SDA	1	IO	YES	I2C1 bus data. This signal has a 1K5 PU resistor. Dual/Quad version.
S141	LCD_BKLT_ PWM	1V8	F17	PWM4_OUT	2	OUT	NO	Display Backlight. PMW output 4.

S142	RSVD	NC	NC	No connected	NA	NC	NC	No connected
S143	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground
S144	RSVD / EDP_HPD	NC	NC	No connected	NA	NC	NC	No connected
S145	WDT_TIME_ OUT#	1V8	T25	WDOG2_B	3	OUT	YES	Watch-Dog-Timer Output
S146	PCIE_WAKE #	3V3	P3	GPIO5_IO20	5	IN	YES	PCIe wake up interrupt to host. This signal has a 4K7 PU resistor.
S147	VDD_RTC	VBAT	NC	LICELL	NA	IO	YES	Low current RTC circuit backup power. Voltages from 2.5V to 3.3V.
S148	LID#	1V8	L3	GPIO6_IO03	5	IN	YES	Lid open/close indication to Module. This signal has a 3K3 PU resistor.
S149	SLEEP#	1V8	L4	GPIO6_IO02	5	IN	YES	Sleep indicator from Carrier board .This signal has a 3K3 PU resistor.
S150	VIN_PWR_B AD#	5V	NC	PWR_BAD_INDIC ATION	NA	IN	YES	Power bad indication from Carrier board
S151	CHARGING #	1V8	M5	GPIO6_IO01	5	IN	YES	Held low by Carrier during battery charging. This signal has a 3K3 PU resistor.
S152	CHARGER_ PRSNT#	1V8	N19	GPIO4_IO16	5	IN	YES	Held low by Carrier if DC input for battery charger is present. This signal has a 3K3 PU resistor.
S153	CARRIER_S TBY#	1V8	R20	GPIO5_IO07	5	OUT	NO	The Module shall drive this signal low when the system is in a standby power state. This signal has a 10K PD resistor.
S154	CARRIER_P WR_ON	1V8	G22	GPIO3_IO25	5	OUT	NO	Carrier board circuits (apart from power management and power path circuits) should not be Powered up until the Module asserts the CARRIER_PWR_ON signal.
S155	FORCE_REC OV#	1V8	NC	FORCE_RECOV	NA	IN	YES	Low on this pin disable boot select circuit. This signal has a 47K PU resistor.
S156	BATLOW#	1V8	U23	GPIO5_IO13	5	IN	YES	Battery low indication to Module. This signal has a 3K3 PU resistor.
S157	TEST#	1V8	C25	GPIO3_IO16	5	IN	YES	Held low by Carrier to invoke Module vendor specific test function(s). This signal has a 3K3 PU resistor.
S158	GND	GND	NC	DGND	NA	POWER	YES	Digital Ground

Table 34 J900 SMARC-314 Pinout Description

7 ELECTRICAL CHARACTERISTICS

Electrical parameter	Min	Typ	Max	Unit
5V INPUT POWER SUPPLY				
DC INPUT POWER SUPPLY	4.75	5	5.25	V
DC INPUT SUPPLY Current (1)	100	360	1200	mA
IO pins (2)				
Input/output High-Level DC voltage	1.26	1.8	2.1	V
Input/output Low-Level DC voltage	-0.5	0	0.54	V
Output drive current	-0.1	0.5	1	mA
RTC_BATTERY type pins				
Input DC voltage	2.5	3	3.3	V

Table 35 MitySOM-iMX6 Electrical Characteristics

(1)Current measured with default delivered software. Be aware that different software configurations could drastically modify current consumption.

(2)The electrical specification depends on the configured mode. For accurate information of each pin, review iMX6 Applications Processor official document from NXP official site https://www.nxp.com/.

MODULES CAN BE DAMAGED IF ANY OF THESE ELECTRICAL LIMITS ARE EXCEEDED AND/OR ELECTROSTATIC DISCHARGE PRECAUTIONS ARE NOT FOLLOWED. **WARRANTY LOST** IF IMPROPER USE OF THE MODULE IS FOUND.

8 CHANGE HISTORY

Revision	Date	Description
1A	2017-Mar-08	Initial release
1B	2018-Mar-28	Updates to available models list, image quality improved for figures

Table 36 Change History