1 INTRODUCTION

The information presented in this data sheet is for the MitySOM-MX6 family Development Board from Critical Link. In addition to supplying these off the shelf solutions, Critical Link's embedded design team provides systems engineering, software development, and hardware design services to support your project anywhere in the development lifecycle. Email info@criticallink.com with any questions.

2 OVERVIEW

2.1 MitySOM-iMX6 SMARC EXPANSION DESCRIPTION

The MitySOM-iMX6 Development Board (also referred to as the SMARC Expansion) is a fully tested, highly reliable, scalable, and high performing base board that allows customers access to the functionalities of the MitySOM-iMX6 and to focus on their end application. It is designed for industrial and commercial purposes, and can also be used to develop and test your application before building a prototype, which saves cost and time-to-market.

Highlights:

- Open source hardware and software to help develop your custom embedded solutions.
- 1x Ethernet.
- 1x USB 3.0 OTG.
- 3x USB 2.0 HOST.
- 1x HDMI output.
- 1x Button LED.
- 1x RTC battery.
- 1x Expansion 28 pins header.
- 1x Terminal 6 pins plug.
- 1x Serial header expansion.
- 1x Serial debug 3V3 interface header.
- 1x Boot select header.
- 1x CSI connector.
- 1x Micro SD connector.
- 1x Line-in audio mini jack.
- 1x Headphones audio mini jack.
- 1x Mic-in audio mini jack.
- 1x DVI-D.
- 1x mSATA connector.
- 1x USB modem miniPCIe connector.
- 1x SIM connector.

2.2 SMARC EXPANSION FEATURES

Feature	Specifications
Ethernet	10/100/1000 Mbps base T 1x RJ45 connector
USB 3.0 OTG	1x USB 3.0 type micro AB receptacle
USB 2.0 HOST	3x USB 2.0 type A receptacle
HDMI output	1x HDMI type A receptacle
Button LED	1x Button with blue and red LEDs integrated
RTC battery	Allow to maintain running the Real Time Clock
Expansion 28 pins header	Multiple peripherals: 2x SPI, 1x I2C, 1x I2S, 1x CAN, 2x PWM, RESET. 1x Male header 2x14 pins 2,54mm pitch spacing
Terminal 6 pins plug	Power (5V), RS485 and CAN interfaces are accessible 1x Male header 1x6 pins 5 mm pitch spacing
Serial header expansion	2x RS232 ports 1x Male header 2x5 pins 2.54 mm pitch spacing
Serial debug 3V3 interface header	Serial TTL 3V3 debug port 1x Male header 1x6 pins 2.54 mm pitch spacing
Boot select header	Header to select the boot interface 1x Male header 2x3 pins 2.54 mm pitch spacing
CSI connector	Used to connect cameras with MIPI CSI2 interface
Micro SD connector	Used to insert SD cards
Line-in audio mini jack	1x Stereo audio in
Headphones audio mini jack	1x Stereo audio out
Mic-in audio mini jack	1x Mic-in
DVI-D	DVI-D Interface on HDMI type A receptacle
mSATA connector	Used to connect mSATA disks
USB modem miniPCIe connector	Used to connect miniPCIe modems through USB interface
SIM connector	Used to insert SIM cards
Processor Board Interface	1x SMARC 314 expansion interface
Power	Supply Voltage +5V DC +-10%
Power from terminal 6 pins plug	Supply Voltage +5V DC +-10%

Table 1 Expansion Board Features

2.3 SMARC EXPANSION BLOCK DIAGRAM

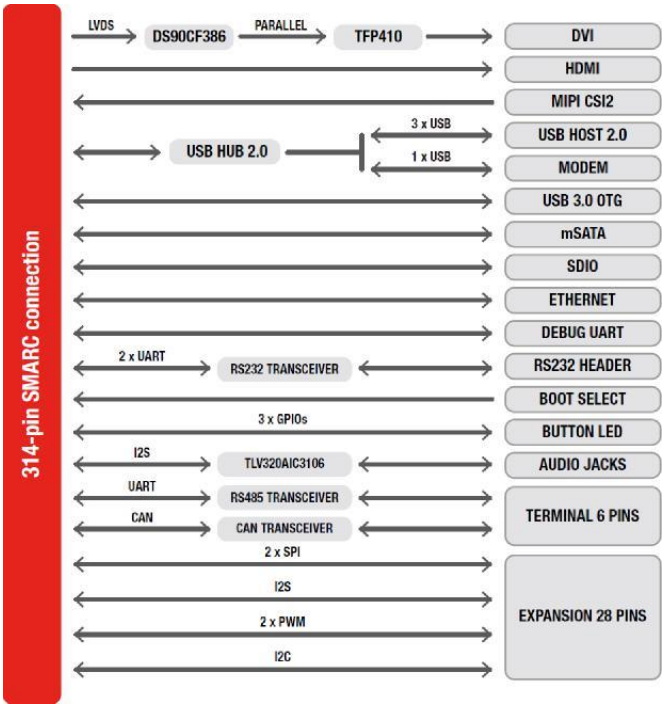

Figure 1 SMARC EXPANSION Block Diagram

Figure 2 SMARC EXPANSION Kit View

3 ON-BOARD INTERFACES

3.1 SUMMARY

Feature	SMARC EXPANSION	SMARC BOARDS interface
Ethernet	J400	GBE
USB 3.0 OTG	J602	USB0 (OTG) and AFB_DIFF0, AFB_DIFF1 (USB3.0)
USB 2.0 HOST	J600(Type A dual) and J601 (Type A)	USB1 (USB hub)
HDMI output	J500 (Type A)	HDMI
Button LED	S1200	GPIO9 (button), GPIO10 (blue LED) and GPIO11 (red LED).
RTC battery	BT300	VDD_RTC
Expansion 28 pins header	J1003	SPI0, I2S1, SPI1, AFB1_OUT (PWM), LCD_BKLT_PWM, WDT_TIME_OUT#, SLEEP#, I2C_PM, AUDIO_MCK and RESET_IN#
Terminal 6 pins plug	J1002	CAN, SER2 and 5V
Serial header expansion	J800	SER0 and SER3 (RS232)
Serial debug 3V3 interface Header	J801	SER1
Boot select header	J1202	BOOT_SEL0#, BOOT_SEL1# and BOOT_SEL2#
CSI connector	J1001	CSI1, GPIO7, GPIO8, I2C_CAM and CAM_MCK
Micro SD connector	J1200	SDIO
Line-in audio mini jack	J904	I2S0, I2C_GP, AUDIO_MCK and GPIO4 (reset) (audio codec)
Headphones audio mini jack	J900	I2S0, I2C_GP, AUDIO_MCK and GPIO4 (reset) (audio codec)
Mic-in audio mini jack	J902	I2S0, I2C_GP, AUDIO_MCK and GPIO4 (reset) (audio codec)
DVI-D	J501	LVDS (converted to DVI lines)
mSATA connector	J1103	SATA
Modem miniPCIe connector	J1100	USB1 (USB hub)
SIM connector	J1102	-
Processor Board Interface	J200	

Table 2 On-Board Interfaces

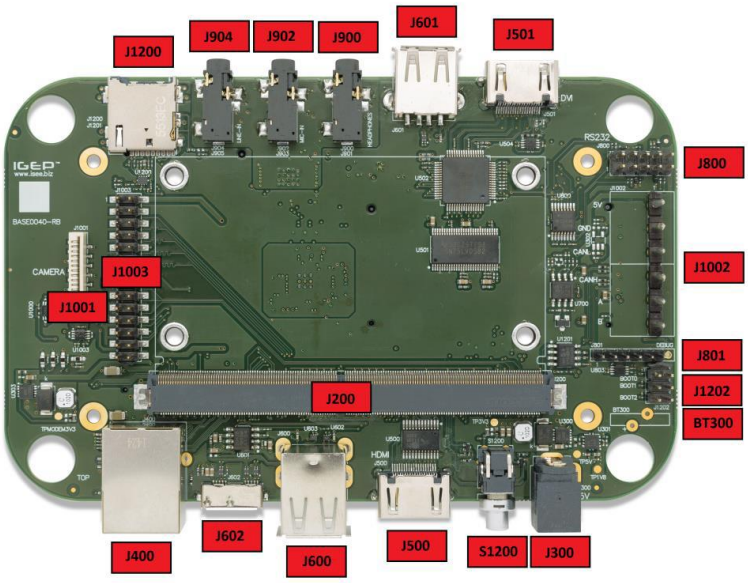

Figure 3 SMARC EXPANSION Interface Connectors Map Top View

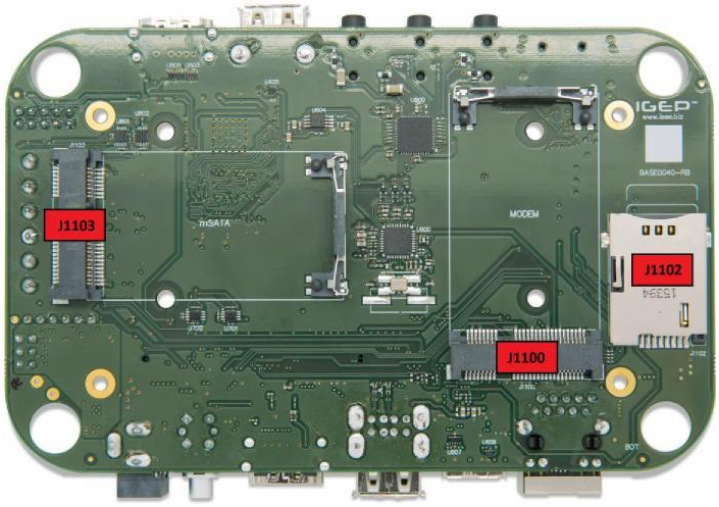

Figure 4 SMARC EXPANSION Interface Connectors Map Bottom View

2.2 ETHERNET

SMARC EXPANSION includes a RJ45 connector (J400), provided for Ethernet Auto-MDIX Full Duplex 10/100/1000 Base T interface. This port is supported by Ethernet Physical Layer Transceiver (PHY) included in the MitySOM-iMX6 modules. The base board only makes a direct link with the Ethernet port.

The Ethernet interface supports the following features:

- Fully compliant with IEEE 802.3/802.3u standards.
- 10BASE-T, 100BASE-T and 1000BASE-T support.
- Full-and Half-duplex support and full-duplex flow control.
- Industrial temperature range (-40°C to 85°C).

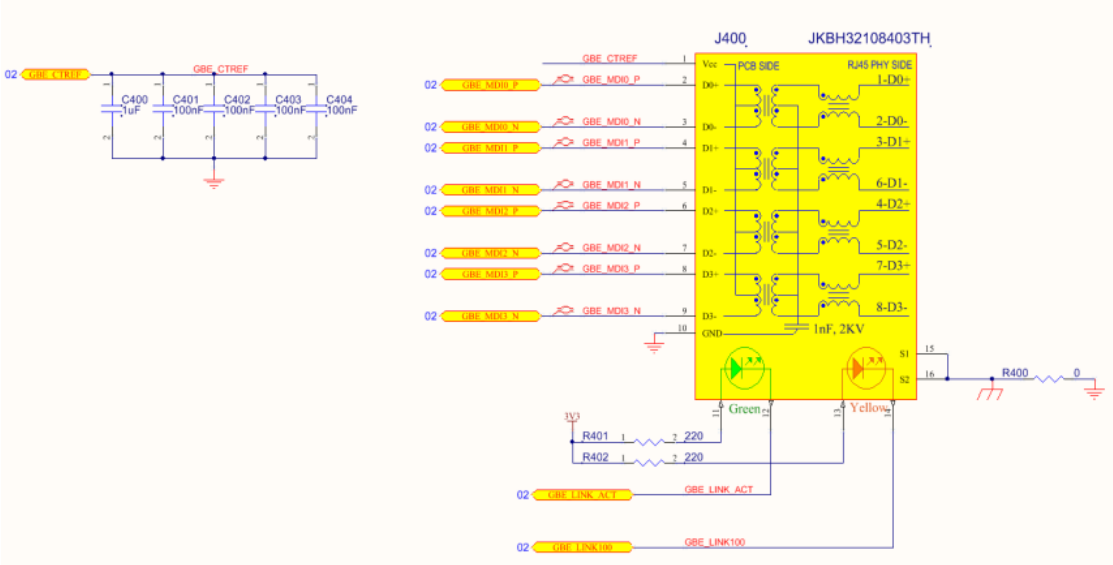

Figure 5 J400 Ethernet Connector Schematic

The Ethernet signals are available through the following connector pins:

Signal Name	SMARC pin	Description
GBE_MDI3-	P19	Analog Transmit/Receive Data 3 Negative. Differential output to magnetics.
GBE_MDI3+	P20	Analog Transmit/Receive Data 3 Positive. Differential output to magnetics.
GBE_LINK100#	P21	Active Low. Means 1000/100 Mbps speed. Inactive if 10 Mbps.
GBE_MDI2-	P23	Analog Transmit/Receive Data 2 Negative. Differential output to magnetics.
GBE_MDI2+	P24	Analog Transmit/Receive Data 2 Positive. Differential output to magnetics.
GBE_LINK_ACT#	P25	Active Low. Indicates valid link and blinks when there is activity.
GBE_MDI1-	P26	Analog Transmit/Receive Data 1 Negative. Differential output to magnetics.
GBE_MDI1+	P27	Analog Transmit/Receive Data 1 Positive. Differential output to magnetics.
GBE_CTREF	P28	Center-Tap reference voltage for Ethernet magnetic (if required by PHY).
GBE_MDI0-	P29	Analog Transmit/Receive Data 0 Negative. Differential output to magnetics.
GBE_MDI0+	P30	Analog Transmit/Receive Data 0 Positive. Differential output to magnetics.

Table 3 Ethernet Signals in J400 RJ45 Connector

3.3 USB 3.0 on-the-go (OTG)

SMARC EXPANSION includes a single USB 3.0 OTG port (J602) directly connected to the USB OTG pins of the MitySOM-iMX6 module interface.

J602 is a USB 3.0 type mini AB receptacle connector. The following figure shows the connection to this port:

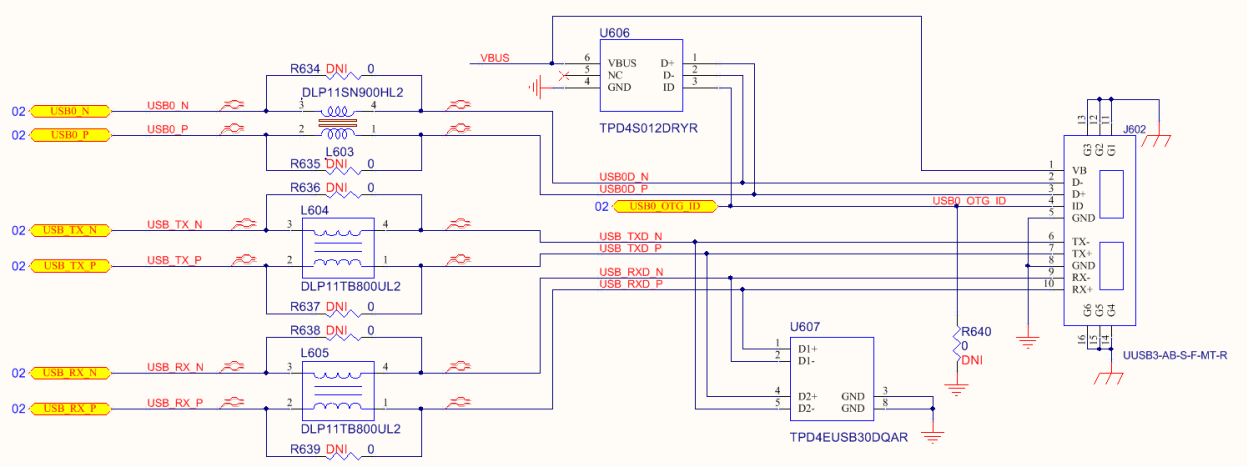

Figure 6 J602 USB 3.0 OTG Connector Schematic

The USB 3.0 OTG interface is implemented with the MitySOM-iMX6 USB OTG controller:

- Operates either as the function controller of a Super/High/Full Speed USB peripheral or as host in point-to-point or multipoint communications.
- Complies with the USB 3.0 standard for SuperSpeed (5 Gbps) function and with OTG supplement.
- Supports USB 3.0 peripheral at SuperSpeed (5 Gbps), High Speed (480 Mbps) and Full Speed (12 Mbps).
- Supports USB 3.0 host at SuperSpeed (5 Gbps), High Speed (480 Mbps), Full Speed (12 Mbps) and Low Speed (1,5 Mbps).

The USB 3.0 OTG signals are available through the following connector pins:

Signal Name	SMARC pin	Description
USB0+	P60	Analog D+ data pin of the USB0
USB0-	P61	Analog D- data pin of the USB0
USB0_VBUS_DET	P63	USB host power detection, when this port is used as a device
USB0_OTG_ID	P64	USB OTG ID input, active high
AFB_DIFF0+ (USB_TX_P)	S62	USB 3.0 transmission line +
AFB_DIFF0- (USB_TX_N)	S63	USB 3.0 transmission line -
AFB_DIFF1+ (USB_RX_P)	S65	USB 3.0 reception line +
AFB_DIFF1- (USB_RX_N)	S66	USB 3.0 reception line -

Table 4 USB 3.0 OTG Signals in J602 Connector

3.4 USB 2.0 HOST

SMARC EXPANSION includes a USB 2.0 Hi-Speed hub controller providing 3x USB 2.0 HS HOST ports available through Type A connectors, J600 and J601 (double and simple respectively). The hardware provides power on/off switch control and up to 500 mA of current limit at 5V on each of three ports. The fourth port of the hub is used for Modem miniPCIe connector. The following figure shows the connection to these ports:

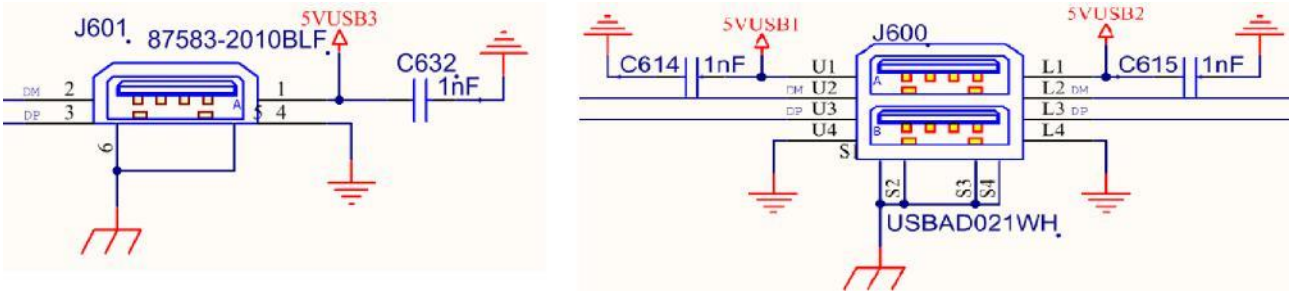

Figure 7 J600 and J601 USB 2.0 HOST Connector Schematic

The USB 2.0 HOST signals are available through the following connector pins:

Signal Name	SMARC pin	Description
USB1+	P65	Analog D+ data pin of the USB1
USB1-	P66	Analog D- data pin of the USB1
USB1_EN_OC#	P67	Active Low. Over current Indication to module
GPIO0	P108	GPIO used to reset HUB controller
GPIO1	P109	GPIO used to enable or disable 5VUSB1
GPIO2	P110	GPIO used to enable or disable 5VUSB2
GPIO3	P111	GPIO used to enable or disable 5VUSB3

Table 5 USB 2.0 HOST Signals in J600 and J601 Connector

3.4 HDMI

SMARC EXPANSION includes an HDMI type A receptacle connector (J500). The following figure shows this connection:

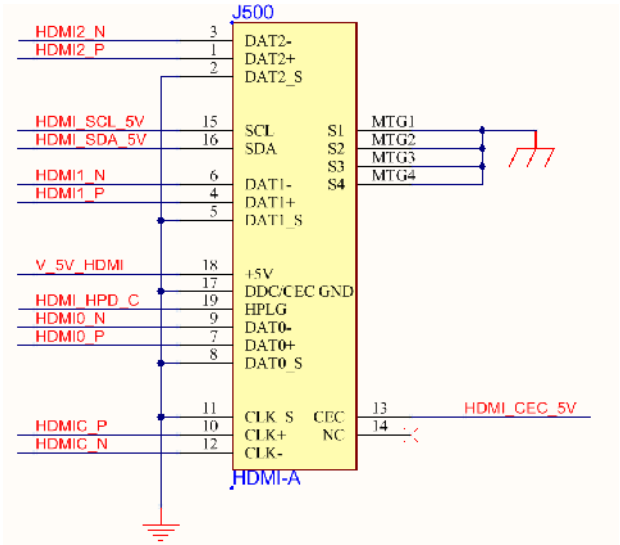

Figure 8 J500 Connector Schematic

The HDMI signals are available through the following connector pins:

Signal Name	SMARC pin	Description
HDMI_D2+	P92	HDMI data differential pair D2 +
HDMI_D2-	P93	HDMI data differential pair D2 -
HDMI_D1+	P95	HDMI data differential pair D1 +
HDMI_D1-	P96	HDMI data differential pair D1 -
HDMI_D0+	P98	HDMI data differential pair D0 +
HDMI_D0-	P99	HDMI data differential pair D0 -
HDMI_CK+	P101	HDMI differential clock output pair +
HDMI_CK-	P102	HDMI differential clock output pair -
HDMI_HPD	P104	HDMI Hot Plug Detect input
HDMI_CTRL_CK	P105	I2C bus clock
HDMI_CTRL_DAT	P106	I2C bus data
HDMI_CEC	P107	HDMI Consumer Electronics Control

Table 6 HDMI Signals in J500 Connector

3.6 BUTTON LED

SMARC EXPANSION includes a button with red and blue LEDs integrated (s1200). The following figure shows this connection:

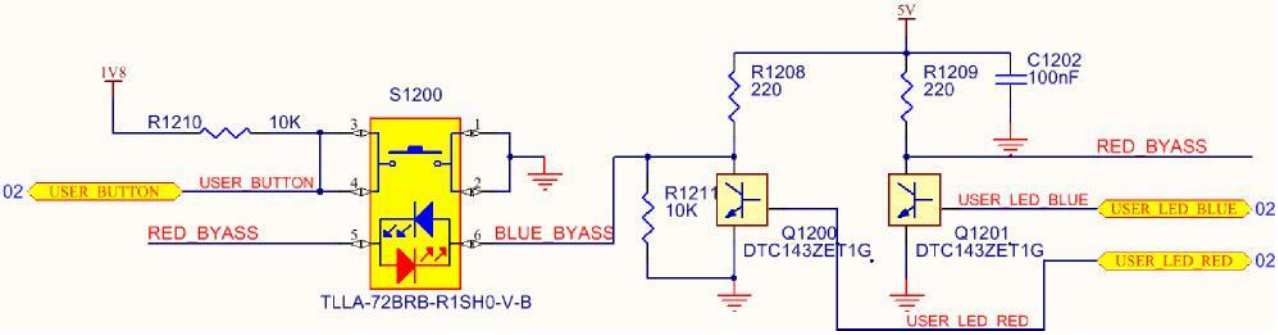

Figure 9 S1200 Button Schematic

The BUTTON LED signals are available through the following connector pins:

Signal Name	SMARC pin	Description
GPIO9	P117	GPIO used to read S1200 input (USER_BUTTON)
GPIO10	P118	GPIO used to control S1200 blue LED (USER_LED_BLUE)
GPIO11	P119	GPIO used to control S1200 red LED (USER_LED_RED)

Table 7 BUTTON LED Signals

3.7 POWER SUPPLY

SMARC EXPANSION must be powered by +5Vdc power source and 5Adc current capacity should be enough to use all board functionalities through J300 or through J1002. The following figure shows the J300 and J1002 connections to power the board:

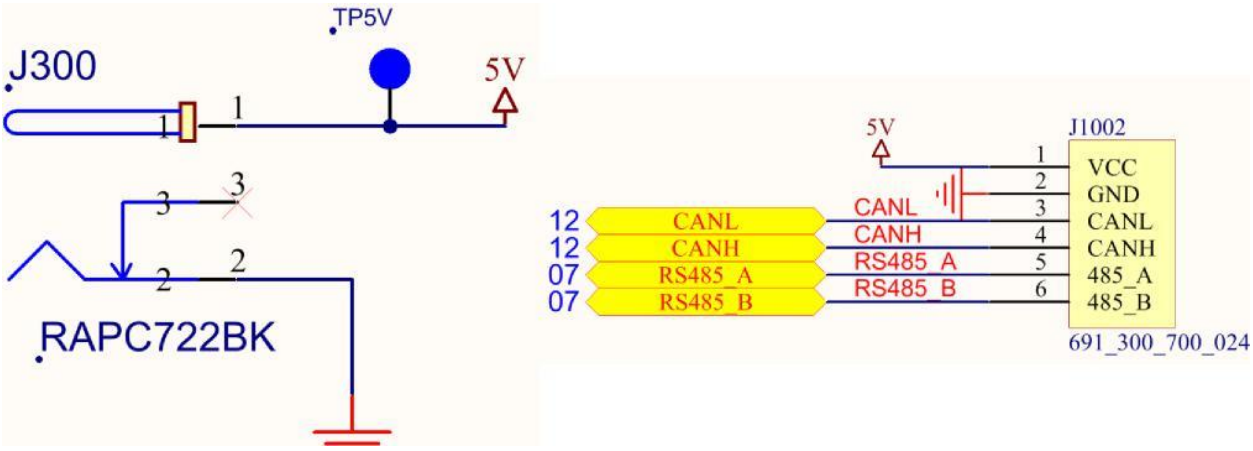

Figure 10 J300 and J1002 Schematics

3.8 RTC BATTERY

SMARC EXPANSION includes a backup battery (BT300) that powers the backup state as far as the input voltage is high enough. It uses VL1220-1VC battery. The following figure shows the BT300 connection:

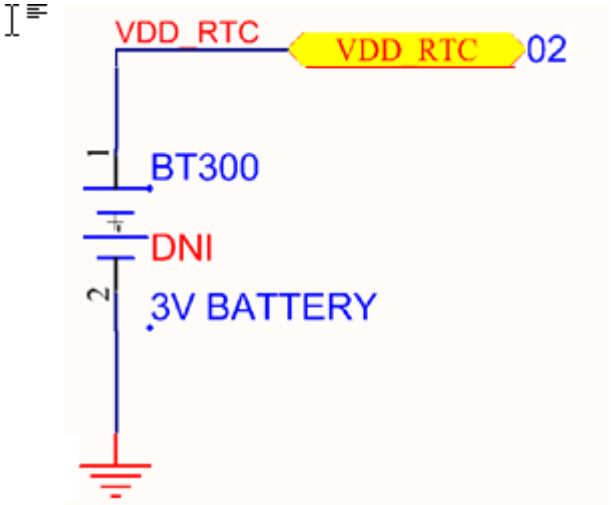

Figure 11 BT300 Schematics

The BUTTON LED signals are available through the following connector pin:

Signal Name	SMARC pin	Description
VDD_RTC	S147	Low current RTC circuit backup power.

Table 8 RTC BATTERY Signals

3.9 EXPANSION HEADERS

3.9.1 EXPANSION 28 PINS HEADER

SMARC EXPANSION includes an expansion header (J1003) that contains features as shown in the next figure:

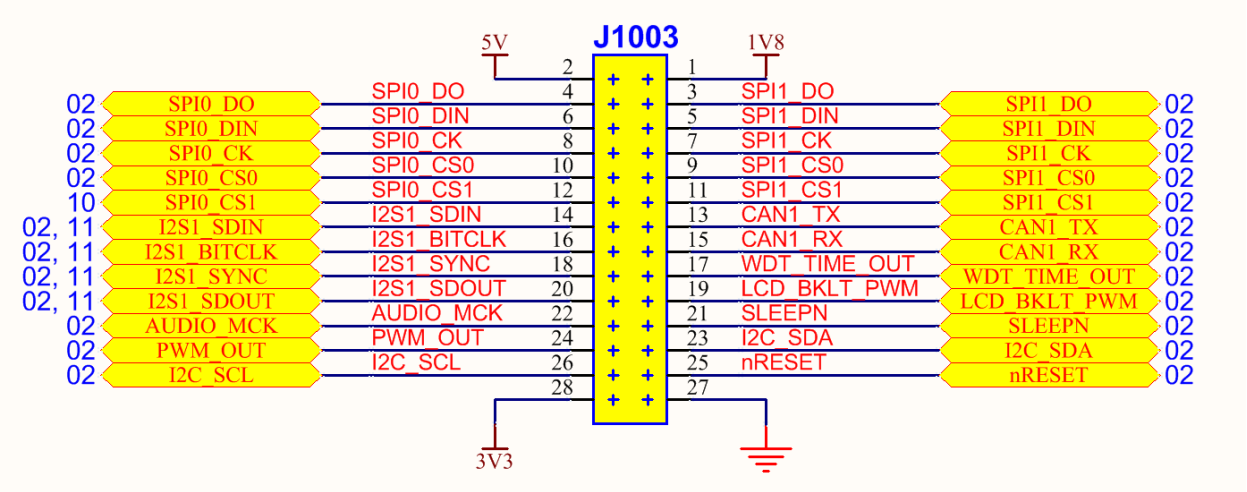

Figure 12 J1003 Schematic

SMARC EXPANSION 28 PINS HEADER signals are available through the following connection pins:

Signal Name	SMARC pin	Description
SPI0_CS1#	P31	SPI0 chip select 1 signal (connected to pin 12)
SPI0_CS0#	P43	SPI0 chip select 0 signal (connected to pin 10)
SPI0_CK	P44	SPI0 clock (connected to pin 8)
SPI0_DIN	P45	SPI0 Master Input-Slave Output(MISO) (connected to pin 6)
SPI0_DO	P46	SPI0 Master Output –Slave Input (MOSI) (connected to pin 4)
SPI1_CS1#	P54	SPI1 chip select 1 signal (connected to pin 11)
SPI1_CS0#	P55	SPI1 chip select 0 signal (connected to pin 9)
SPI1_CK	P56	SPI1 clock (connected to pin 7)
SPI1_DIN	P57	SPI1 Master Input-Slave Output(MISO) (connected to pin 5)
SPI1_DO	P58	SPI1 Master Output –Slave Input (MOSI) (connected to pin 3)
I2C_PM_CK	P121	I2C bus clock (connected to pin 26)
I2C_PM_DAT	P122	I2C bus data (connected to pin 23)
RESET_IN#	P127	Reset input from Carrier board (connected to pin 25)
CAN1_TX	P145	CAN1 Transmission line (connected to pin 13)
CAN1_RX	P146	CAN1 Reception line (connected to pin 15)
AFB1_OUT	S18	PWM output (connected to pin 24)
AUDIO_MCK	S38	Master clock output to Audio codecs (connected to pin 22)
I2S1_LRCK	S43	I2S1 Transmit Frame Sync signal (connected to pin 18)
I2S1_SDOUT	S44	I2S1 Data Transmit signal (connected to pin 20)

Signal Name	SMARC pin	Description
I2S1_SDIN	S45	I2S1 Data Receive signal (connected to pin 14)
I2S1_CK	S46	I2S1 Transmit Clock signal (connected to pin 16)
LCD_BKLT_PWM	S141	Display backlight (connected to pin 19)
WDT_TIME_OUT#	S145	Watch-Dog-Timer Output (connected to pin 17)
SLEEP#	S149	Sleep indicator from Carrier board (connected to pin 21)

Table 9 SMARC EXPANSION 28 PINS HEADER Signals

3.9.2 TERMINAL 6 PINS PLUG

SMARC EXPANSION includes a terminal plug (J1002) that contains power, CAN and RS485 interfaces. It is important to note that CAN signals are CAN bus standard compatible. The following figure shows the J1002 connections:

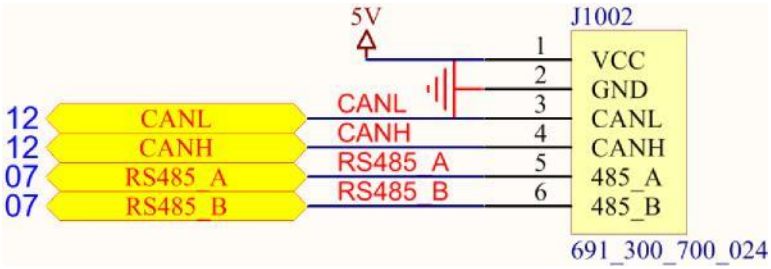

Figure 13 J1002 Schematic

TERMINAL 6 PINS PLUG signals are available through the following connection pins with RS485 and CAN transceivers:

Signal Name	SMARC pin	Description
SER2_TX	P136	SER2 Transmit Data Output
SER2_RX	P137	SER2 Receive Data Input
SER2_RTS#	P138	SER2 RTSn Output
SER2_CTS#	P139	SER2 CTSn Input
CAN0_TX	P143	CAN0 Transmission Line
CAN0_RX	P144	CAN0 Reception Line

Table 10 TERMINAL 6 PINS PLUG Signals

3.9.3 SERIAL HEADER EXPANSION

SMARC EXPANSION includes a serial header expansion (J800) which is a 5x2 pin double row 2.54 mm male header.

The 5x2 Header follows the IDC-10 (AT-Everex) configuration. It requires null modem configuration (connection between two computers). RX and TX lines are crossed in this null modem configuration (TX1->RX2 / TX2->RX1).

The following figure shows the SERIAL HEADER EXPANSION connections:

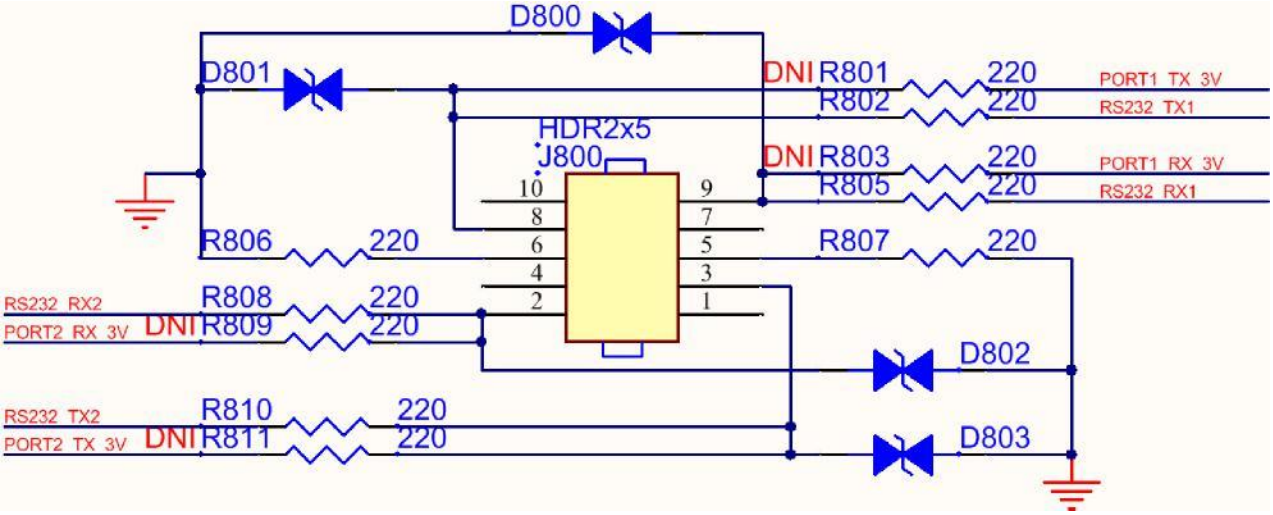

Figure 14 J800 Schematic

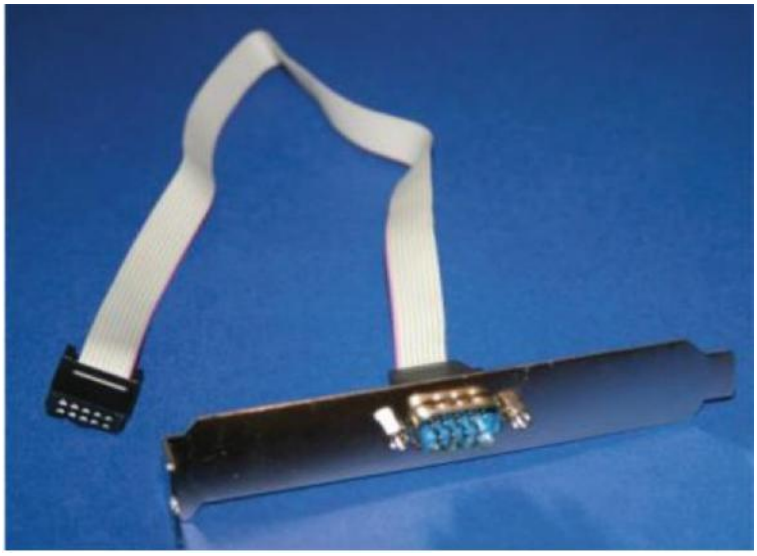

Figure 15 IDC-10 to DB9 Cable

SERIAL HEADER EXPANSION signals are available through the followinf connection pins with RS232 transceiver:

Signal Name	SMARC pin	Description
SER0_TX	P129	SER0 Transmit Data Output (RS232_TX2)
SER0_RX	P130	SER0 Receive Data Input (RS232_RX2)
SER3_TX	P140	SER3 Transmit Data Output (RS232_TX1)
SER3_RX	P141	SER3 Receive Data Input (RS232_RX1)

Table 11 SERIAL HEADER EXPANSION Signals

3.9.4 SERIAL DEBUG 3V3 INTERFACE HEADER

SMARC EXPANSION includes a serial debug header (J801) connected through TXS0102 voltage translator to protect MitySOM-iMX6 modules from latch up currents. J801 has 7 pins with 2.54 mm pitch spacing. This connector lets you debug the system using USB to 3V3 TTL level serial like TTL-232R-3V3 converter from FTDI (http://www.ftdichip.com/Products/Cables/USBTTLSerial.htm) or compatible reference. The TTL-232R-3V3 converter has 6 pins and SMARC EXPANSION adds a seventh way (3v3 power). The following figure shows the SERIAL DEBUG 3V3 INTERFACE HEADER connections:

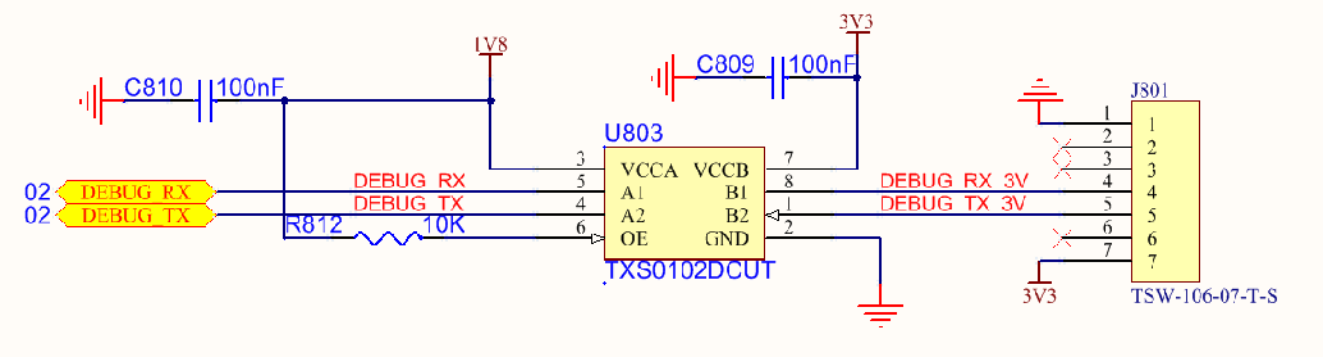

Figure 16 J801 Schematic

SERIAL DEBUG 3V3 INTERFACE HEADER signals are available through the following connection pins:

Signal Name	SMARC pin	Description
SER1_TX	P134	SER1 Transmit Data Output (DEBUG_TX)
SER1_RX	P135	SER1 Receive Data Input (DEBUG_RX)

Table 12 SERIAL DEBUG 3V3 INTERFACE HEADER Signals

3.9.5 BOOT SELECT HEADER

SMARC EXPANSION includes a BOOT SELECT HEADER (J1202). It can modify the module boot up sequence. The following figure shows the BOOT SELECT HEADER connections:

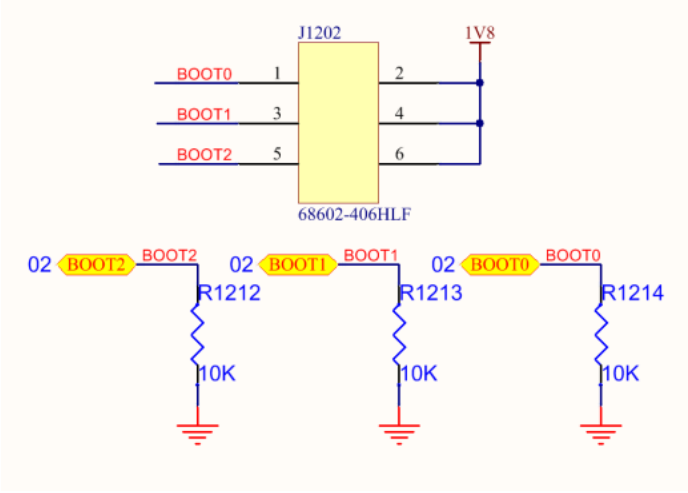

Figure 17 J1202 Schematic

The following table is transcribed from the MitySOM-iMX6 specification. Some MitySOM-iMX6 modules may not support all options. For information, refer to the module documentation.

BOOT_SEL2#	BOOT_SEL1#	BOOT_SEL0#	Boot Source
GND	GND	GND	Carrier SATA
GND	GND	Float	Carrier SD Card
GND	Float	GND	Carrier eMMC Flash
GND	Float	Float	Carrier SPI
Float	GND	GND	Module device (NAND, NOR) – vendor specific
Float	GND	Float	Remote boot (GBE, serial) – vendor specific
Float	Float	GND	Module eMMC Flash
Float	Float	Float	Module SPI

Table 13 Boot Select SMARC Specification

BOOT SELECT HEADER signals are available through the following connection pins:

Signal Name	SMARC pin	Description
BOOT_SEL_0#	P123	Boot select 0
BOOT_SEL_1#	P124	Boot select 1
BOOT_SEL_2#	P125	Boot select 2

Table 14 BOOT SELECT HEADER Signals

3.10 CSI CONNECTOR

SMARC EXPANSION includes a MIPI CSI2 CONNECTOR for MIPI CSI2 cameras which is pin compatible with Raspberry Pi CSI connector. The following figure shows the CSI CONNECTOR connections:

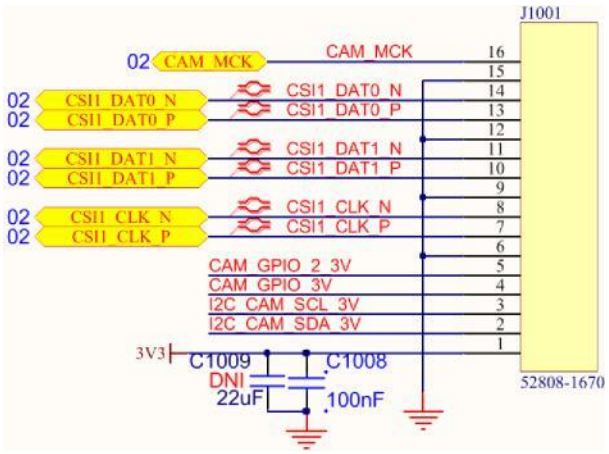

Figure 18 J1001 Schematic

CSI CONNECTOR signals are available through the following connection pins:

Signal Name	SMARC pin	Description
CSI1_CK+	P3	CSI1 differential clock input +
CSI1_CK-	P4	CSI1 differential clock input -
CSI1_D0+	P7	CSI1 differential data input D0 +
CSI1_D0-	P8	CSI1 differential data input D0 -
CSI1_D1+	P10	CSI1 differential data input D1 +
CSI1_D1-	P11	CSI1 differential data input D1 -
I2C_CAM_CK	S5	I2C bus clock (3V3 or 1V8 configurable)
CAM_MCK	S6	Master clock output for CSI camera support
I2C_CAM_SDA	S7	I2C bus data (3V3 or 1V8 configurable)
GPIO7	P115	GPIO used as CAM_GPIO (3V3 or 1V8 configurable)
GPIO8	P116	GPIO used as CAM_GPIO_2 (3V3 or 1V8 configurable)

Table 15 CSI CONNECTOR Signals

3.11 MICRO SD CONNECTOR

SMARC EXPANSION includes a micro-SD connector (J1200). The following figure shows the connections:

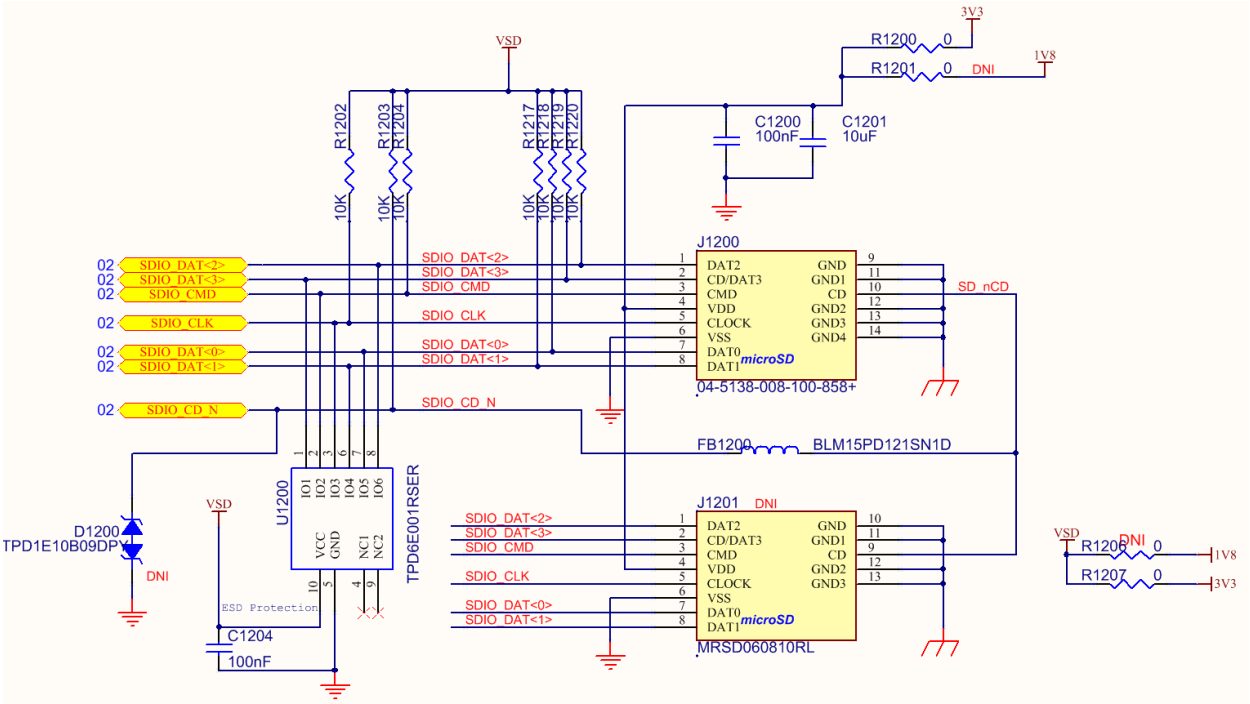

Figure 19 J1200 Schematic

MICRO SD CONNECTOR signals are available through the following connection pins:

Signal Name	SMARC pin	Description
SDIO_CMD	P34	SDIO Command
SDIO_CD#	P35	SDIO Card Detect
SDIO_CK	P36	SDIO Clock
SDIO_D0	P39	SDIO Data Bus 0
SDIO_D1	P40	SDIO Data Bus 1
SDIO_D2	P41	SDIO Data Bus 2
SDIO_D3	P42	SDIO Data Bus 3

Table 16 MICRO SD CONNECTOR Signals

3.12 AUDIO

SMARC EXPANSION includes three 3.5 mm standard stereo input and output audio jacks (J900, J902 and J904) which are provided to access the stereo input, output and mic-in of the audio codec TLV320AIC3106 included on the SMARC EXPANSION board. The following figure shows the TLV320AIC3106 connections:

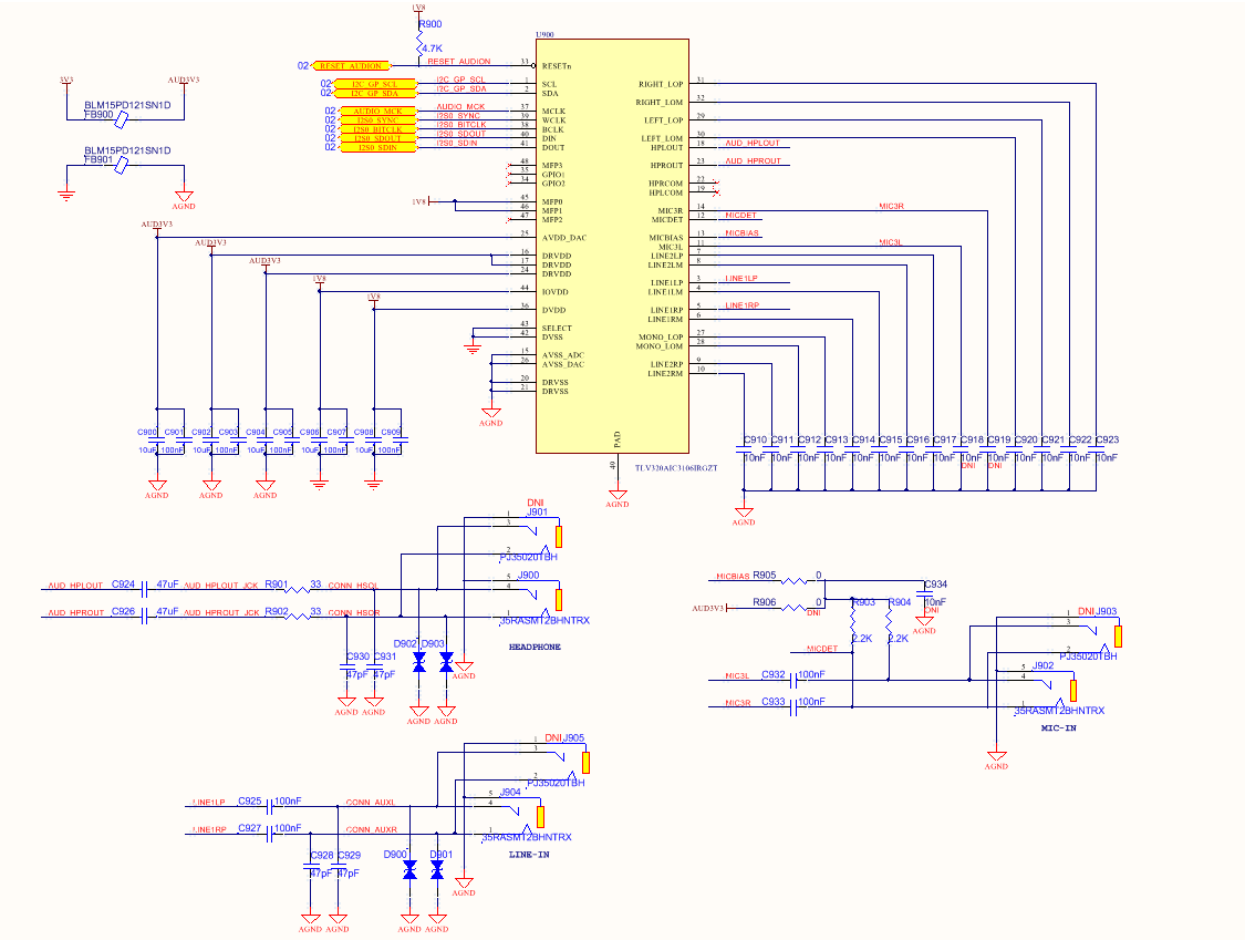

Figure 20 Audio Schematics

AUDIO signals are available through the following connection pins:

Signal Name	SMARC pin	Description
AUDIO_MCK	S38	Master clock output to Audio codecs
I2S0_LRCK	S39	I2S0 Transmit Frame Sync signal
I2S0_SDOUT	S40	I2S0 Data Transmit signal
I2S0_SDIN	S41	I2S0 Data Receive signal
I2S0_CK	S42	I2S0 Transmit Clock signal
I2C_GP_CK	S48	I2C bus clock
I2C_GP_DAT	S49	I2C bus data
GPIO4	P112	GPIO used to reset audio codec

Table 17 AUDIO Signals

3.13 DVI

SMARC EXPANSION includes a DVI interface. This interface is obtained converting LVDS interface to DVI with two chips. These chips convert LVDS to parallel and parallel to DVI respectively. The following figure shows the DVI connections:

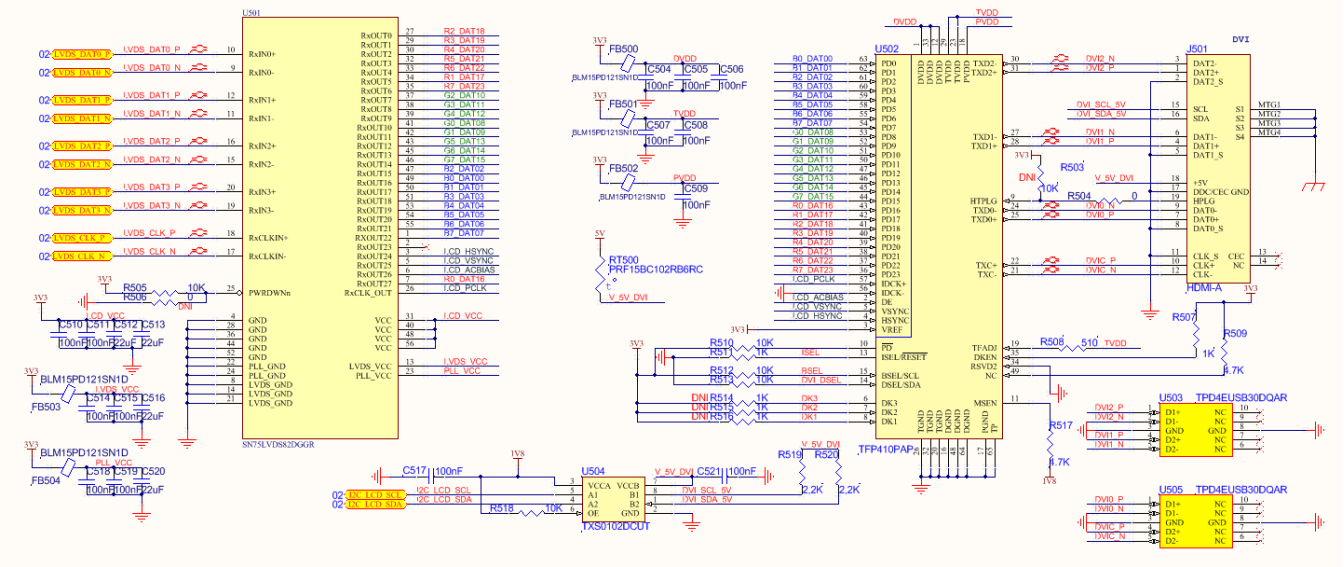

Figure 21 DVI Schematic

DVI signals are available through the following connection pins:

Signal Name	SMARC pin	Description
LVDS0+	S125	LVDS data channel differential pair D0 +
LVDS0-	S126	LVDS data channel differential pair D0 -
LVDS1+	S128	LVDS data channel differential pair D1 +
LVDS1-	S129	LVDS data channel differential pair D1 -
LVDS2+	S131	LVDS data channel differential pair D2 +
LVDS2-	S132	LVDS data channel differential pair D2 -
LVDS_CK+	S134	LVDS clock channel differential pair +
LVDS_CK-	S135	LVDS clock channel differential pair -
LVDS3+	S137	LVDS data channel differential pair D3 +
LVDS3-	S138	LVDS data channel differential pair D3 -
I2C_LCD_CK	S139	I2C bus clock
I2C_LCD_DAT	S140	I2C bus data

Table 18 DVI Signals

3.14 mSATA CONNECTOR

SMARC EXPANSION includes an mSATA CONNECTOR (J1103). The following figure shows the mSATA connections:

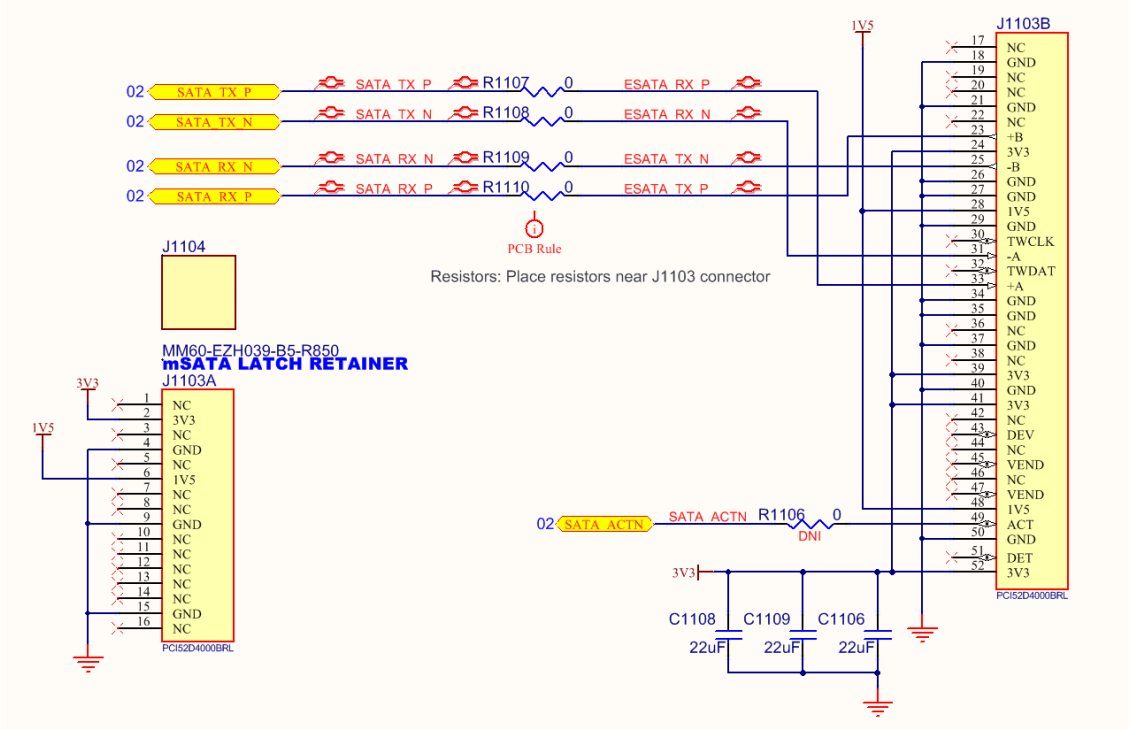

Figure 22 mSATA Schematic

mSATA signals are available through the following connection pins:

Signal Name	SMARC pin	Description
SATA_TX+	P48	Differential SATA transmit data +
SATA_TX-	P49	Differential SATA transmit data -
SATA_RX+	P51	Differential SATA receive data +
SATA_RX-	P52	Differential SATA receive data -
SATA_ACT#	S54	Active low SATA activity indicator

Table 19 SATA Connections

3.15 GSM

SMARC EXPANSION includes GSM Modem connectors, miniPCIe connector for USB modems (J1100) and a SIM card connector (J1102). As it is explained in Section 3.4, the fourth port of USB hub controller is used to establish communication to GSM Modem. The following figure shows the GSM connections:

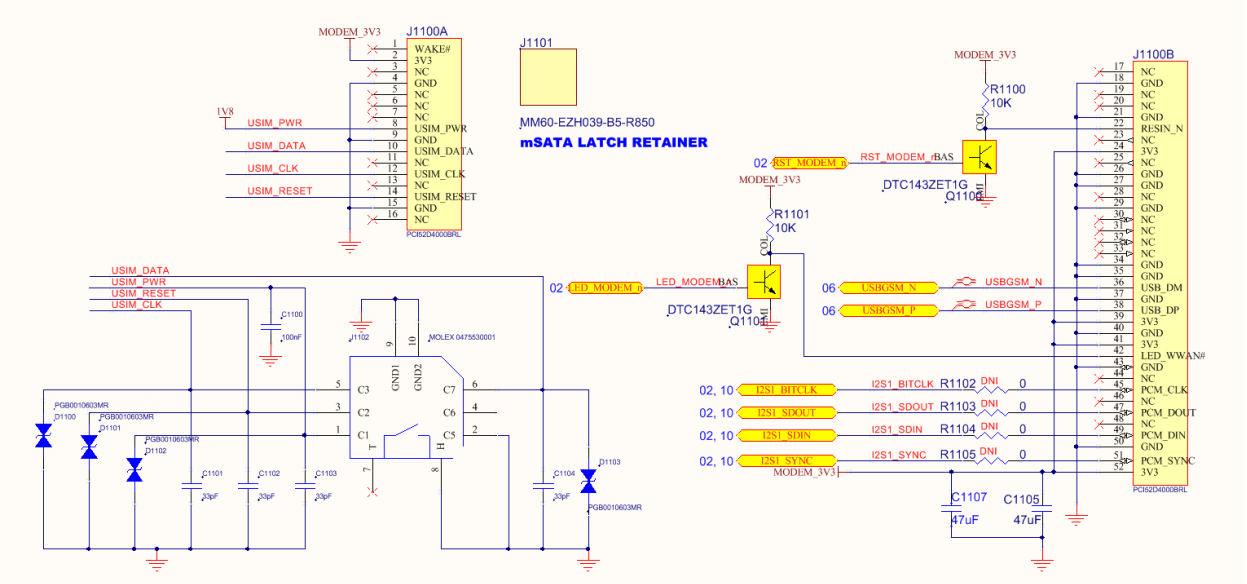

Figure 23 GSM Schematic

GSM signals are available through the following connection pins:

Signal Name	SMARC pin	Description
USB1+	P65	Analog D+ data pin of the USB1
USB1-	P66	Analog D- data pin of the USB1
USB1_EN_OC#	P67	Active low. Over current Indication to module.
I2S1_LRCK	S43	I2S1 Transmit Frame Sync signal
I2S1_SDOUT	S44	I2S1 Data Transmit signal

Signal Name	SMARC pin	Description
I2S1_SDIN	S45	I2S1 Data Receive signal
I2S1_CK	S46	I2S1 Transmit Clock signal
GPIO5	P113	GPIO used to control modem LED
GPIO6	P114	GPIO used to reset GSM Modem

Table 20 GSM Signals

4 MECHANICAL SPECIFICATIONS

The following figure shows the mechanical dimensions of the SMARC EXPANSION board:

1. All dimensions are in millimeters.
2. 6 layer Printed Circuit board size: 142 x 90 mm.
3. MitySOM-iMX6 module size is 82x50 mm.
4. 4 mounting holes (R 1.5 mm) are provided to subject SMARC EXPANSION.
5. 4 mounting holes (R 1.8 mm) are provided for the MitySOM-iMX6 modules.
6. 4 through holes (R 5 mm) are used to insert SMARC EXPANSION in its box.

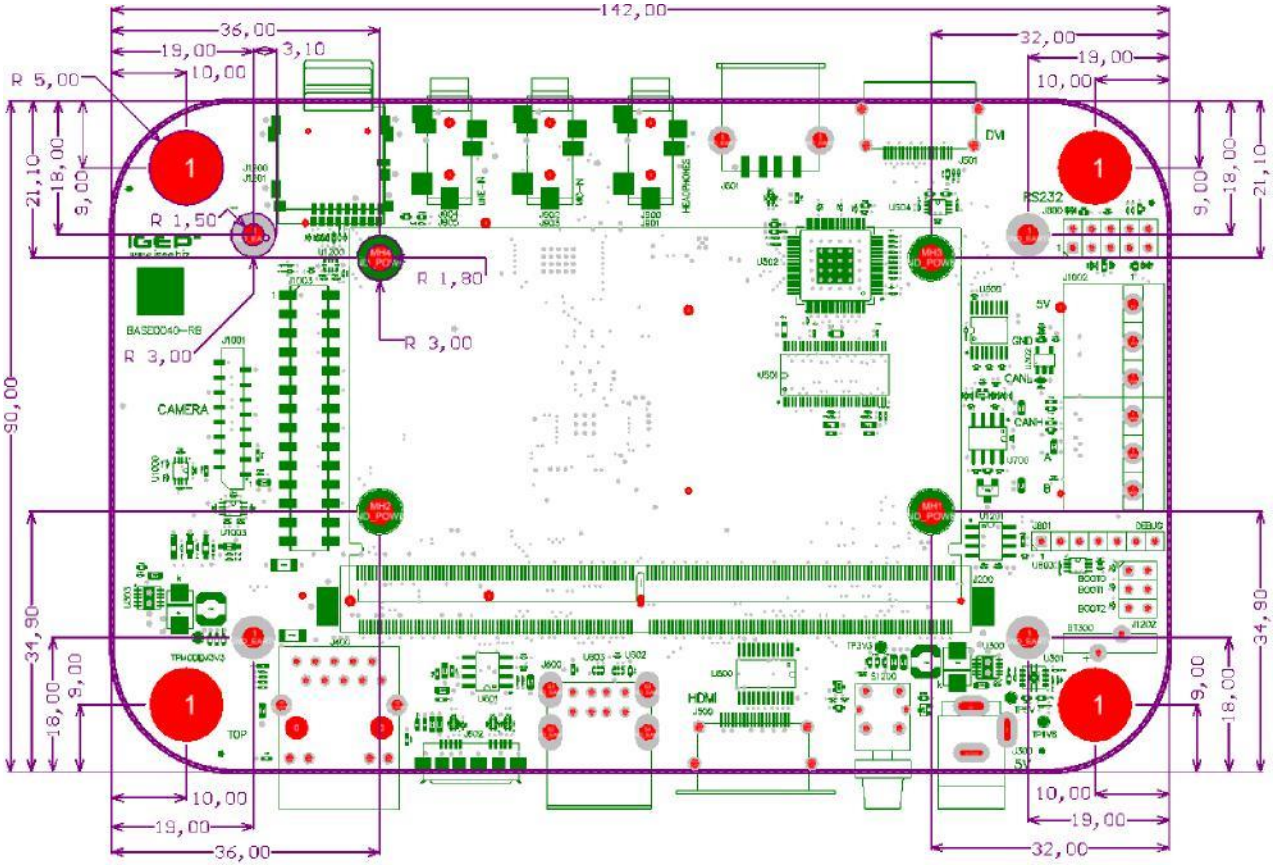

Figure 24 SMARC EXPANSION Mechanical Drawing

5 ELECTRICAL CHARACTERISTICS

All electrical characteristics pins are stablished by SMARC specification.

Electrical parameter	Min	Typ	Max	Unit
5V INPUT POWER SUPPLY				
SMARC EXPANSION DC INPUT POWER SUPPLY	4.75	5	5.25	V
SMARC EXPANSION DC INPUT CURRENT(1)	100	360	1200	mA
IO pins				
Input/output High-Level DC voltage(1)	1.26	1.8	2.1	V
Input/output Low-Level DC voltage(1)	-0.5	0	0.54	V
Output drive current(1)	-0.1	0.5	1	mA
RTC_BATTERY type pins				
Input DC voltage	2.5	3	3.3	V
SPI, I2C, I2S, UART				
Input/output High-Level DC voltage(1)	1.26	1.8	2.1	V
Input/output Low-Level DC voltage(1)	-0.5	0	0.54	V
Output drive current(1)	-0.1	0.5	1	mA
USB type pins				
Input/output High-Level DC voltage	4.75	5	5.25	V
Output drive current	0	500	500	mA
SDIO type pins				
Input/output High-Level DC voltage(1)	2.9	3.3	3.4	V
Output drive current(1)	0	1	2	mA
ETH type pins				
Input/output High-Level DC voltage(1)	1.26	1.8	2.1	V
Input/output Low-Level DC voltage(1)	-0.5	0	0.54	V
Output drive current(1)	-0.1	0.5	1	mA

Table 21 SMARC EXPANSION Electrical Characteristics

(1 - Values depends on which MitySOM-iMX6 module is used.)

SMARC EXPANSION BOARDS CAN BE DAMAGED IF ANY OF THESE ELECTRICAL LIMITS ARE EXCEEDED AND/OR ELECTROSTATIC DISCHARGE PRECAUTIONS ARE NOT FOLLOWED. **WARRANTY LOST** IF IMPROPER USE OF THE MODULE IS FOUND.

6 CHANGE HISTORY

Revision	Date	Description
1A	2017-Mar-08	Initial Release
1B	2018-Mar-20	Updated figures to improve image quality.

Table 22 Change History