MityDSP™ Document

Document: MityDSP-Pro™ Carrier Board Design Guide

Revision: 1.1

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1 Overview

1.1 Fast Facts for Getting Started

Facts	MityDSP-Pro
Required socket connector	FCI: 10033853-152FSLF
Voltages required	3.3V
Supported I/O standards	LVTTL, LVCMOS33, LVCMOS25, LVDS25
Total number of FPGA I/O's	140 G.P. + 8 other
Number of LVDS capable I/O's	140 (70 pairs)

1.2 Introduction

MityDSP modules are designed to be easy to integrate into an end-user embedded system. The modules integrate many crucial elements of an embedded DSP system, and do so with an established design framework utilizing a common set of core libraries. End-user design of the application PCB is also intended to be as simple as possible, allowing the PCB designer to concentrate on the custom I/O interfaces – especially analog & mixed-signal – instead of getting distracted with the learning curve of designing a brand new embedded digital system from scratch.

1.3 MityDSP™ Modules

There are three main types of MityDSP modules. The original MityDSP module is based on a Texas Instruments TMS320C6711 DSP, includes SDRAM and Flash memories, and is interfaced by a 144-pin SO-DIMM card-edge connector. The module also integrates a Xilinx Spartan3 FPGA for implementing required on-board logic, and also for end-user customizable logic and I/O interfaces. Also available in the same footprint is the MityDSP-XM, which includes more memory and a larger FPGA than the original module.

A more powerful module, the MityDSP-Pro is based on a Texas Instruments TMS320C645x DSP, includes DDR2 SDRAM and Flash memories, and is interfaced by a 200-pin SO-DIMM card-edge connector and a 100-pin high-density, low-profile Hirose connector. The module integrates a large Xilinx Spartan3 FPGA for implementing required on-board logic and I/O interfaces, and also for end-user customizable logic and I/O interfaces. The

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module also incorporates a number of powerful features not available on the original MityDSP platform. These include: PCI/HPI, Serial RapidIO (C6455 only), and Gigabit Ethernet interfaces provided by the DSP; DDR SDRAM dedicated to the FPGA; all external FPGA I/O is LVDS capable; and all core power regulation is done on-board. Carrier board design for the MityDSP-Pro is the main focus of this document.

All types of MityDSP are available with options for speed grade, memory size, FPGA size, operating temperature ranges, and RoHS / non-RoHS compliance. Please contact Critical Link for the current list of MityDSP variants.

1.4 Module Dimensions

The MityDSP-Pro module is slightly more than twice the size of the original MityDSP module, but the same exact width at the edge connector. A dimensioned drawing of the MityDSP-Pro module is included below in Figure 1.

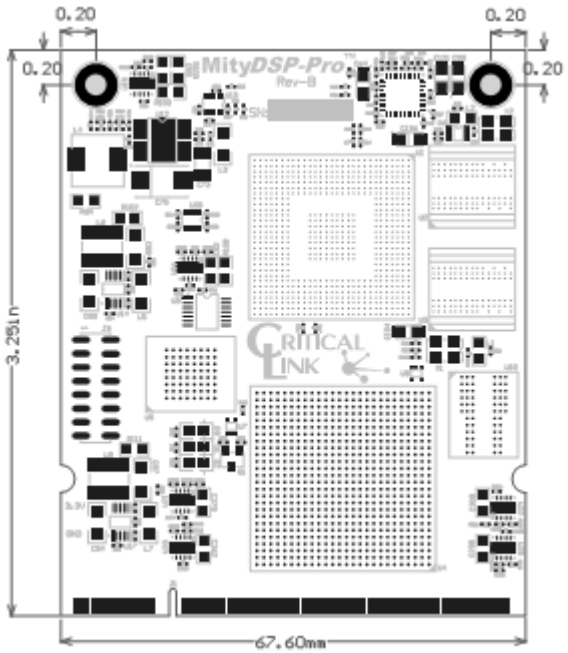

Figure 1: MityDSP-Pro Mechanical Drawing

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2 Connectors

All types of MityDSP utilize SO-DIMM style edge-connectors for main connectivity with the end user application PCB. These connectors were chosen for their high density, compact size, ease of procurement, and low cost. With edge connectors, a physical socket component is only required on one side – the main PCB side. The SO-DIMM standard also allows the MityDSP module to lay flat, in parallel with the main PCB, as they were intended for use by memory modules in compact equipment, such as laptops.

2.1 Card-edge compatibility

The MityDSP-Pro module is designed to plug into a 200-pin SO-DIMM DDR2 memory module socket. It was desired to have more I/O capability than the original MityDSP, but keep the same style of connector, and this socket fit the bill. These sockets currently are commonly used as memory sockets in compact PC equipment, such as laptops. The rationale for the decision to use this connector, despite them being still in common use, is that in practice it is unlikely that a MityDSP-Pro will be used in the same system with a DDR2 memory module. However, in the event that a board is designed for both sockets, it would be wise to clearly label the two sockets, even though the MityDSP-Pro module is much longer than a standard DDR2 memory module, and might be obvious where each one is supposed to fit. Please note that although they share the same physical connection, the MityDSP-Pro and DDR2 memory module standards are NOT electrically compatible, and intermixing modules/sockets from the two standards would very possibly cause permanent damage to one or both sides.

2.2 MityDSP-Pro Module Pin-out

Table 1: MityDSP-Pro Card-edge (J1) Pin-Out

Pin #	Signal	FPGA Bank	Signal	Pin #
1	+3.3V	-	+3.3V	2
3	+3.3V	-	+3.3V	4
5	+3.3V	-	+3.3V	6
7	GND	-	GND	8
9	GND	-	GND	10
11	MRESET#	-	BOOT_MODE	12
13	ETH_TD_P	-	RS232_TXD	14
15	ETH_TD_N	-	RS232_RXD	16
17	ETH_RD_P	-	RS232_RTS	18
19	ETH_RD_N	-	RS232_CTS	20
21	FPGA_RSV1	-	SCL	22
23	FPGA_RSV2	-	SDA	24
25	CLKR0	-	CLKR1	26
27	CLKX0	-	CLKX1	28
29	DR0	-	DR1	30
31	DX0	-	DX1	32
33	FSR0	-	FSR1	34
35	FSX0	-	FSX1	36

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Pin #	Signal	FPGA Bank	Signal	Pin #
37	VCCO_2	-	VCCO_1	38
39	VCCO_0	-	VCCO_7	40
Mechanical Key Gap				
41	GND	-	GND	42
43	ODD1_P.N26	2	EVN1_P.N22	44
45	ODD1_N.N25	2	EVN1_N.N21	46
47	ODD2_P.M26	2	EVN2_P.N24	48
49	ODD2_N.M25	2	EVN2_N.N23	50
51	ODD3_P.M22	2	EVN3_P.M24	52
53	ODD3_N.M21	2	EVN3_N.L23	54
55	ODD4_P.L26	2	EVN4_P.K24	56
57	ODD4_N.L25	2	EVN4_N.K23	58
59	ODD5_P.K26	2	EVN5_P.J25	60
61	ODD5_N.K25	2	EVN5_N.J24	62
63	GND	-	GND	64
65	ODD6_P.K22	2	EVN6_P.H24	66
67	ODD6_N.K21	2	EVN6_N.H23	68
69	ODD7_P.H26	2	EVN7_P.J23	70
71	ODD7_N.H25	2	EVN7_N.J22	72
73	ODD8_P.J21	2	EVN8_P.H21	74
75	ODD8_N.H22	2	EVN8_N.H20	76
77	ODD9_P.D26	2	EVN9_P.E24	78
79	ODD9_N.D25	2	EVN9_N.E23	80
81	ODD10_P.F21	1	EVN10_P.C23	82
83	ODD10_N.E21	1	EVN10_N.B23	84
85	GND	-	GND	86
87	ODD11_P.E20	1	EVN11_P.C22	88
89	ODD11_N.D20	1	EVN11_N.B22	90
91	ODD12_P.B21	1	EVN12_P.D21	92
93	ODD12_N.A21	1	EVN12_N.C21	94
95	ODD13_P.B20	1	EVN13_P.G18	96
97	ODD13_N.A20	1	EVN13_N.F18	98
99	ODD14_P.B19	1	EVN14_P.G17	100
101	ODD14_N.A19	1	EVN14_N.F17	102
103	ODD15_P.F16	1	EVN15_P.E17	104
105	ODD15_N.E16	1	EVN15_N.D17	106
107	GND	-	GND	108
109	ODD16_P.B15	1	EVN16_P.F15	110
111	ODD16_N.A15	1	EVN16_N.E15	112
113	ODD17_P.C14	1	EVN17_P.E14	114
115	ODD17_N.B14	1	EVN17_N.D14	116
117	ODD18_P.A13	0	EVN18_P.F13	118
119	ODD18_N.B13	0	EVN18_N.G13	120
121	ODD19_P.A12	0	EVN19_P.C13	122
123	ODD19_N.B12	0	EVN19_N.D13	124
125	ODD20_P.H13	0	EVN20_P.E12	126
127	ODD20_N.G12	0	EVN20_N.F12	128
129	GND	-	GND	130

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Pin #	Signal	FPGA Bank	Signal	Pin #
131	ODD21_P.F11	0	EVN21_P.D11	132
133	ODD21_N.G11	0	EVN21_N.E11	134
135	ODD22_P.A8	0	EVN22_P.C10	136
137	ODD22_N.B8	0	EVN22_N.D10	138
139	ODD23_P.A7	0	EVN23_P.E10	140
141	ODD23_N.B7	0	EVN23_N.F10	142
143	ODD24_P.D7	0	EVN24_P.F9	144
145	ODD24_N.E7	0	EVN24_N.G9	146
147	ODD25_P.D6	0	EVN25_P.B6	148
149	ODD25_N.E6	0	EVN25_N.C6	150
151	GND	-	GND	152
153	ODD26_P.A4	0	EVN26_P.B5	154
155	ODD26_N.B4	0	EVN26_N.C5	156
157	ODD27_P.D2	7	EVN27_P.J5	158
159	ODD27_N.D1	7	EVN27_N.J4	160
161	ODD28_P.H5	7	EVN28_P.H4	162
163	ODD28_N.J6	7	EVN28_N.H3	164
165	ODD29_P.K6	7	EVN29_P.J3	166
167	ODD29_N.K5	7	EVN29_N.J2	168
169	ODD30_P.G2	7	EVN30_P.K4	170
171	ODD30_N.G1	7	EVN30_N.K3	172
173	GND	-	GND	174
175	ODD31_P.H2	7	EVN31_P.L6	176
177	ODD31_N.H1	7	EVN31_N.L5	178
179	ODD32_P.K2	7	EVN32_P.M5	180
181	ODD32_N.K1	7	EVN32_N.M6	182
183	ODD33_P.L2	7	EVN33_P.L4	184
185	ODD33_N.L1	7	EVN33_N.M3	186
187	ODD34_P.M2	7	EVN34_P.N4	188
189	ODD34_N.M1	7	EVN34_N.N3	190
191	ODD35_P.N2	7	EVN35_P.N6	192
193	ODD35_N.N1	7	EVN35_N.N5	194
195	GND	-	GND	196
197	+3.3V	-	+3.3V	198
199	+3.3V	-	+3.3V	200

Table 2: MityDSP-Pro Auxiliary I/O Connector (J2) Pin-out

Pin	Signal	Signal	Pin
1	GND	GND	2
3	RIORX0_N	RIOTX0_P	4
5	RIORX0_P	RIOTX0_N	6
7	RIORX1_P	RIOTX1_P	8
9	RIORX1_N	RIOTX1_N	10
11	RIORX2_N	RIOTX2_N	12
13	RIORX2_P	RIOTX2_P	14
15	RIORX3_P	RIOTX3_N	16
17	RIORX3_N	RIOTX3_P	18

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Pin	Signal	Signal	Pin
19	RIOCLK_N	GND	20
21	RIOCLK_P	HPI_WIDTH	22
23	GND	PCI_AD27	24
25	PCI_EEAI	PCI_AD1	26
27	PCI66	PCI_AD30	28
29	PCI_EN	PCI_AD0	30
31	PCI_AD11	PCI_AD4	32
33	PCI_AD10	PCI_AD22	34
35	PCI_AD3	PCI_AD25	36
37	PCI_AD5	PCI_AD8	38
39	PCI_AD29	PCI_AD21	40
41	PCI_AD23	PCI_AD13	42
43	PCI_AD7	PCI_AD2	44
45	PCI_AD9	PCI_AD19	46
47	PCI_AD28	PCI_AD15	48
49	PCI_AD31	PCI_ERR#	50
51	PCI_AD16	PCI_AD17	52
53	PCI_AD6	PCI_AD18	54
55	PCI_AD14	PCI_STOP#	56
57	GND	PCI_AD26	58
59	PCI_CLK	PCI_AD20	60
61	GND	PCI_CBE2#	62
63	PCI_AD12	PCI_AD24	64
65	PCI_FRAME#	PCI_SERR#	66
67	PCI_DEVSEL#	PCI_RST#	68
69	PCI_PAR	PCI_CBE1#	70
71	PCI_IDSEL	PCI_CBE0#	72
73	PCI_IRDY#	PCI_CBE3#	74
75	PCI_GNT#	PCI_REQ#	76
77	PCI_INTA#	MAC_SEL	78
79	PCI_TRDY#	RGMII_VREF	80
81	GND	GND	82
83	RGMDCLK	RGREFCLK	84
85	RGMDIO	GND	86
87	RGRXD3	RGTXD3	88
89	RGRXD2	RGTXD2	90
91	RGRXD1	RGTXD1	92
93	RGRXD0	RGTXD0	94
95	RGRXCTL	RGTXCTL	96
97	RGRXC	RGTXC	98
99	GND	GND	100

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Table 3: MityDSP-Pro Debug Header (J3) Pin-out

Pin	Signal	Signal	Pin
1	DSP_EMU0	DSP_TMS	2
3	DSP_EMU1	DSP_TDI	4
5	3.3V	DSP_TDO	6
7	GND	DSP_TCK	8
9	GND	DSP_TRST#	10
11	FPGA_TDI	FPGA_TMS	12
13	FPGA_TCK	FPGA_TDO	14
15	GND	2.5V	16

Table 4: MityDSP-Pro Signal Group Description

Signal / Group	Type	Description
+3.3V	PWR	3.3 volt input power referenced to GND.
MRESET#	I	Manual Reset. Pulled-up on the MityDSP-Pro module. When driven to GND for a minimum of 1 us, a module-wide reset is triggered. Can be tied into system system-wide reset and power monitoring circuitry.
ETH_TD_P / N ETH_RD_P / N	O I	Ethernet Transmit Data & Receive Data link lines. These pairs of signals are connected to the onboard 10/100 Ethernet PHY connected to the DSP EMAC. These pairs should be routed as differential-pairs to appropriate 1:1 Ethernet MDI-X transformers prior to exposure to an RJ-45 type connector interface. The center-tap of the transformers these signals attach to should be tied to system 3.3V, and bypassed with a 0.1uF capacitor to GND on each.
FPGA_RSV1 / 2	I/O	Reserved for Ethernet RJ45 Link & Activity LED signals, driven by the on-board 10/100 PHY. Can also be used as general purpose FPGA I/O. FPGA_RSV1 is on FPGA pin P26, and FPGA_RSV2 is on FPGA pin P25.
CLKR0 / 1 CLKX0 / 1 DR0 / 1 DX0 / 1 FSR0 / 1 FSX0 / 1	I/O	These pins are direct connects to the corresponding McBSP port-0 / port-1 pins on the C645x DSP. For further interface information, please consult the DSP datasheet and McBSP User's Guide.
BOOT_MODE	I	Boot Mode Selection. Reserved for future use. Do not connect.
SDA, SCL	I/O	These pins are connected to the I2C interface on the C645x DSP. The signals are also routed to FPGA pins: SDA is on P23, and SCL is on P24. For further interface information, please consult the DSP datasheet and I2C User's Guide.
GND	PWR	System Digital Ground.

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Signal / Group	Type	Description
ODDxx_P/N.YYY EVNxx_P/N.YYY	I/O	FPGA General Purpose I/O pin. FPGA I/O pins have been routed to the MityDSP connector in pairs denoted ODDxx (odd pin side of connector) or EVNxx (even pin side of connector). When configured for differential termination the pairs should be used according to the _P (positive) or _N (negative) extension. The YYY portion of the name corresponds to the FPGA pin location mapped to the signal.
VCCO_n	PWR	FPGA Banks 0, 1, 2, and 7 voltage configuration. Leave disconnected for 2.5V bank logic (LVCMOS25 or LVDS25). Connect to 3.3V power supply for 3.3V bank logic (LVCMOS33 or LVTTL). PCB trace must be capable of providing a minimum of 200 mA.
RIOCLK125P / N RIORXnP / N RIOTXnP / N	I I O	Serial RapidIO (SRIO) differential signal pairs. Applicable to the TMS320C6455 DSP only. These signals are connected directly to their corresponding DSP pins via differential pair traces. The input pairs are AC coupled with 0.01uF capacitors at the DSP package pins, while the output pairs are direct connects. For further information, please consult the TMS320C6455 datasheet and Serial RapidIO User's Guide.
HPI_WIDTH	I	HPI peripheral bus width selection. Applies only when HPI is enabled: PCI_EN = 0. 0 (left floating) = 16-bits wide (default). 1 (tied to 3.3V) = 32-bits wide.
PCI_EEAI	I	PCI I2C EEPROM Auto-Initialization. Applies only when PCI is enabled: PCI_EN = 1. 0 (left floating) = PCI I2C EEPROM Auto-Init. disabled (default). 1 (tied to 3.3V) = PCI I2C EEPROM Auto-Init. enabled. Must not be enabled if PCI is disabled.
PCI66	I	PCI bus operational speed selection. Applies only when PCI is enabled: PCI_EN = 1. 0 (left floating) = PCI operates at 33MHz (default). 1 (tied to 3.3V) = PCI operates at 66MHz. Must not be enabled if PCI is disabled.
PCI_EN	I	PCI / HPI peripheral function enable. 0 (left floating) = HPI is enabled (PCI disabled) at device reset. 1 (tied to 3.3V) = PCI is enabled (HPI disabled) at device reset.
PCI_*	I/O	PCI & HPI shared signals. Signals are connected directly to the DSP pins, and are named by their PCI functions. For more information, including the mapping to HPI pin functions, please consult the DSP datasheet and PCI and HPI User's Guides.
MAC_SEL	I	Ethernet MAC interface selection. 0 (left floating) = 10/100 EMAC via on-module PHY (default). 1 (tied to 3.3V) = 10/100/1000 EMAC with RGMII interface to off-module RGMII-capable Gigabit Ethernet PHY.
RGMII_VREF	A	RGMII Analog Voltage Reference. RGMII uses 1.5V HSTL signaling, so the reference voltage is set at 0.75V.
RGREFCLK	O	RGMII Reference Clock. A 125MHz clock signal is provided on this pin as a convenient clock source to an off-module RGMII-capable Gigabit Ethernet PHY.

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Signal / Group	Type	Description
RGMDCLK RGMDIO	O I/O	RGMII mode EMAC Management Data I/O (MDIO) clock & data signals. Connect to an off-module RGMII-capable Gigabit Ethernet PHY.
RGRX* RGTX*	I O	RGMII mode EMAC clock, data, and control signals. Connect to an off-module RGMII-capable Gigibit Ethernet PHY.
DSP_*	I/O	DSP JTAG/Emulation signals.
FPGA_*	I/O	FPGA JTAG signals.

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3 Electrical Requirements

The following sections describe the various electrical requirements for the MityDSP-Pro module.

3.1 Power Supplies

The MityDSP-Pro module requires only one regulated power supply for the main +3.3V I/O power rail. All other required power rails are generated on-module by a combination of switching and linear, high-efficiency voltage regulators. The main +3.3V power rail can be sourced by either a linear or switching regulator as system requirements dictate, however due to the fairly high load current, a switching regulator will be the most efficient. Table 5 describes the specifications of the input voltage, allowed ripple, and current requirements.

Table 5: Module Voltage and Current Specifications

Module	Spec.	Minimum	Typical	Maximum	Units
MityDSP-Pro	$V_{3.3}$	3.14	3.3	3.46	V
	$I_{3.3}$	TBD	TBD	TBD	mA

3.2 Recommended Capacitance

The MityDSP-Pro module includes some power supply rail bypass capacitors on-board, however additional capacitance is recommended on the carrier board to minimize the ripple effect caused by changing load currents. It is common practice to place one 10uF tantalum capacitor nearby each power supply pin pair. On the MityDSP-Pro module, there are ten 3.3V power pins, or five pairs, so five capacitors are required. It would also be sensible to include additional capacitance for the VCCO pins if they are powered by 3.3V, though this is not required as each FPGA bank is well bypassed on-module. Please note that this is the minimum recommended amount of additional capacitance, and even more is always better.

3.3 I/O Interfaces

Unless otherwise specified, all MityDSP-Pro I/O pins are compliant to 3.3V I/O standards. For the majority of DSP connected pins, this means LVTTL, however the PCI and I2C interfaces are LVCMOS33. The SRIO and RGMII interfaces use CML and HSTL standards, respectively, and therefore are not 3.3V compliant. The FPGA I/O pins are both LVTTL and LVCMOS33 compliant. The FPGA I/O pins can also be LVCMOS25 and LVDS25 compliant if a given bank VCCO is run at 2.5V. See section 2.2 and section 3.3.8, and consult the device datasheets for more information.

3.3.1 Module Reset

On the MityDSP-Pro module, the main 3.3V input supply and all on-module generated power supplies are monitored and will trigger a module hard-reset if any of them fails or goes unstable. Also included on this module is a manual-reset (MRESET#) input pin that can be connected to carrier board system reset and power supply monitoring circuitry.

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3.3.2 Emulator/JTAG

The MityDSP-Pro module includes connectivity for DSP emulation and FPGA JTAG. There is a dedicated on-module 2mm header that is intended for use with a Critical Link supplied breakout cable. Please refer to section 2.2 for specific pin-out information.

The DSP emulator connection is used for code download to RAM, and real-time debugging with TI's Code Composer Studio. The FPGA JTAG connection is used for the download of images directly into the FPGA, and for debug with tools such as Xilinx's Chipscope Pro. All on-module signals are directly connected to the DSP and FPGA pins. Connection to the emulator/JTAG pods via appropriate headers should be direct and made as short as possible, within reason.

3.3.3 McBSP Ports

The MityDSP-Pro module includes two Multi-channel Buffered Serial Ports provided by the DSP. These ports support a variety of synchronous serial communication protocols including TDM and SPI types. They can be used for connectivity to a wide array of data converters (DACs and ADCs), other DSPs, and other communications equipment. The signals are connected directly to the DSP device pins. For more information, please consult the DSP device datasheets and McBSP user guide documents provided by Texas Instruments.

3.3.4 Serial UARTs

While not directly provided by the DSP's, asynchronous serial communications (eg. RS-232, RS-422) is available on the MityDSP-Pro module. This functionality is provided as one or more soft cores in the FPGA. If a system requires the actual RS-232 or RS-422 interface signal levels, a physical layer transceiver is required to convert the FPGA's LVTTL logic levels. Commonly used transceivers include MAX3232 for +3.3V systems, and SN75C1406 for systems which already have ±12V and +5V available. However, please note that if a transceiver such as the SN75C1406 is used, series resistors (~1k ohms) are required on the UART inputs (RXD & CTS) because the MityDSP I/O's are not 5V tolerant.

The stock bootloader FPGA images for MityDSP-Pro always contain just one UART core – usually for RS-232 communication, but it could also be used for USB communications via a UART-to-USB bridge chip (discussed in the next section). The soft UART core is capable of full bi-directional data (RX & TX), and features automatic hardware flow control (RTS & CTS). The core also features the modem control lines (DTR, DSR, DCD & RI) though these are not frequently used or connected up in the FPGA top-level designs.

The MityDSP-Pro module has a set of I/O pins reserved for the one UART in the bootloader FPGA, or for end application FPGA use. It is not to say that these pins are reserved exclusively for this purpose, but in this case it is not recommended to re-use them because of the potential for contention. Table 6 below lists the standard UART pin-outs for the MityDSP-Pro module.

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Table 6: MityDSP-Pro UART Pin-out

UART Signal	Signal Direction	Main I/O Connector Pin #	FPGA Pin #
TXD	Out	14	U26
RXD	In	16	U25
RTS	Out	18	T26
CTS	In	20	T25

RS-485 interfacing is also possible with the soft UART cores. This would require an appropriate physical layer transceiver (such as SN65HVD08), plus bringing out the transmit drive-enable line (o_xmit_enb) from the soft core to an FPGA I/O pin, and tying it to the correct pin on the transceiver.

3.3.5 UART-to-USB Bridge

As mentioned in the previous section, it is possible and easy to add a low-speed USB interface to the MityDSP. This is usually accomplished using one of many UART-to-USB IC's available on the market today. These devices are easy to connect up at the board level, and also very easy to control and use on the PC end. Most manufacturers provide royalty-free virtual COM port drivers for Windows. Some even provide a more sophisticated API via DLL access for further integration into end-user PC applications. IC's commonly used by Critical Link include the CP2102 from Silicon Labs, the PL2303X from Prolific, and the VNC1L from FTDI, which actually can be used as a host device as well. Please consult the specific device datasheets and user guides for more information. When connecting these devices to the MityDSP-Pro UART pins, please pay special attention to the direction of the signals, such as the TXD/RXD and RTS/CTS pairs, as most devices (MityDSP UART included) are self-centric with respect to their signal naming conventions, and signal paths usually need to "cross-over".

3.3.6 10/100 Ethernet MAC – FPGA Core

Ethernet on the MityDSP-Pro is available as a soft MAC core in the FPGA. This Ethernet MAC is capable of full and half duplex 10/100 Mbit operation. To complete the interface, the MAC core requires a physical-layer device (PHY), an Ethernet isolation transformer (H1102 or equivalent), and an RJ-45 style connector (RJHSE-5381 or equivalent) on the carrier board. The PHY IC most commonly used by Critical Link is the National Semiconductor DP83848 family, although many other suitable ICs exist on the market today. It is also possible to connect the MAC core directly to an Ethernet Switch IC, such as the Micrel KS8995, via its standard Ethernet MII port. This option gives the carrier board the flexibility of easily making connections with several other Ethernet devices, without the need for additional networking equipment.

The stock bootloader FPGA images for all MityDSP types do not include the soft MAC core. The reason for this is that the complete MII connection to the PHY device uses 19 MityDSP I/O pins, and we did not want to reserve this many pins for one interface that may or may not be used by and end user. However, it is still possible to use the Ethernet interface for code downloads via the bootloader. All that is required is an alternate bootloader FPGA image that includes the soft MAC core with the MII port pins connected to the correct MityDSP I/O pins for a given carrier board design. Usually this is simply a copy of the end-user application FPGA image. The

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bootloader automatically detects the core and initializes the network stack for use in downloading new DSP code and FPGA images.

3.3.7 Customizable GPIO

The majority of the main interface connector pins on all MityDSP platforms are General-Purpose I/O (GPIO) pins that can be customized for any end-user purpose. This is not to say that on any given end-user application board the majority of MityDSP I/O will be fully customized. Most of the MityDSP I/O required by the majority of customer platforms actually falls into the category of "off-the-shelf" core modules already designed and tested by Critical Link. These modules include, but are not limited to: UART, Ethernet MAC, High-speed USB, I^2C controller, stepper motor controller, DACs, ADCs, LCD display, Camera-Link interfaces, and simple CPU controlled GPIO. Any desired interface that is not covered by Critical Link's library of modules can either be custom designed by Critical Link, or the end customer.

3.3.8 LVDS

On the MityDSP-Pro module, all FPGA GPIO is actually capable of LVDS communication. Pairs of I/O pins are grouped by their associated FPGA bank. Each of the four banks can be individually configured for 3.3V operation, or 2.5V operation, which is required by the Xilinx FPGA for the LVDS I/O standard. With careful I/O planning, the board designer can allocate all LVDS signal pairs to one or more FPGA banks, as required. Please note that once a bank has been configured for 2.5V operation, all I/O pins within that bank can only be used with 2.5V I/O standards, such as LVDS25 or LVCMOS25 – LVTTL or LVCMOS33 is not interoperable within a bank. Likewise, a bank configured for 3.3V operation cannot be used with the 2.5V I/O standards, LVDS25 or LVCMOS25.

LVDS communication allows for faster and more reliable communication between devices that support it. Critical Link has frequently used this feature of the MityDSP FPGA for communication with SERDES (Serializer-Deserializer) ICs for high-speed I/O expansion, LCD display connections, and for custom board-to-board communication protocols.

3.3.9 I^2C

The MityDSP-Pro module provides a dedicated I^2C interface on its main I/O connector. The interface pins are connected to the DSP's I^2C peripheral port, and also to a pair of FPGA pins. This shared wiring arrangement can allow I^2C communication between the DSP, FPGA, and any I^2C devices on the carrier board. The DSP's I^2C peripheral can act as a master or slave device, and can operate in a multi-master system. The FPGA can contain a soft I^2C controller core that currently acts only as a master device, but a slave device core could also be designed or acquired.

I^2C bus requires pull-up resistors on both of the SDA and SCL lines, however pull-up resistors have not been included on the MityDSP-Pro module. The reason for this is that an I^2C bus must be treated as a system, and only one set of pull-up resistors should exist on the bus. If the MityDSP-Pro's I^2C interface is connected with that of another subsystem that includes the pull-up resistors, then no additional pull-up resistors are required.

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Please note that the DSP and FPGA pins dedicated to this interface are 3.3V capable only. Do not pull-up the MityDSP's I^2C port pins to any voltage higher than 3.3V.

The designer of the carrier board will most likely need to add a pair of pull-up resistors to the SDA and SCL lines if this interface is going to be used. The nominal value for the resistors is 2.2k ohms each, and they should be tied to the main I/O 3.3V supply – the same one supplying current to the MityDSP-Pro module. Alternatively, it is also possible to implement the pull-up resistors in the FPGA, though this is not recommended as there is little control over the value of the pull-ups, and probably should only be attempted for communication between the DSP and FPGA only. Please consult the DSP and FPGA device datasheets and user guides for more information. Critical Link may also be contacted for more information on the available soft I^2C core.

3.3.10 10/100 Ethernet MAC – DSP Peripheral

In addition to the ability of using soft Ethernet MAC cores in the FPGA, the MityDSP-Pro module also has a dedicated Ethernet interface. This interface is powered by a high-performance Ethernet MAC built into the C645x DSP and an on-module 10/100 Mbit Ethernet PHY device. The use of this interface can free up the 19 I/O pins that would be required to use a soft Ethernet MAC core in the FPGA. Use of this dedicated interface only requires the addition of an Ethernet isolation transformer (H1102 or equivalent) and an RJ-45 style connector (RJHSE-5381 or equivalent) on the carrier board. It is often desirable to use a combined transformer and connector component (HFJ11-2450E-L12RL or equivalent), which include several of the recommended high-voltage passive components. Most Ethernet RJ-45 connectors also usually feature two LEDs for link and activity indication. The link and activity LED drive signals are routed from the PHY device to pins on the FPGA. Two more FPGA pins are reserved for routing the signals through the FPGA and out to pins on the main I/O connector (FPGA_RSV1 and FPGA_RSV2). Beginning with MDK 2.7.0, this interface is supported by the bootloader system.

3.3.11 Gigabit Ethernet

The Ethernet MAC built into the C645x DSP actually supports up to 1000 MBit (Gigabit) operation, however the on-module PHY is only capable of 10/100 Mbit operation. Operating this peripheral at Gigabit speed requires an alternate connection to an off-board Gigabit PHY device, such as the Vitesse VSC8641, and appropriate RJ-45 connector and magnetics. The MityDSP-Pro module's auxiliary I/O connector (J2) contains a set of signals dedicated to the Reduced Gigabit Media-Independent Interface (RGMII) port on the C645x DSP. These signals are listed in Table 2 as "RGxxxx". The signals are direct connects from the auxiliary I/O connector to the DSP, so please consult the DSP and PHY device datasheets for more information on making the RGMII connection.

3.3.12 Serial RapidIO

The TMS320C6455 DSP features a Serial RapidIO (SRIO) port that is capable of approximately 9 Gbps data throughput in each direction. The port consists of 4 differential pair lanes for each direction, and each lane operates at a raw data rate of 3.125 Gbps. The port signals are accessible on the MityDSP-Pro's auxiliary I/O connector (J2), and all signals are named "RIOxxx_x" – refer to Table 2 for details. Because the RapidIO interface runs at a very high speed and requires careful attention to signal integrity, it is strongly advisable to work closely with Critical Link to devise a system-level solution.

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3.3.13 PCI/HPI

The C645x DSP includes a Peripheral Component Interconnect (PCI) local bus port that is capable of communication with other PCI devices via either direct chip-to-chip, or backplane connections. The peripheral is compliant with PCI Local Bus Specification revision 2.3, and operates up to 66 MHz at 32-bits, and can act as either a master or a slave device. The port pins are routed to the MityDSP-Pro's auxiliary I/O connector (J2), and all signals are named "PCI_xxxx" – refer to Table 2 for details. For more information on this DSP peripheral, please consult the DSP datasheet and PCI User Guide.

The C645x DSP's PCI port pins are multiplexed with another peripheral port called the Host Port Interface (HPI). This interface port, which is common on many TI DSP's, is a multiplexed address/data asynchronous parallel communication bus that is intended for connection to a host processor for control and movement of data. The multiplexed port pins, which are available on the MityDSP-Pro's auxiliary I/O connector (J2), are only listed in Table 2 by their PCI names. Please refer to the DSP datasheet pin-out tables for the PCI-to-HPI pin name mapping. Also, please consult the DSP datasheet and HPI User guide for more information on this peripheral.

3.3.14 FPGA I/O Pin Power-up & Boot-up States

There are a couple of issues relating to FPGA I/O pin states on power-up and boot-up that the system and carrier board designer(s) need to be aware of. The first is that immediately upon power-up, all of the MityDSP-Pro's FPGA I/O's are configured to float, with no pull-ups or pull-downs. Once the FPGA is loaded by the bootloader system, the I/O pins are configured as designed into the FPGA's bitstream configuration data.

Next is that the standard MityDSP-Pro boot-up process includes two loads of the FPGA – one for running the bootloader, and the second for running the end-user application. What this means is that in between the two times that the FPGA is loaded, there is actually an additional state where all of the FPGA I/O pins are floating. So the full sequence is as follows:

1) Power-up
2) FPGA un-loaded with all I/O's floating
3) FPGA loaded with stock bootloader image (unused I/O's floating)
4) FPGA un-loaded with all I/O's floating
5) FPGA loaded with end-user application image

For many MityDSP-Pro based designs, this boot-up sequence is just fine. However, for some designs it may present problems with some carrier board interfaces connected to the MityDSP-Pro's FPGA pins. In these instances, it may be necessary to take measures such as adding pull-ups / pull-downs on the carrier board. If no reasonable solution can be identified, please contact Critical Link because it may be possible come up with a slightly more customized boot-up sequence and/or modification to the MityDSP-Pro module itself.

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4 Mechanical Requirements

The following sections describe some of the mechanical requirements of incorporating a MityDSP-Pro module in a board design.

4.1 Module Connectors

The MityDSP-Pro module requires as its main interface the low-profile connector socket P/N 10033853-152FSLF from FCI, which is available from Digi-Key and other vendors. Sockets which are compatible with this industry standard DDR2 memory module socket are also available from other manufacturers and vendors. The MityDSP-Pro module's auxiliary I/O connector (J2) mates with P/N FX8-100P-SV from Hirose. If the auxiliary connector is not used for its advanced interface connections, it is still recommended to be included for extra grounding via its GND pins. It is also recommended for the additional mechanical attachment it provides, as discussed in section 4.3, below. Figure 2 illustrates the relative positioning of the two MityDSP-Pro connectors.

The MityDSP-Pro module may also be able to use a higher-profile connector socket that is mechanically compatible, but not necessarily footprint compatible with the connector mentioned above. Please contact Critical Link for a current list of compatible connector sockets for the MityDSP-Pro module.

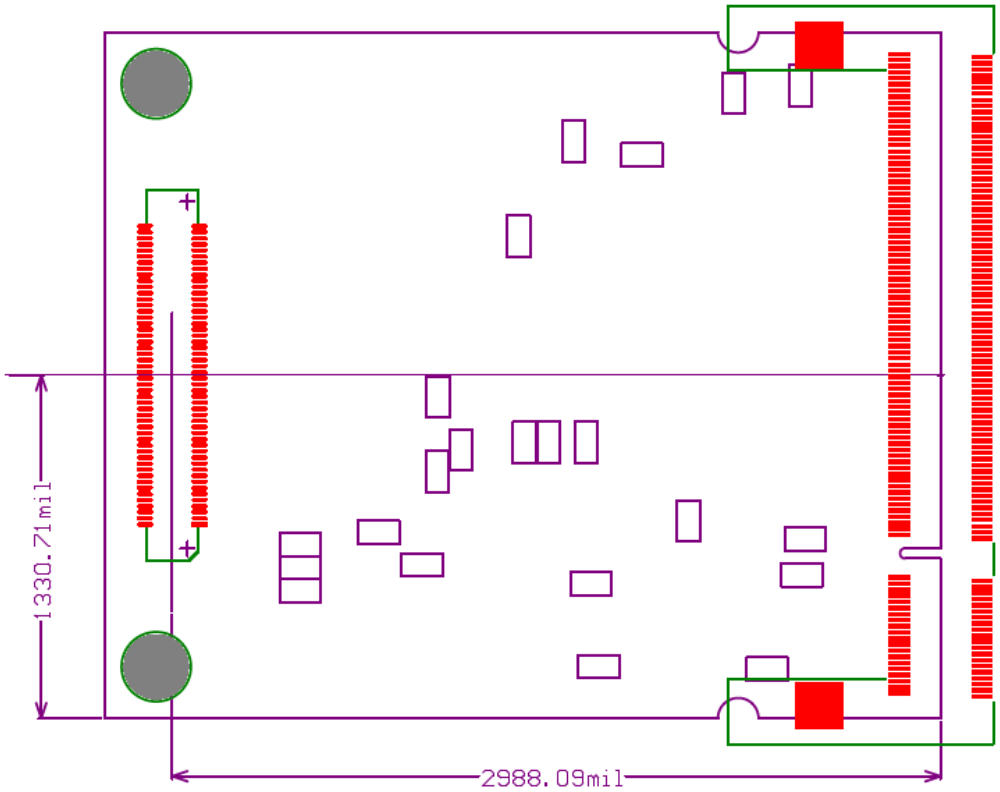

Figure 2: Mating Connector Relative Positioning

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4.2 Module Clearance

The MityDSP-Pro module types use a SO-DIMM style main interface connector for electrical and mechanical attachment to the carrier board. This style of connector positions the MityDSP-Pro module in parallel with the carrier board, and as such there is limited clearance between the MityDSP-Pro module and the carrier board. Therefore it is impossible to place high-profile carrier board components underneath the MityDSP-Pro module. However, it is possible to utilize most of this space for low-profile components. Please refer to the following diagrams and tables for module-specific clearances.

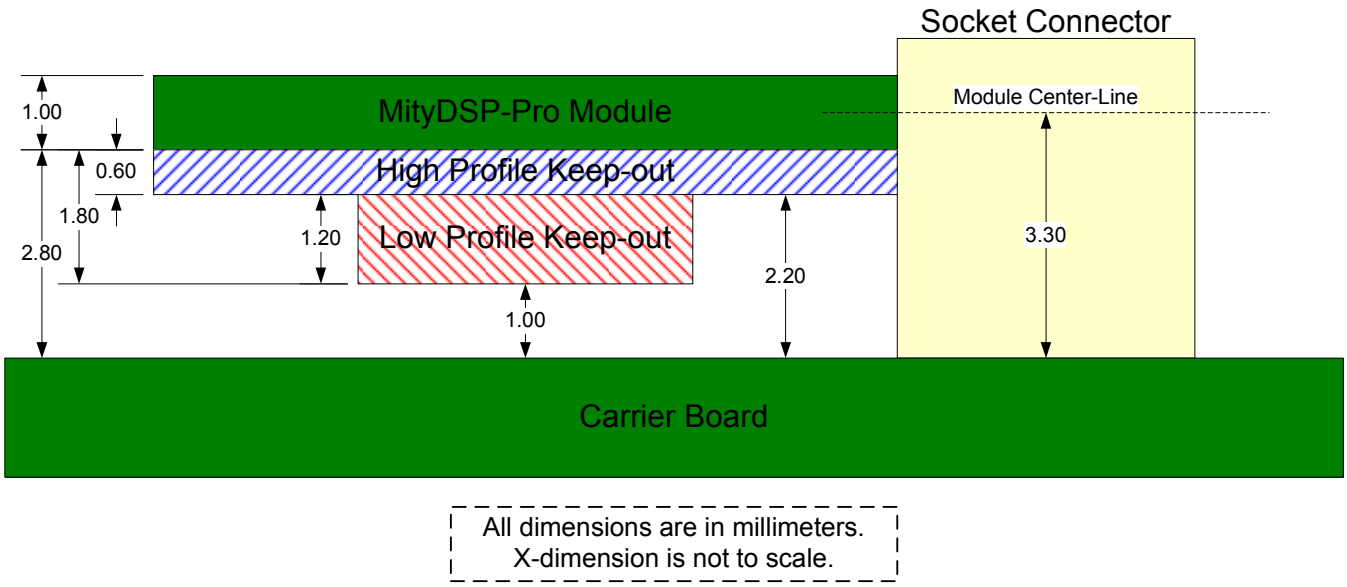

Figure 3: MityDSP-Pro Module Clearance - Side View

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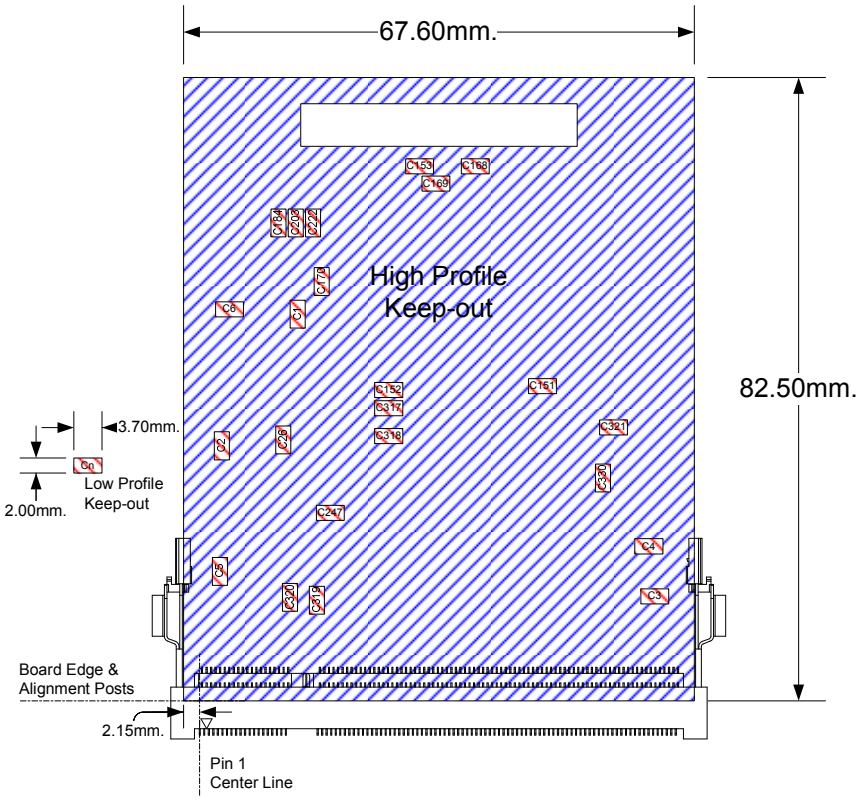

Figure 4: MityDSP-Pro Keep-outs

Table 7: MityDSP-Pro Low Profile Keep-out Centroids

Centroids:	From Pin-1 CL and lower-edge	
Component	X (mm)	Y (mm)
C1	12.96	51.18
C2	2.93	33.78
C3	60.21	13.84
C4	59.45	20.45
C5	2.68	17.15
C6	3.95	51.82
C26	11.06	34.54
C151	45.35	41.66
C152	25.03	41.15
C153	29.09	70.74
C168	36.46	70.74
C169	31.25	68.45
C170	16.14	55.50
C184	10.42	63.25
C203	12.71	63.25
C222	15.00	63.25
C247	17.28	24.89

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Centroids:	From Pin-1 CL and lower-edge	
Component	X (mm)	Y (mm)
C317	25.03	38.74
C318	25.03	35.05
C319	15.50	13.34
C320	11.95	13.72
C321	54.75	36.20
C330	53.35	29.52

4.3 Mounting Methods

The MityDSP-Pro module features two additional optional mechanical attachment methods. The first is the module's auxiliary I/O connector (see section 4.1), which is located on the bottom side at the free end of the module as it sits in the main I/O socket. This connector provides friction locking and additional mechanical support for the long-extending MityDSP-Pro module. The second method is hard mechanical attachment by board-to-board standoffs and screw hardware. The corners of the free-floating edge of the MityDSP-Pro feature mounting holes that are compatible with 4-40 size mounting hardware. The mechanical drawing Figure 5below illustrates the mechanical requirements of these optional attachment methods.

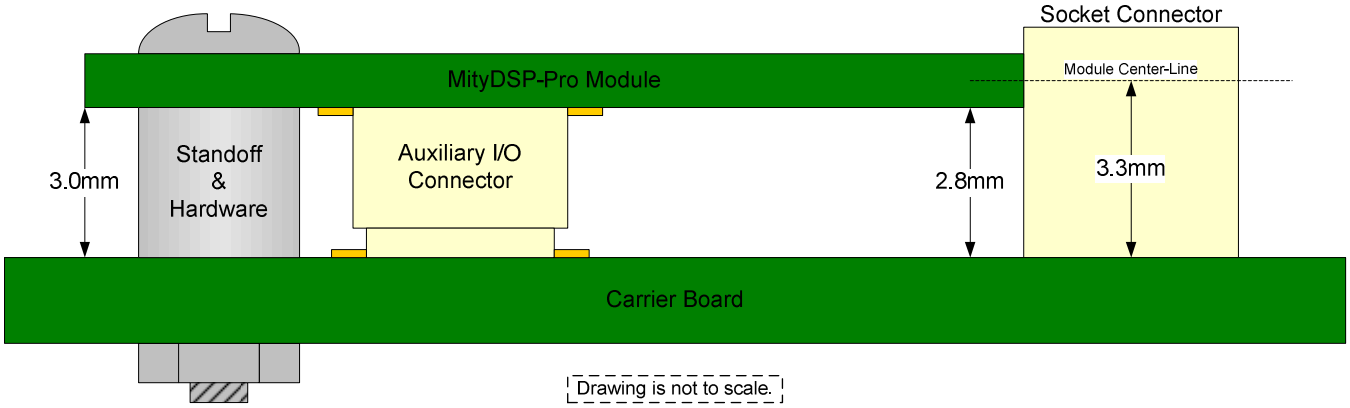

Figure 5: MityDSP-Pro Optional Attachment Drawing

4.4 Shock & Vibration

For customers who are interested in using MityDSP modules in rugged environments, the optional mechanical attachment methods discussed in section 4.3 above enable MityDSP modules to tolerate much greater mechanical shock and vibration forces than without any additional mounting support.

4.5 Thermal Management

The MityDSP-Pro module does require some amount of thermal management even at room temperatures. The primary concern is with the DSP device, which does generate quite a bit of heat, even when idle. Of course more processing activity will mean more power draw and more heat dissipation. Critical Link has operated the MityDSP-Pro module without heat sinking or air flow on bench tops at room temperatures for long periods of

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time without failure. However, using the module inside an enclosure is cause for concern, as the heat will most likely build up inside and eventually cause the DSP or other components to malfunction. Existing customers have successfully used small fans to move air across the surface of the MityDSP-Pro module to keep the DSP temperature within operating range. However, every end product is different, and it is advisable to do plenty of testing to ensure that the product will meet desired performance specifications.

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5 Board Layout Recommendations

The following sections discuss topics for successful board layouts incorporating the MityDSP-Pro module.

5.1 Placement

Placement of the MityDSP-Pro module site is crucial to a successful carrier board layout. Because the module connector footprint is fine-pitch and dual-row, it is generally best to place the connector fairly centered in the overall board layout. This placement allows traces to be routed out from both sides of the connector, using mainly top-side copper tracks. The use of less signal layers, and therefore less vias, generally results in a more compact design with better signal integrity than a board using many layers and vias. Of course, ideally central placement is not always possible because of other mechanical constraints.

Mechanically, enough space must be allocated for the full extension of the MityDSP-Pro module. Although it is possible for a MityDSP-Pro module to hang over the edge of its carrier board, this may not be desirable if additional mechanical attachment methods are desired for ruggedness, as discussed in sections 4.3 and 4.4. Another thing to keep in mind with placement on the carrier board and in enclosures is the cam-in action of the MityDSP-Pro module into its socket. The module is generally installed at an angle of about 25° to 30° before swinging down to locked position. Enclosure designs should accommodate this motion, keeping in mind that the MityDSP-Pro module is long and travels quite a large distance at the free-floating edge.

5.2 Pin-out and Routing

Because the MityDSP-Pro module pins are mostly configurable FPGA I/O, board level pin-out and routing is greatly simplified. This is done by taking advantage of the FPGA tools' sophisticated signal routing capabilities, instead of creating a tangled mess of tracks and vias in copper. MityDSP-Pro pin allocation in the schematic is generally best done in tandem with PCB layout. In this method, the components are first captured in schematic, but not yet connected to the MityDSP-Pro's configurable FPGA I/O pins, except for the dedicated functionality pins. Then in PCB layout, parts are placed according to mechanical and positional requirements with components needing connection to the MityDSP-Pro placed nearby the MityDSP-Pro's socket connector. At this point it becomes much easier to see which MityDSP-Pro pins are ideal for allocation for the various required functions. The designer can then go back and forth between schematic and layout to complete the connections between IC's and the MityDSP-Pro connector. Some PCB design tools make this process even easier with abilities to automatically re-assign nets to pins that would otherwise require many crossovers in copper features to complete. Once the signals are assigned to pins on the MityDSP-Pro, this information can be given to the FPGA designer who will capture the pin-out in a User Constraints File (UCF) for input into the FPGA's place and route tools.

5.3 Access issues

Given that it is possible and often desirable to make best use of available space by placing components underneath the MityDSP-Pro module (refer to section 0), hardware and software engineers who will be

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debugging code on the platform could find themselves in a tough situation if the component they need to access is blocked by the installed MityDSP-Pro module. Because of these situations it is advisable to either not use the space under the MityDSP-Pro module for active components that might need live probing with the MityDSP-Pro in-circuit, or only place circuits there that are already tried and tested by engineers on other platforms. In the event that an obscured circuit does need to be probed, it may be necessary to solder temporary wires onto probe points. An even better solution would be to design the board with bottom-side test points, at least in the MityDSP-Pro region, if this is possible on a given design.

5.4 PCB/PCA Technology

The MityDSP-Pro module does not have any specific requirements about the PCB technology used for its carrier board. The required socket connectors are available as RoHS compliant, and may be used in both leaded and lead-free assembly processes. The only recommendation is to fabricate the carrier board thick enough to rigidly support the MityDSP-Pro socket connector. In practice, FR-4 with a common finished thickness of 0.062 inches is enough for all types of MityDSP modules.

5.5 PCB Footprints

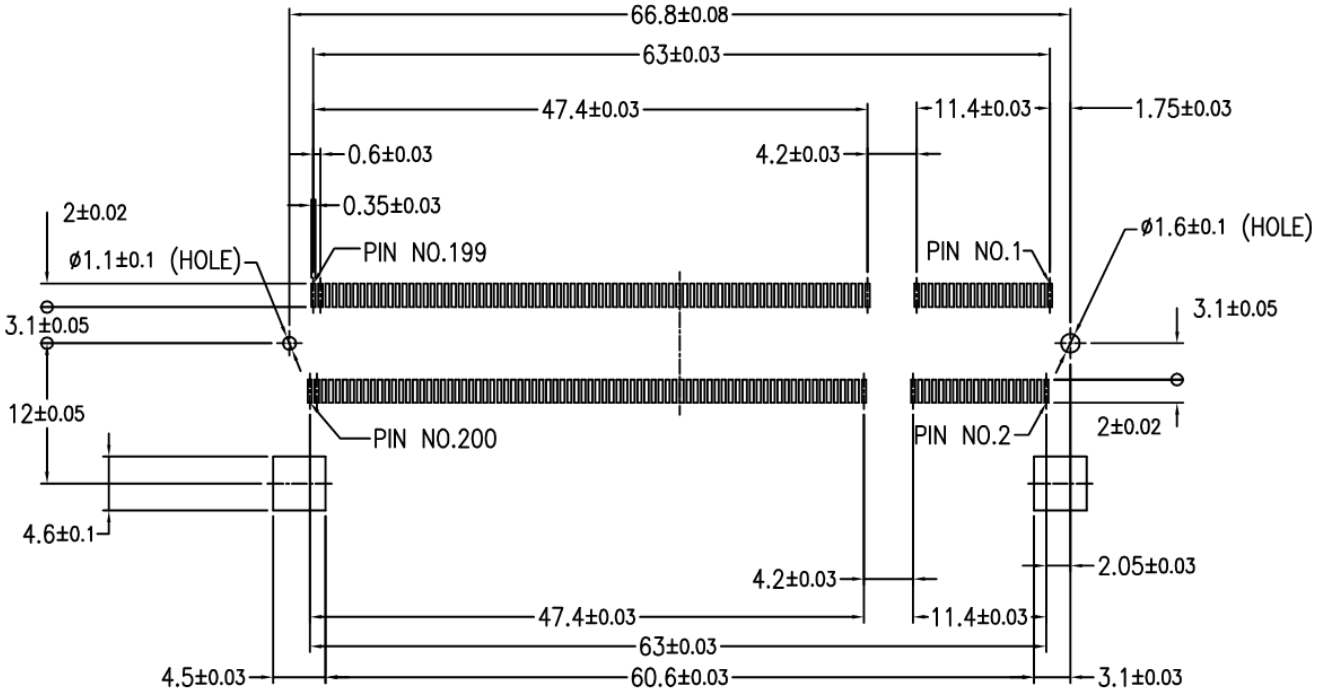

Figure 6: FCI 10033853-152FSLF Recommended PCB Footprint

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REVISION HISTORY

Date	Change Description
23-OCT-2009	Initial Release
27-OCT-2011	Add mechanical drawing showing relative positioning of mating connectors

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