MityDSP™ Document

Document: MityDSP™ Carrier Board Design Guide

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1 Overview

1.1 Fast Facts for Getting Started

Facts	MityDSP & MityDSP-XM
Required socket connector	AMP: 390111-1
Voltages required	3.3V, 2.5V, 1.23V
Supported I/O standards	LVTTL, LVCMOS33, LVCMOS25, LVDS25
Total number of FPGA I/O's	98 General Purpose
Number of LVDS capable I/O's	20 (10 pairs)

1.2 Introduction

MityDSP modules are designed to be easy to integrate into an end-user embedded system. The modules integrate many crucial elements of an embedded DSP system, and do so with an established design framework utilizing a common set of core libraries. End-user design of the application PCB is also intended to be as simple as possible, allowing the PCB designer to concentrate on the custom I/O interfaces – especially analog & mixed-signal – instead of getting distracted with the learning curve of designing a brand new embedded digital system from scratch.

1.3 MityDSP™ Modules

There are three main types of MityDSP modules. The original MityDSP module is based on a Texas Instruments TMS320C6711 DSP, includes SDRAM and Flash memories, and is interfaced by a 144-pin SO-DIMM card-edge connector. The module also integrates a Xilinx Spartan3 FPGA for implementing required on-board logic, and also for end-user customizable logic and I/O interfaces. Also available in the same footprint is the MityDSP-XM, which includes more memory and a larger FPGA than the original module. Carrier board design for these two types of MityDSP is the main focus of this document.

A more powerful module, the MityDSP-Pro is based on a Texas Instruments TMS320C645x DSP, includes DDR2 SDRAM and Flash memories, and is interfaced by a 200-pin SO-DIMM card-edge connector and a 100-pin high-density, low-profile Hirose connector. The module integrates a large Xilinx Spartan3 FPGA for implementing required on-board logic and I/O interfaces, and also for end-user customizable logic and I/O interfaces. The

module also incorporates a number of powerful features not available on the original MityDSP platform. These include: PCI/HPI, Serial RapidIO (C6455 only), and Gigabit Ethernet interfaces provided by the DSP; DDR SDRAM dedicated to the FPGA; all external FPGA I/O is LVDS capable; and all core power regulation is done on-board.

All types of MityDSP are available with options for speed grade, memory size, FPGA size, operating temperature ranges, and RoHS / non-RoHS compliance. Please contact Critical Link for the current list of MityDSP variants.

1.4 Module Dimensions

The MityDSP module is compact! The module footprint is less than 60% of the area of a standard business card (not including edge connector). A dimensioned drawing of the MityDSP / MityDSP-XM module is included below in Figure 1.

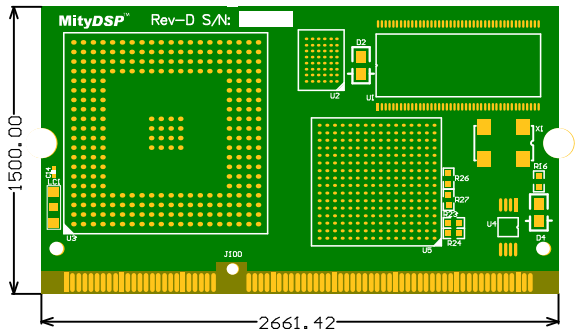

Figure 1: MityDSP & MityDSP-XM Mechanical Drawing

2 Connectors

All types of MityDSP utilize SO-DIMM style edge-connectors for main connectivity with the end user application PCB. These connectors were chosen for their high density, compact size, ease of procurement, and low cost. With edge connectors, a physical socket component is only required on one side – the main PCB side. The SO-DIMM standard also allows the MityDSP module to lay flat, in parallel with the main PCB, as they were intended for use by memory modules in compact equipment, such as laptops.

2.1 Card-edge compatibility

The original MityDSP and MityDSP-XM modules are designed to plug into a 144-pin SO-DIMM SGRAM socket. These sockets were once used for memory upgradability on PC video systems. Because they are no longer commonly used for this purpose, it was thought to be a good choice for the MityDSP because it would lessen the chance that someone would attempt to plug a MityDSP into an SGRAM socket, or plug an SGRAM module into a MityDSP socket. Please note that the MityDSP is NOT electrically compatible with the SGRAM socket standard, and intermixing modules/sockets from the two standards would very possibly cause permanent damage to one or both sides.

2.2 MityDSP & MityDSP-XM Module Pin-out

Table 1: MityDSP & MityDSP-XM Card-edge (J100) Pin-out

Pin #	Alt. Pin # [1]	Signal	FPGA Bank	Pin #	Alt. Pin #	Signal	FPGA Bank
1	A1	+3.3V (I/O)	-	2	B1	+3.3V (I/O)	-
3	A2	GND	-	4	B2	GND	-
5	A3	DSP_TMS	-	6	B3	MRESET#	-
7	A4	DSP_TDO	-	8	B4	DSP_TRST	-
9	A5	DSP_TDI	-	10	B5	DSP_EMU1	-
11	A6	DSP_TCK	-	12	B6	DSP_EMU0	-
13	A7	CLKS0	-	14	B7	CLKS1	-
15	A8	CLKR0	-	16	B8	CLKR1	-
17	A9	CLKX0	-	18	B9	CLKX1	-
19	A10	DR0	-	20	B10	DR1	-
21	A11	DX0	-	22	B11	DX1	-
23	A12	FSR0	-	24	B12	FSR1	-

[1] Alternate Pin # refers to a pin-numbering scheme used by Critical Link in most of its MityDSP/-XM carrier board designs, where the pin numbers are prefixed by A or B, which denotes the Top (A) and Bottom (B) rows, of gold fingers on the module itself. The more standard pin-numbering scheme for these types of connectors, according to manufacturer datasheets, is to number the pins in an odd/even fashion, where odds would connect to top-side gold fingers, and evens would connect to bottom-side gold fingers.

Pin #	Alt. Pin # [1]	Signal	FPGA Bank	Pin #	Alt. Pin #	Signal	FPGA Bank
25	A13	FSX0	-	26	B13	FSX1	-
27	A14	GND	-	28	B14	GND	-
29	A15	+1.23V (core)	-	30	B15	+1.23V (core)	-
31	A16	RESET#	-	32	B16	CLKOUT2	-
33	A17	RESET	-	34	B17	CLKOUT3	-
35	A18	GND	-	36	B18	GND	-
37	A19	FPGA_TCK	-	38	B19	FPGA_TDO	-
39	A20	FPGA_TDI	-	40	B20	FPGA_TMS	-
41	A21	IO_L13	3	42	B21	IO_K14 / UART1_TXD	3
43	A22	IO_H16	2	44	B22	IO_L12 / UART1_RXD	3
45	A23	IO_K13	3	46	B23	IO_J14 / UART1_RTS	3
47	A24	IO_H15	2	48	B24	IO_G16 / UART1_CTS	2
49	A25	IO_J13	3	50	B25	IO_H14 / UART2_TXD	2
Mechanical Key Gap							
51	A26	IO_G15	2	52	B26	IO_K12 / UART2_RXD	3
53	A27	IO_E16	2	54	B27	IO_F15 / UART2_RTS	2
55	A28	IO_G14	2	56	B28	IO_H13 / UART2_CTS	2
57	A29	IO_D16	2	58	B29	IO_E15	2
59	A30	IO_F14	2	60	B30	IO_C16	2
61	A31	IO_G13	2	62	B31	IO_D15	2
63	A32	IO_B16	2	64	B32	IO_E14	2
65	A33	IO_C15	2	66	B33	IO_F13	2
67	A34	IO_D14	2	68	B34	IO_G12	2
69	A35	IO_F12	2	70	B35	IO_E13	2
71	A36	IO_B14	1	72	B36	IO_A14	1
73	A37	IO_B13	1	74	B37	IO_D12	1
75	A38	IO_A13	1	76	B38	IO_C12	1
77	A39	IO_E11	1	78	B39	IO_B12	1
79	A40	IO_A12	1	80	B40	IO_D11	1
81	A41	IO_C11	1	82	B41	IO_B11	1
83	A42	IO_D9	1	84	B42	IO_E10	1
85	A43	IO_C9	1	86	B43	IO_D10	1
87	A44	IO_B8	0	88	B44	IO_A10	1
89	A45	IO_A8	0	90	B45	IO_B10	1
91	A46	IO_C10	1	92	B46	IO_A9	1
93	A47	IO_D8	0	94	B47	IO_C8	0
95	A48	IO_P7	5	96	B48	IO_B7	0
97	A49	IO_A7	0	98	B49	IO_C7	0
99	A50	IO_D7	0	100	B50	IO_E7	0
101	A51	IO_M7	5	102	B51	IO_P6	5

Pin #	Alt. Pin # [1]	Signal	FPGA Bank	Pin #	Alt. Pin #	Signal	FPGA Bank
103	A52	IO_B6	0	104	B52	IO_C6	0
105	A53	IO_D6	0	106	B53	IO_A5	0
107	A54	IO_E6	0	108	B54	IO_B5	0
109	A55	IO_C5	0	110	B55	IO_A4	0
111	A56	IO_D5	0	112	B56	IO_B4	0
113	A57	IO_A3	0	114	B57	IO_N7	5
115	A58	IO_J4	6	116	B58	IO_M14	3
117	A59	IO_K5	6	118	B59	IO_M10	4
119	A60	GND	-	120	B60	GND	-
121	A61	IO_L2P_E4	7	122	B61	IO_L4P_F5	7
123	A62	IO_L2N_F4	7	124	B62	IO_L4N_G5	7
125	A63	IO_L3P_F3	7	126	B63	IO_L8P_D3	7
127	A64	IO_L3N_F2	7	128	B64	IO_L8N_E3	7
129	A65	IO_L5P_G4	7	130	B65	IO_L7P_C3	7
131	A66	IO_L5N_G3	7	132	B66	IO_L7N_C2	7
133	A67	IO_L6P_H4	7	134	B67	IO_L0P_D2	7
135	A68	IO_L6N_H3	7	136	B68	IO_L0N_D1	7
137	A69	IO_L9P_G1	7	138	B69	IO_L1P_E2	7
139	A70	IO_L9N_H1	7	140	B70	IO_L1N_E1	7
141	A71	GND	-	142	B71	GND	-
143	A72	+2.5V (FPGA)	-	144	B72	+2.5V (FPGA)	-

Table 2: MityDSP & MityDSP-XM Signal Group Description

Signal / Group	Type	Description
+3.3V	PWR	3.3 volt input power referenced to GND. Power for I/O interfaces.
+2.5V	PWR	2.5 volt input power referenced to GND. Power for FPGA use.
+1.23V	PWR	1.23 volt input power referenced to GND. Power for DSP & FPGA cores.
MRESET#	I	Manual reset input. Pulled-up on the MityDSP/XM module. When driven to GND for a minimum of 1 us, a module-wide reset is triggered. Can be tied into system system-wide reset and power monitoring circuitry.
DSP_TMS, DSP_TDO DSP_TDI, DSP_TCK DSP_EMU0, DSP_EMU1 DSP_TRST	I/O	These pins are directly connected to the JTAG emulator port on the TMS320C6711 DSP.
FPGA_TMS, FPGA_TDI FPGA_TDO, FPGA_TCK	I/O	These pins are directly connected to the JTAG programming port on the Xilinx Spartan3 FPGA device.
CLKS0 / 1 CLKR0 / 1 CLKX0 / 1 DR0 / 1 DX0 / 1 FSR0 / 1 FSX0 / 1	I/O	These pins are directly connected to the corresponding McBSP port-0 / port-1 pins on the TMS320C6711 DSP. Please refer to the DSP datasheet and McBSP User Guide for more information.
RESET#, RESET	O	Reset output signals (active-low and active-high pair) from the on-board reset monitor circuit. These signals may be used to initiate reset circuitry on MityDSP carrier cards.
CLKOUT2	O	Connected directly to DSP's CLKOUT2 pin. Consult DSP device datasheet for further details on operation. Also connected directly to a spare FPGA pin with GCLK capability.
CLKOUT3	O	Connected directly to DSP's CLKOUT3 pin. Consult DSP device datasheet for further details on operation.
GND	PWR	System Digital Ground.
IO_XX	I/O	FPGA I/O pins. These pins are routed to FPGA pins XX. These pins all provide 3.3V bank logic and are available for application use.
IO_LnP_XX, IO_LnN_XX	I/O	FPGA I/O pins. These pins are routed to FPGA pins XX. By default, these pins are configured for 3.3V logic. However, they can also be configured for 2.5V logic, and optionally be run as LVDS pairs according to the P/N (positive/negative) letters in the net names.

3 Electrical Requirements

The following sections describe the various electrical requirements for the MityDSP and MityDSP-XM modules.

3.1 Power Supplies

The MityDSP and MityDSP-XM modules require regulated power supplies for both the I/O and core power rails. These are +3.3V for main I/O, +2.5V for FPGA I/O, and +1.23V for DSP and FPGA core power. The power supplies can be either linear or switching type. Linear supplies should be able to respond quickly to changes in current load. Switching supplies should adhere to the ripple voltage specification. Table 3 describes the specifications of the input voltage, allowed ripple, and current requirements.

Table 3: Module Voltage and Current Specifications

Module	Spec.	Minimum	Typical	Maximum	Units
MityDSP	$V_{1.23}$	1.2	1.23	1.25	V
	$I_{1.23}$	220	250	600	mA
	$V_{2.5}$	2.38	2.5	2.63	V
	$I_{2.5}$	28	30	45	mA
	$V_{3.3}$	3.14	3.3	3.46	V
	$I_{3.3}$	66	75	300	mA
MityDSP-XM	$V_{1.23}$	1.2	1.23	1.25	V
	$I_{1.23}$	270	300	700	mA
	$V_{2.5}$	2.38	2.5	2.63	V
	$I_{2.5}$	50	50	75	mA
	$V_{3.3}$	3.14	3.3	3.46	V
	$I_{3.3}$	55	75	300	mA

Current MityDSP and MityDSP-XM modules do not have any specific requirement for sequencing of the three power supply rails. However, it is usually a good idea to power up all three rails at nearly the same time so that no one rail is powered for an extended period of time, while another rail is still unpowered. The basis of this recommendation comes from the recommendations given in the datasheets of the two main components, the DSP and the FPGA.

For more information on this topic, please consult the DSP datasheet (TI document # SPRS292B, page 57) and the FPGA datasheet (Xilinx document # DS099 v2.4, page 52). The Xilinx datasheet, along with device errata sheets, indicate that older revision of the devices did have some power supply sequencing issues, but these are no longer a problem with current devices, which are used on current versions of the MityDSP & MityDSP-XM modules.

3.2 Recommended Capacitance

All MityDSP modules include some power supply rail bypass capacitors on-board, however additional capacitance is recommended on the carrier board to minimize the ripple effect caused by changing load currents. It is common practice to place one 10uF tantalum capacitor nearby each power supply pin pair. On the MityDSP and MityDSP-XM modules there is one pair of pins per power rail, so three capacitors are required. Please note that this is the minimum recommended amount of additional capacitance, and even more is always better.

3.3 I/O Interfaces

All MityDSP I/O pins are compliant to only 3.3V I/O standards. For DSP connected pins, this means LVTTL only. For the FPGA I/O pins, this means either LVTTL or LVCMOS33. The only exception to this rule is for FPGA bank 7, which can be switched over to 2.5V I/O standards. See section 3.3.8 for more details.

The following sections describe I/O interfaces that are found on all current MityDSP types.

3.3.1 Module Reset

All modules include an on-board power supply monitor and timed reset circuit. On the MityDSP and MityDSP-XM modules, this circuit monitors only the 3.3V supply. The assumption is that on the carrier board, all three required power supplies are sourced by a single system-level power supply, such as +5V. In this scenario, if the 3.3V supply was collapsing because of overload or a short, the 2.5V and 1.23V supplies would probably be collapsing soon, and the whole module should be held in reset. Also, the module cannot function properly without a stable 3.3V I/O supply, even if the other two supplies are good. The only scenario the on-module supply monitor does not cover is if somehow the 3.3V supply is good, but one or both of the other two are unstable or collapsed. To completely cover these types of cases, the modules have a manual-reset (MRESET#) input pin that can be connected to carrier board system reset and power supply monitoring circuitry. It is common practice to connect this pin to the power-good (PG) pins of all the individual power supplies on the carrier board. Voltage regulators commonly used by Critical Link that have this PG pin feature are the Texas Instruments TPS54110 synchronous-buck switcher and the TPS76801 fast-transient-response LDO.

3.3.2 Emulator/JTAG

All modules include connectivity for DSP emulation and FPGA JTAG. On the MityDSP and MityDSP-XM modules, the connection is made via the main I/O interface connector. Please refer to section 2.2 for specific module pin-out information.

The DSP emulator connection is used for code download to RAM, and real-time debugging with TI's Code Composer Studio. The FPGA JTAG connection is used for the download of images directly into the FPGA, and for debug with tools such as Xilinx's Chipscope Pro. All on-module signals are directly connected to the DSP and FPGA pins. Connection to the emulator/JTAG pods via appropriate headers should be direct and made as short as possible, within reason.

3.3.3 McBSP Ports

All modules include two Multi-channel Buffered Serial Ports provided by the DSP. These ports support a variety of synchronous serial communication protocols including TDM and SPI types. They can be used for connectivity to a wide array of data converters (DACs and ADCs), other DSPs, and other communications equipment. The signals are connected directly to the DSP device pins. For more information, please consult the DSP device datasheets and McBSP user guide documents provided by Texas Instruments.

3.3.4 Serial UARTs

While not directly provided by the DSP, asynchronous serial communications (eg. RS-232, RS-422) is available on all MityDSP modules. This functionality is provided as one or more soft cores in the FPGA. If a system requires the actual RS-232 or RS-422 interface signal levels, a physical layer transceiver is required to convert the FPGA's LVTTL logic levels. Commonly used transceivers include MAX3232 for +3.3V systems, and SN75C1406 for systems which already have ±12V and +5V available. However, please note that if a transceiver such as the SN75C1406 is used, series resistors (~1k ohms) are required on the UART inputs (RXD & CTS) because the MityDSP I/O's are not 5V tolerant.

The stock bootloader FPGA images for MityDSP and MityDSP-XM always contain two UART cores – one for RS-232 communication, and one for USB communication via a UART-to-USB bridge chip (discussed in the next section). The second channel can also be used for RS-422 type interfaces, or just another RS-232 interface.

The soft UART core is capable of full bi-directional data (RX & TX), and features automatic hardware flow control (RTS & CTS). The core also features the modem control lines (DTR, DSR, DCD & RI) though these are not frequently used or connected up in the FPGA top-level designs.

The two UARTs in the stock bootloader FPGA for MityDSP and MityDSP-XM are pinned out to a standard set of MityDSP I/O pins. While not exactly reserved exclusively for this purpose, these pins are very commonly used for the same purpose in end-user applications because most users will want or need to use the UART(s) for code download via the bootloader anyway. It is also fairly common practice to only use one of the UART interfaces for serial connectivity, and re-use the other UART's pins as another function in the end-user application FPGA. However, if this is desired, then it is usually a good idea to match input and output signal directions with the UART pin-out so that contention with other carrier board circuitry does not occur. Please contact Critical Link for more information on sharing these pins.

Table 4: Standard UART Pin-outs

MityDSP Type	UART #	UART Signal	Signal Direction	Main I/O Connector Pin #	FPGA Pin #
MityDSP & MityDSP-XM	1	TXD	Out	B21	K14
		RXD	In	B22	L12
		RTS	Out	B23	J14
		CTS	In	B24	G16
	2	TXD	Out	B25	H14
		RXD	In	B26	K12
		RTS	Out	B27	F15
		CTS	In	B28	H13

RS-485 interfacing is also possible with the soft UART cores. This would require an appropriate physical layer transceiver (such as SN65HVD08), plus bringing out the transmit drive-enable line (o_xmit_enb) from the soft core to an FPGA I/O pin, and tying it to the correct pin on the transceiver.

3.3.5 UART-to-USB Bridge

As mentioned in the previous section, it is possible and easy to add a low-speed USB interface to the MityDSP. This is usually accomplished using one of many UART-to-USB IC's available on the market today. These devices are easy to connect up at the board level, and also very easy to control and use on the PC end. Most manufacturers provide royalty-free virtual COM port drivers for Windows. Some even provide a more sophisticated API via DLL access for further integration into end-user PC applications. IC's commonly used by Critical Link include the CP2102 from Silicon Labs, the PL2303X from Prolific, and the VNC1L from FTDI, which actually can be used as a host device as well. Please consult the specific device datasheets and user guides for more information. When connecting these devices to the MityDSP UART pins, please pay special attention to the direction of the signals, such as the TXD/RXD and RTS/CTS pairs, as most devices (MityDSP UART included) are self-centric with respect to their signal naming conventions, and signal paths usually need to "cross-over".

3.3.6 10/100 Ethernet

Ethernet on the MityDSP is available as a soft MAC core in the FPGA. This Ethernet MAC is capable of full and half duplex 10/100 Mbit operation. To complete the interface, the MAC core requires a physical-layer device (PHY), an Ethernet isolation transformer (H1102 or equivalent), and an RJ-45 style connector (RJHSE-5381 or equivalent) on the carrier board. The PHY IC most commonly used by Critical Link is the National Semiconductor DP83848 family, although many other suitable ICs exist on the market today. It is also possible to connect the MAC core directly to an Ethernet Switch IC, such as the Micrel KS8995, via its standard Ethernet MII port. This option gives the carrier board the flexibility of easily making connections with several other Ethernet devices, without the need for additional networking equipment.

The stock bootloader FPGA images for all MityDSP types do not include the soft MAC core. The reason for this is that the complete MII connection to the PHY device uses 19 MityDSP I/O pins, and we did not want to reserve this many pins for one interface that may or may not be used by and end user. However, it is still possible to use the Ethernet interface for code downloads via the bootloader. All that is required is an alternate bootloader

FPGA image that includes the soft MAC core with the MII port pins connected to the correct MityDSP I/O pins for a given carrier board design. Usually this is simply a copy of the end-user application FPGA image. The bootloader automatically detects the core and initializes the network stack for use in downloading new DSP code and FPGA images.

3.3.7 Customizable GPIO

The majority of the main interface connector pins on all MityDSP platforms are General-Purpose I/O (GPIO) pins that can be customized for any end-user purpose. This is not to say that on any given end-user application board the majority of MityDSP I/O will be fully customized. Most of the MityDSP I/O required by the majority of customer platforms actually falls into the category of "off-the-shelf" core modules already designed and tested by Critical Link. These modules include, but are not limited to: UART, Ethernet MAC, High-speed USB, I^2C controller, stepper motor controller, DACs, ADCs, LCD display, Camera-Link interfaces, and simple CPU controlled GPIO. Any desired interface that is not covered by Critical Link's library of modules can either be custom designed by Critical Link, or the end customer.

3.3.8 LVDS

A portion of MityDSP and MityDSP-XM I/O pins are capable of Low-Voltage-Differential-Signaling (LVDS). These pins are and grouped into a single I/O bank on the FPGA, and routed in differential pairs. This allows the one bank to be switched over from the 3.3V power rail to the 2.5V power rail, as it is required by the FPGA. The switch is made by moving a single 0603 size zero-ohm resistor from one set of pads to another on the MityDSP module itself. Once the switch is made, the I/O bank can only then be used for LVDS25 or LVCMOS25 I/O standards. If the end customer is uncomfortable with making this switch themselves, it is possible to order MityDSP modules with the LVDS option already enabled. Please contact Critical Link for the current list of orderable MityDSP variants.

LVDS communication allows for faster and more reliable communication between devices that support it. Critical Link has frequently used this feature of the MityDSP FPGA for communication with SERDES (Serializer-Deserializer) ICs for high-speed I/O expansion, LCD display connections, and for custom board-to-board communication protocols.

3.3.9 FPGA I/O Pin Power-up & Boot-up States

There are a couple of issues relating to FPGA I/O pin states on power-up and boot-up that the system and carrier board designer(s) need to be aware of. The first is that immediately upon power-up, all of the MityDSP's FPGA I/O's are configured as pull-ups with a resistance that varies with bank voltage. For 3.3V I/O's, the resistance is between 1.27kΩ and 4.11kΩ. For 2.5V I/O's (Bank 7 only – see section 3.3.8 above), the resistance is between 1.15kΩ and 3.25kΩ. Once the FPGA is loaded by the bootloader system, the I/O pins are configured as designed into the FPGA's bitstream configuration data.

Next is that the standard MityDSP boot-up process includes two loads of the FPGA – one for running the bootloader, and the second for running the end-user application. What this means is that in between the two times that the FPGA is loaded, there is actually an additional state where the FPGA I/O pins are pulled-up. So the full sequence is as follows:

1) Power-up
2) FPGA un-loaded with all I/O's pulled up
3) FPGA loaded with stock bootloader image (unused I/O's floating)
4) FPGA un-loaded with all I/O's pulled up
5) FPGA loaded with end-user application image

For many MityDSP based designs, this boot-up sequence is just fine. However, for some designs it may present problems with some carrier board interfaces connected to the MityDSP's FPGA pins. In these instances, it may be necessary to take measures such as using inverted logic and adding pull-ups / pull-downs on the carrier board. If no reasonable solution can be identified, please contact Critical Link because it may be possible come up with a slightly more customized boot-up sequence and/or modification to the MityDSP module itself.

4 Mechanical Requirements

The following sections describe some of the mechanical requirements of incorporating a MityDSP module in a board design.

4.1 Module Connectors

The MityDSP and MityDSP-XM modules require the low-profile connector socket P/N 390111-1 from AMP/Tyco Electronics, which is available from Digi-Key and other vendors. A high-profile connector socket may also be available in limited quantities – contact Critical Link for more details.

4.2 Module Clearance

All MityDSP module types use a SO-DIMM style main interface connector for electrical and mechanical attachment to the carrier board. This style of connector positions the MityDSP module in parallel with the carrier board, and as such there is limited clearance between the MityDSP module and the carrier board. Therefore it is impossible to place high-profile carrier board components underneath the MityDSP module. However, it is possible to utilize most of this space for low-profile components. Please refer to the following diagrams and tables for module-specific clearances.

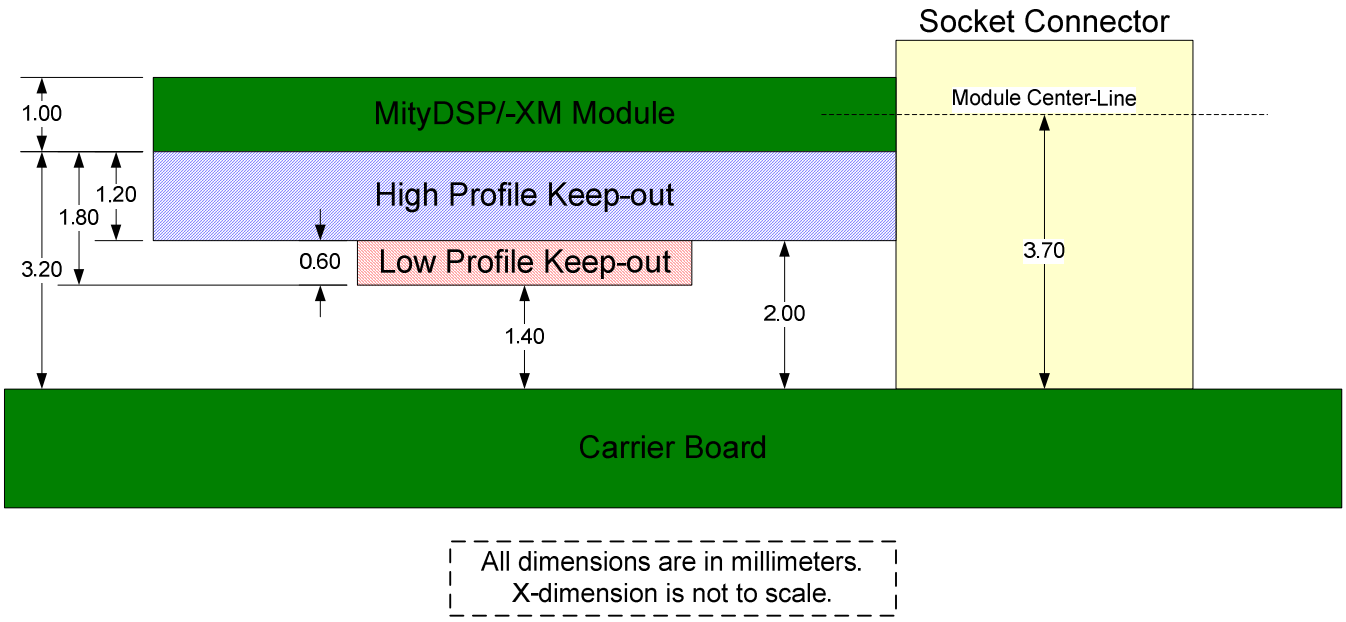

Figure 2: MityDSP/-XM Module Clearance - Side View

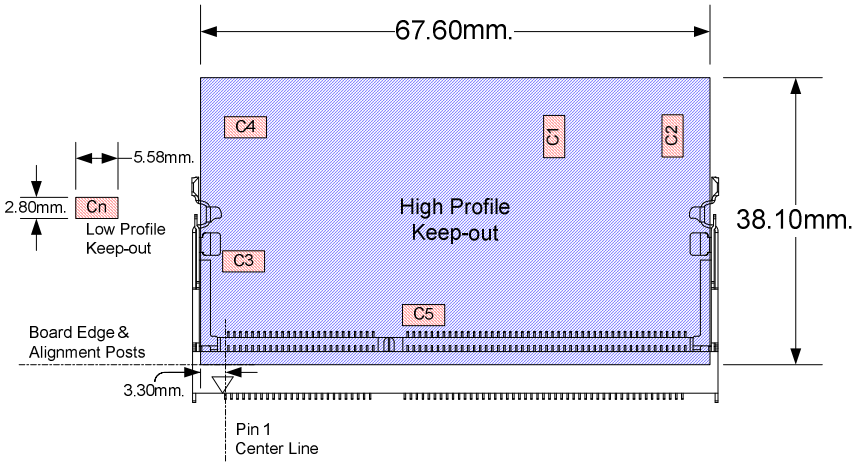

Figure 3: MityDSP Keep-out Zones

Table 5: MityDSP Low Profile Keep-out Centroids

Centroids:	From Pin-1 CL and lower-edge	
Component	X (mm)	Y (mm)
C1	43.61	30.28
C2	59.31	30.36
C3	2.42	13.72
C4	2.67	31.50
C5	26.29	6.60

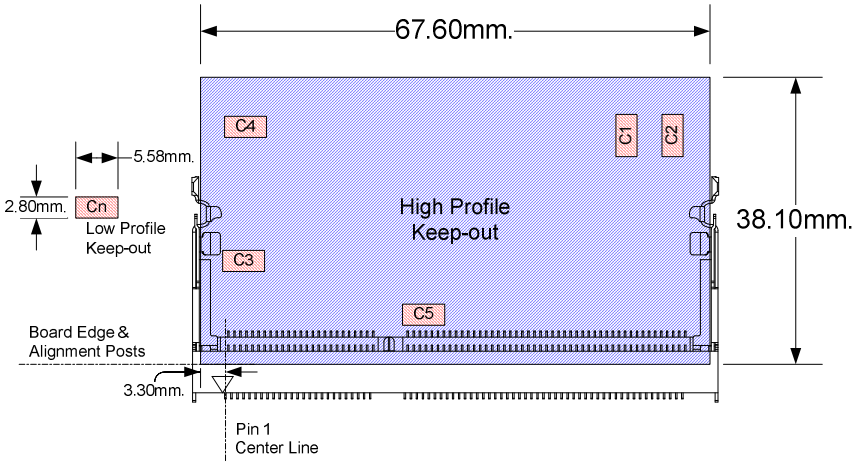

Figure 4: MityDSP-XM Keep-out Zones

Table 6: MityDSP-XM Low Profile Keep-out Centroids

Centroids:	From Pin-1 CL and lower-edge	
Component	X (mm)	Y (mm)
C1	53.22	30.36
C2	59.31	30.36
C3	2.42	13.72
C4	2.67	31.50
C5	26.29	6.60

4.3 Mounting Methods

Apart from the main interface I/O connector, all MityDSP modules feature optional additional mechanical attachment methods. Optionally available for the MityDSP and MityDSP-XM modules is a small metal clip fabricated from spring steel that captures the free-floating edge of the module PCB and can then be mechanically fastened to the carrier board with standard hardware. The mechanical drawing Figure 5 and photo Figure 6 below illustrates this concept. Contact Critical Link for metal clip mechanical drawings and ordering information.

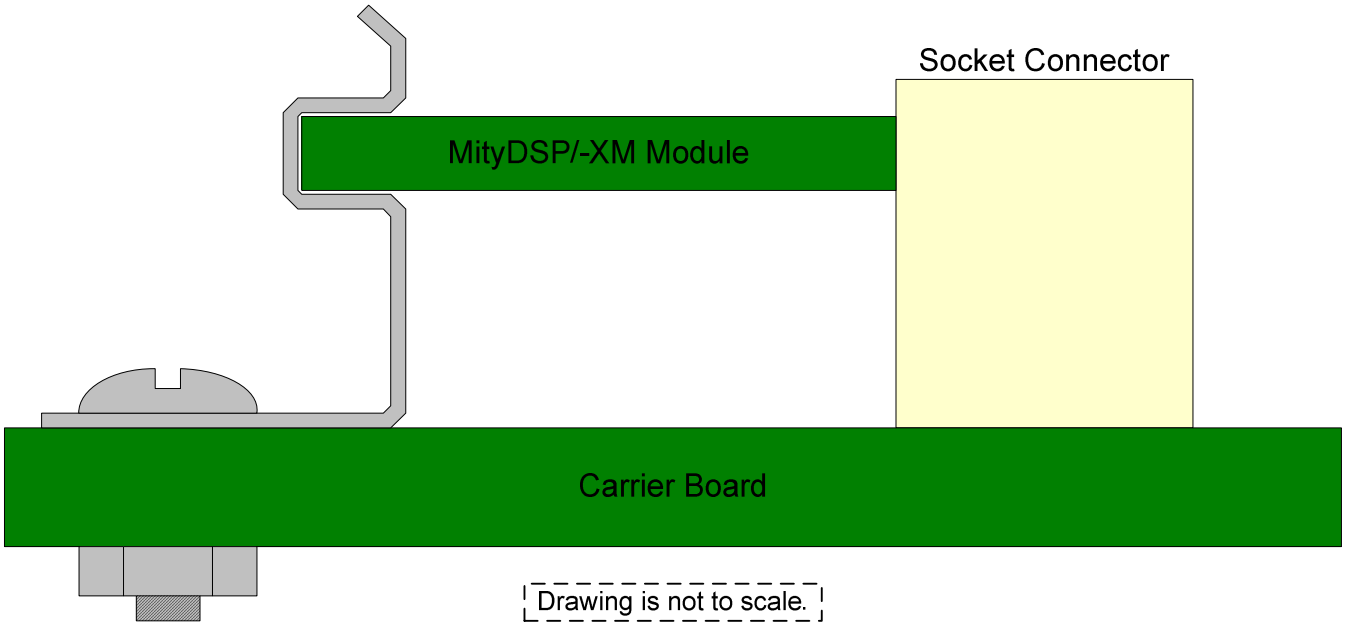

Figure 5: Metal Clip Concept Drawing

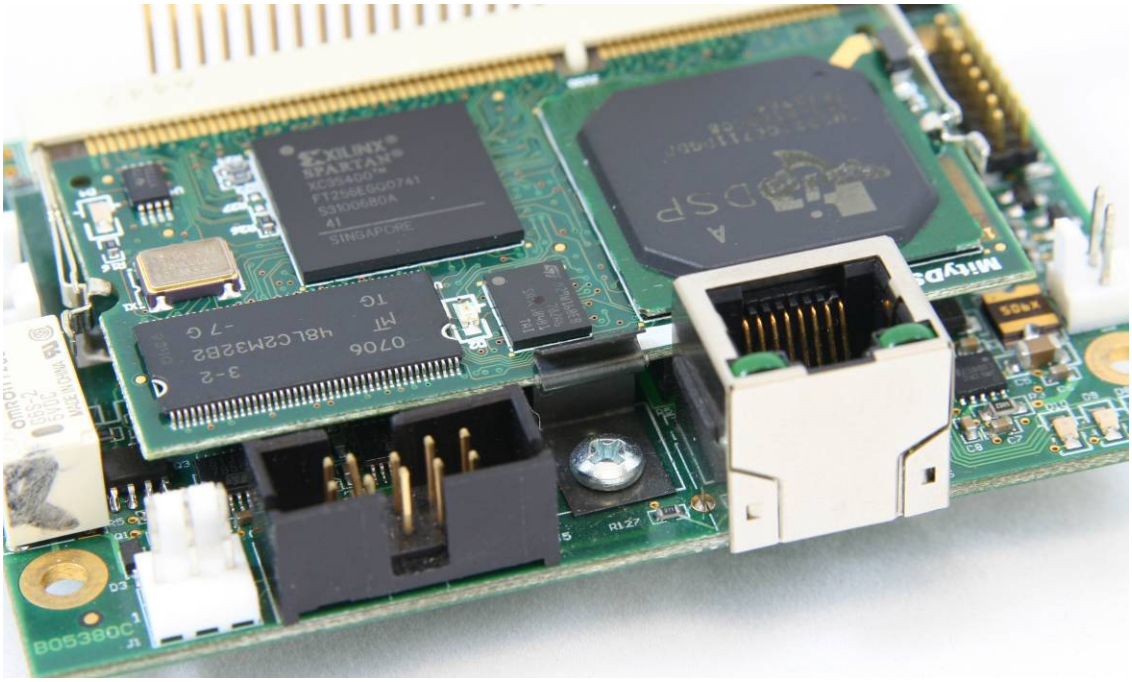

Figure 6: Photo of MityDSP held in place by Metal Clip

4.4 Shock & Vibration

For customers who are interested in using MityDSP modules in rugged environments, the optional mechanical attachment methods discussed in section 4.3 above enable MityDSP modules to tolerate much greater mechanical shock and vibration forces than without any additional mounting support. The MityDSP and MityDSP-XM modules have been tested for high mechanical shock and vibration stress both with and without the optional metal clip. Please contact Critical Link for details of these tests.

4.5 Thermal Management

The MityDSP and MityDSP-XM modules have no specific requirements regarding thermal management. The modules can be operated without heat sinks or air flow, and inside tight enclosures. However, if a module is intended to be used in hot industrial environments, it is advisable to do plenty of testing in the enclosure and environment that the MityDSP module will be used in. In these cases, it may be necessary to either add thermal management to the enclosure, or lower the operating temperature specification of the end product.

5 Board Layout Recommendations

The following sections discuss topics for successful board layouts incorporating any MityDSP module.

5.1 Placement

Placement of the MityDSP module site is crucial to a successful carrier board layout. Because the module connector footprint is fine-pitch and dual-row, it is generally best to place the connector fairly centered in the overall board layout. This placement allows traces to be routed out from both sides of the connector, using mainly top-side copper tracks. The use of less signal layers, and therefore less vias, generally results in a more compact design with better signal integrity than a board using many layers and vias. Of course, ideally central placement is not always possible because of other mechanical constraints.

Mechanically, enough space must be allocated for the full extension of the MityDSP module. Although it is possible for a MityDSP module to hang over the edge of its carrier board, this may not be desirable if additional mechanical attachment methods are desired for ruggedness, as discussed in sections 4.3 and 4.4. Another thing to keep in mind with placement on the carrier board and in enclosures is the cam-in action of the MityDSP modules into their respective sockets. The modules are generally installed at an angle of about 25° to 30° before swinging down to locked position. Enclosure designs should accommodate this motion.

5.2 Pin-out and Routing

Because the MityDSP module pins are mostly configurable FPGA I/O, board level pin-out and routing is greatly simplified. This is done by taking advantage of the FPGA tools' sophisticated signal routing capabilities, instead of creating a tangled mess of tracks and vias in copper. MityDSP pin allocation in the schematic is generally best done in tandem with PCB layout. In this method, the components are first captured in schematic, but not yet connected to the MityDSP's configurable FPGA I/O pins, except for the dedicated functionality pins. Then in PCB layout, parts are placed according to mechanical and positional requirements with components needing connection to the MityDSP placed nearby the MityDSP's socket connector. At this point it becomes much easier to see which MityDSP pins are ideal for allocation for the various required functions. The designer can then go back and forth between schematic and layout to complete the connections between IC's and the MityDSP connector. Some PCB design tools make this process even easier with abilities to automatically re-assign nets to pins that would otherwise require many crossovers in copper features to complete. Once the signals are assigned to pins on the MityDSP, this information can be given to the FPGA designer who will capture the pin-out in a User Constraints File (UCF) for input into the FPGA's place and route tools.

5.3 Access issues

Given that it is possible and often desirable to make best use of available space by placing components underneath the MityDSP module (refer to section 4.2), hardware and software engineers who will be debugging code on the platform could find themselves in a tough situation if the component they need to access is blocked by the installed MityDSP module. Because of these situations it is advisable to either not use the space under

the MityDSP module for active components that might need live probing with the MityDSP in-circuit, or only place circuits there that are already tried and tested by engineers on other platforms. In the event that an obscured circuit does need to be probed, it may be necessary to solder temporary wires onto probe points. An even better solution would be to design the board with bottom-side test points, at least in the MityDSP region, if this is possible on a given design.

5.4 PCB/PCA Technology

MityDSP modules do not have any specific requirements about the PCB technology used for its carrier board. The required socket connectors are available as RoHS compliant, and may be used in both leaded and lead-free assembly processes. The only recommendation is to fabricate the carrier board thick enough to rigidly support the MityDSP socket connector. In practice, FR-4 with a common finished thickness of 0.062 inches is enough for all types of MityDSP modules.

5.5 PCB Footprints

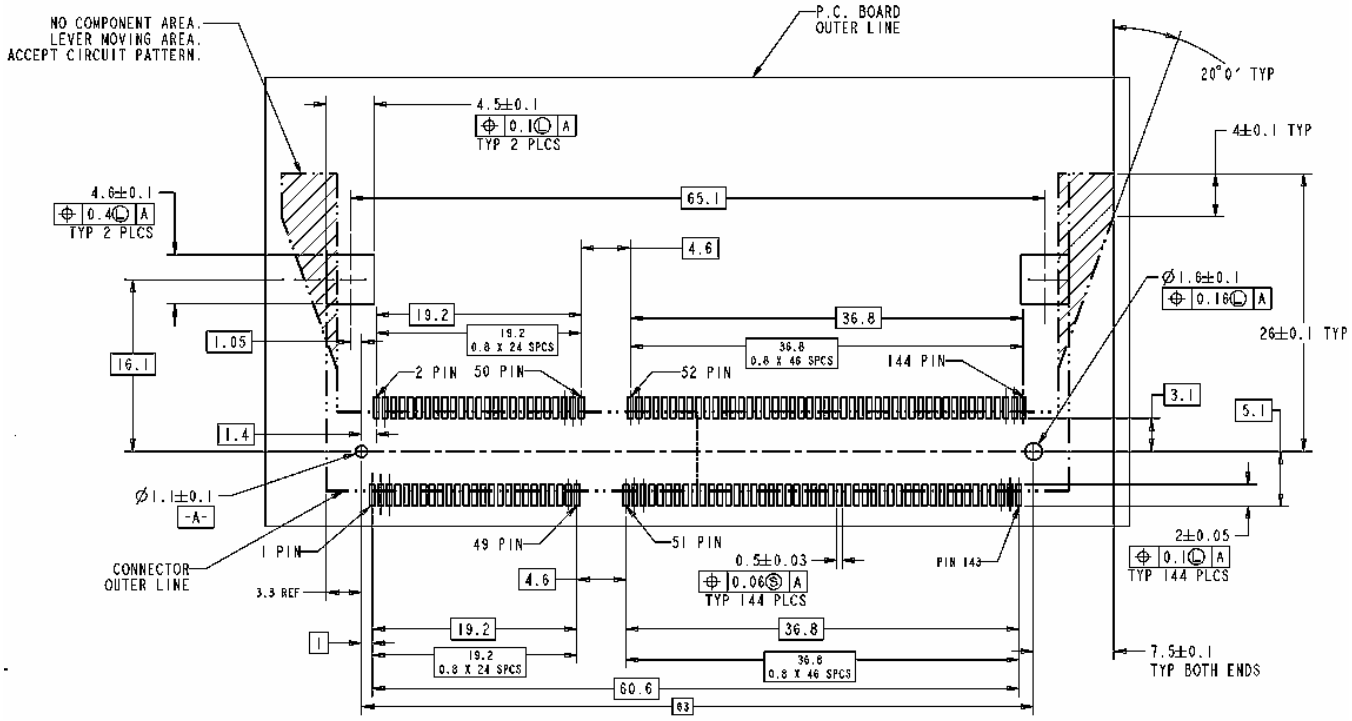

Figure 7: AMP/Tyco 390111-1 Recommended PCB Footprint

A. Appendix

A.1 Reference Schematics

A.2 Reference Layouts