MityARM™ Document

Document: MityARM-335x Carrier Board Design Guide

Revision: 1.5

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1 Overview

1.1 Fast Facts for Getting Started

Facts	MityARM-335x
Required socket connector	JAE Electronics MM80-204B1-E1, MM80-204B1-1 or equivalent
Voltage required	3.3V to 5V
Serial Peripherals*	6x UART, 2x SPI, 2x I2C, 2x McASP, 2x CAN, 2x USB, 2x EMAC (MII or RMII or RGMII)
Other Peripherals*	8x ADC, 4x Timer, 3x eHRPWM, 3x eQEP, 3x eCAP
PRU Peripherals*	UART, MII/MDIO, eCAP
*Peripherals share pins, see AM335x datasheet and Appendix for specific pin-multiplexing options	

1.2 Introduction

The MityARM-335x family of modules are System on Modules (SoMs) designed to be easy to integrate into an end-user embedded system. The modules integrate many crucial elements of an embedded system, and do so with an established design framework utilizing a common set of core libraries. End-user design of the application PCB is also intended to be as simple as possible, allowing the PCB designer to concentrate on the custom I/O interfaces – especially analog & mixed-signal – instead of getting distracted with the learning curve of designing a brand new embedded digital system from scratch.

1.3 MityARM-335x Family Modules

The MityARM-335x family of modules represents a 4th generation SoM in the MityDSP/MityARM product line. These modules are based on a Texas Instruments AM335x family of System On Chip (SOC) IC's.

Each module includes power management, DDR2 SDRAM, NAND and NOR Flash memories, and is interfaced by a 204-pin low-profile SO-DIMM card-edge connector. Carrier board design for these types of MityARM is the main focus of this document.

The MityDSP-L138, MityARM-1808, and MityDSP-6748 family of modules represents a 3rd generation SoM in the MityDSP product line. These modules are based on a Texas Instruments OMAPL138, Sitara AM1808, and the TMS320C6748 System On Chip (SOC) modules, respectively. Each of these SOC modules are pin compatible

devices that employ one or both of an ARM 9 core and a DSP 674x floating point DSP core according to the table below.

Core	OMAPL138	AM1808	TMS320C6748
ARM926EJ-S 300/375/456 MHz	Y	Y	N
DSP 674X Floating Point DSP 300/375/456 MHz	Y	N	Y

In addition, this 3rd generation of modules also features models that include a Xilinx Spartan-6 FPGA tightly integrated with the processor.

The 2nd generation module, the MityDSP-Pro (MityDSP-6455), is based on a Texas Instruments TMS320C645x DSP, includes DDR2 SDRAM and Flash memories, and is interfaced by the same 200-pin SO-DIMM card-edge connector and a 100-pin high-density, low-profile Hirose connector. The module integrates a large Xilinx Spartan3 FPGA for implementing required on-board logic and I/O interfaces, but primarily for end-user customizable logic and I/O interfaces. The module also incorporates a number of high bandwidth I/O interfaces including: PCI/HPI, Serial RapidIO, and Gigabit Ethernet interfaces provided by the DSP; and DDR SDRAM dedicated to the FPGA.

The 1st generation family of modules, the MityDSP and MityDSP-XM (MityDSP-6711 and MityDSP-6711XM), are based on a Texas Instruments TMS3206711 DSP, include SDRAM and Flash memories, and are interfaced using a 144-pin SO-DIMM card edge connector. The module integrates a Xilinx Spartan 3 FPGA for implementing required on-board logic and I/O interfaces.

All types of MityDSP are available with options for speed grade, memory size, FPGA size (or complete removal), operating temperature ranges, and RoHS compliant. Please contact Critical Link for the current list of MityDSP and MityARM variants.

1.4 Module Dimensions

A dimensioned drawing of module is included below in Figure 1.

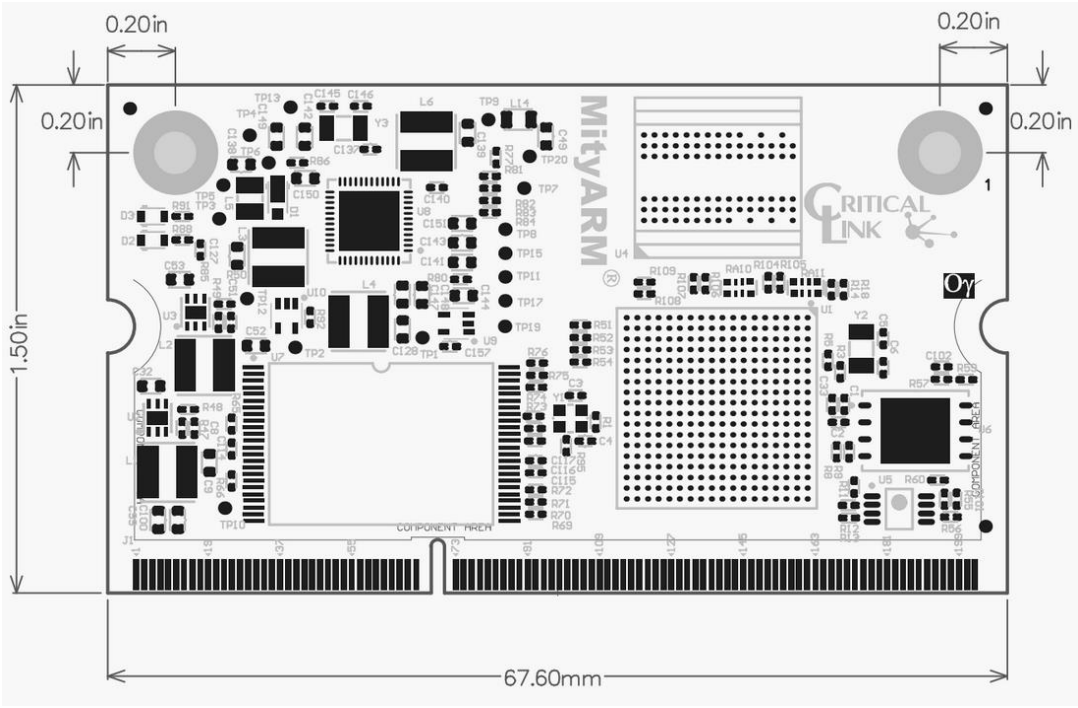

Figure 1: MityARM-335x Mechanical Drawing

1.5 Links to Design Documents

There are many useful documents and resources available that can be referenced when designing a system with the MityARM-335x module which are listed below. It is recommended that the information on the TI webpages be reviewed often for updates.

AM335x Data sheet	http://www.ti.com/lit/ds/symlink/am3359.pdf
AM335x Technical Reference Manual (Rev I)	http://www.ti.com/litv/pdf/spruh73i
AM335x "Home" Page	http://www.ti.com/product/am3359#technicaldocuments
TPS65910A PMIC Data Sheet	http://www.ti.com/lit/ds/symlink/tps65910.pdf

2 Connectors

The MityARM-335x utilizes a 204 pin, SO-DIMM style edge-connector for connectivity with the end user application PCB. This connector was chosen for its high density, compact size, ease of procurement, and low cost. With edge connectors, a physical socket component is only required on one side – the main PCB side. The SO-DIMM standard also allows the MityARM-335x module to lay flat, in parallel with the main PCB as they were intended for use by memory modules in compact equipment, such as laptops. Other connector styles are available that also allow for vertically mounting the MityARM-335x.

2.1 Card-edge compatibility

The MityARM-335x is designed to plug into a 204-pin SO-DIMM DDR3 RAM socket. These sockets are commonly used for memory in PC products. Please note that the MityARM-335x is NOT electrically compatible with the DDR3 socket standard. Intermixing modules/sockets from the two standards would very possibly cause permanent damage to one or both sides.

2.2 MityARM-335x Module Pin-out

Table 1: MityARM-335x Card-edge (J1) Pin-out

Pin	Signal	Pin	Signal
1	VIN	2	GND
3	VIN	4	GND
5	VIN	6	GND
7	VIN	8	GND
9	VIN	10	GND
11	VIN	12	GND
13	VIN	14	GND
15	VIN	16	GND
17	GND	18	GND
19	GND	20	GND
21	VIO_3P3	22	VIO_1P8
23	VIO_3P3	24	VIO_1P8
25	VIO_3P3	26	VIO_1P8
27	VIO_3P3	28	VIO_1P8
29	LCD_DATA0	30	LED_RTN
31	LCD_DATA1	32	PWR_ON
33	LCD_DATA2	34	VBACKUP
35	LCD_DATA3	36	PMIC_SLEEP
37	GND	38	GND
39	LCD_DATA4	40	GND
41	LCD_DATA5	42	GND

Pin	Signal
43	LCD_DATA6
45	LCD_DATA7
47	LCD_DATA8
49	LCD_DATA9
51	LCD_DATA10
53	LCD_DATA11
55	GND
57	LCD_DATA12
59	LCD_DATA13
61	LCD_DATA14
63	LCD_DATA15
65	LCD_PCLK
67	LCD_VSYNC
69	LCD_HSYNC
71	LCD_AC_BIAS_EN
73	GND
75	GPMC_AD0
77	GPMC_AD1
79	GPMC_AD2
81	GPMC_AD3
83	GPMC_AD4
85	GPMC_AD5
87	GPMC_AD6
89	GPMC_AD7
91	GND
93	GPMC_AD8
95	GPMC_AD9
97	GPMC_AD10
99	GPMC_AD11
101	GPMC_AD12
103	GPMC_AD13
105	GPMC_AD14
107	GPMC_AD15
109	GND
111	GPMC_CSN2
113	GPMC_CSN1
115	USB0_VBUS
117	USB0_ID
119	USB1_VBUS
121	USB1_DP
123	USB1_DM
125	USB1_CE

Pin	Signal
44	VDDS_HV2
46	VDDS_HV2
48	VDDS_HV4
50	VDDS_HV4
52	PMIC_INT_N
54	GND
56	GND
58	GPMC_A0
60	GPMC_A1
62	GPMC_A2
64	GPMC_A3
66	GPMC_A4
68	GPMC_A5
70	GPMC_A6
72	GPMC_A7
74	GND
76	GPMC_A8
78	GPMC_A9
80	GPMC_A10
82	GPMC_A11
84	GPMC_CLK
86	GPMC_BEN0_CLE
88	GPMC_ADVN_ALE
90	GPMC_OEN_RE_N
92	GND
94	GPMC_CSN3
96	RFU
98	GPMC_WE_N
100	GPMC_WAIT0
102	GPMC_BEN1
104	GPMC_WP_N
106	RFU
108	RFU
110	GND
112	GMII1_RXD0
114	GMII1_RXD1
116	GMII1_RXD2
118	GMII1_RXD3
120	GMII1_RXCLK
122	GMII1_RXDV
124	RFU
126	GMII1_TXCLK

Pin	Signal
127	GND
129	USB1_ID
131	USB0_DM
133	USB0_DP
135	USB0_CE
137	USB1_DRVVBUS
139	USB0_DRVVBUS
141	MDC
143	MDIO
145	RMII1_REFCLK
147	I2C1_SDA
149	I2C1_SCL
151	MMC0_CMD
153	MMC0_CLK
155	MMC0_DAT0
157	MMC0_DAT1
159	MMC0_DAT2
161	MMC0_DAT3
163	GND
165	UART0_CTSN
167	UART0_RTSN
169	UART0_TXD
171	UART0_RXD
173	UART1_RXD
175	UART1_TXD
177	I2C0_SDA
179	I2C0_SCL
181	GND
183	SPI0_D0
185	SPI0_D1
187	SPI0_SCLK
189	SPI0_CS1
191	SPI0_CS0
193	SPI1_SCLK
195	SPI1_D0_MOSI
197	SPI1_D1_MISO
199	GND
201	XDMA_EVENT_INTR1
203	XDMA_EVENT_INTR0

Pin	Signal
128	GMII1_TXD0
130	GMII1_TXD1
132	GMII1_TXD2
134	GMII1_TXD3
136	GMII1_TXEN
138	GMII1_COL
140	RFU
142	RFU
144	MCASP0_AXR1
146	GND
148	MCASP0_FSR
150	MCASP0_ACLKR
152	MCASP0_ACLKX
154	MCASP0_AHCLKX
156	EXTINT_N
158	WARMRST_N
160	EMU0
162	EMU1
164	GND
166	TCK
168	TDI
170	TDO
172	TMS
174	TRSTN
176	VREFN
178	VREFP
180	EXT_WAKEUP
182	GND
184	AIN0
186	AIN1
188	AIN2
190	AIN3
192	AIN4
194	AIN5
196	AIN6
198	AIN7
200	GND
202	AGND
204	AGND

Table 2: MityARM-335x Signal Group Description

Signal / Group	Type	# Pins	Description
VIN	PWR	8	MityARM-335x input power referenced to GND.
GND	PWR	33	System Digital Ground.
VIO_3P3	PWR	4	3.3 Volt power supply pins. Power is available on these pins to supply power to the VDDSHV2 or VDDSHV4 power domains on the AM335x processor. If used as an external supply the current usage should be limited to 500mA.
VIO_1P8	PWR	4	1.8 Volt power supply pins. Power is available on these pins to supply power to the VDDSHV2 or VDDSHV4 power domains on the AM335x processor. If used as an external supply the current usage should be limited to 500mA.
VDDSHV2	PWR	2	Input Power for the HV2 power domain on the AM335x processor. These pins are directly connected to the corresponding VDDSHV2 pins on the AM335x processor. For additional details please refer to the AM335x Datasheet and Technical Reference manual.
VDDSHV4	PWR	2	Input Power for the HV4 power domain on the AM335x processor. These pins are directly connected to the corresponding VDDSHV4 pins on the AM335x processor. For additional details please refer to the AM335x Datasheet and Technical Reference manual.
LED_RTN	PWR	1	LED Return This pin is connected to the cathode of the two LEDs on the MityARM-335x allowing the LEDs to be disabled for applications that require low power.
VBACKUP	PWR	1	MityARM-335x Backup Power Source. This pin is directly connected to the TPS65910 Power Management IC and can be used to provide backup power to support a Real Time Clock and various sleep modes. For additional details, please refer to the TPS65910 Datasheet.
PMIC_INT_N	O	1	Power Management IC Interrupt flag. This pin is directly connected to the TPS65910 Power Management IC and can be used to report power problems to the AM335x processor. For additional details, please refer to the TPS65910 Datasheet.
PWR_ON	I	1	External Switch-On Control pin. This pin is directly connected to the TPS65910 Power Management IC and can be used to power the MityARM-335x on or off. There is a pull up resistor on the module allowing this pin to be left floating if user control is not desired. For additional details, please refer to the TPS65910 Datasheet.

Signal / Group	Type	# Pins	Description
PMIC_SLEEP	I	1	Sleep State Transition Control pin. This pin is directly connected to the TPS65910 Power Management IC and can be used to control the sleep state of the TPS65910. This pin should be pulled up to VIO_3P3 if it is not used. For additional details, please refer to the TPS65910 Datasheet.
EXT_WAKEUP	I	1	AM335x External Wakeup pin. This pin is directly connected to the corresponding pin on the AM335x processor. For additional details please refer to the AM335x Datasheet and Technical Reference manual.
EXTINT_N	I	1	Non-Maskable External Interrupt pin. This pin is directly connected to the corresponding pin on the AM335x processor. For additional details please refer to the AM335x Datasheet and Technical Reference manual.
WARMRST_N	I	1	Manual Reset. When pulled to GND for a minimum of 1 usec, resets the AM335x processor.
RMII1_REFCLK	I/O	1	Reduced Media Independent Interface Reference Clock pin. This pin is directly connected to the corresponding RMII1_REFCLK pin on the AM335x processor. This pin is multiplexed with other functions available in the AM335x as summarized in the Pin Function Table located in the Appendix. For additional details please refer to the AM335x Datasheet and Technical Reference manual.
LCD_*	I/O	20	Liquid Crystal Display pins. These pins are directly connected to the corresponding LCD_* pins on the AM335x processor. The LCD_* function pins are multiplexed with other functions available in the AM335x as summarized in the Pin Function Table located in the Appendix. For additional details please refer to the AM335x Datasheet and Technical Reference manual.
USB0_*, USB1_*	I/O	12	Universal Serial Bus 0 / 1 pins. These pins are directly connected to the corresponding USB_* pins on the AM335x processor. All but two of the signals that comprise these two interfaces have dedicated pins on the AM335x. The USB0_DRVVBUS and USB1_DRVVBUS signals can also be used as general purpose I/O pins. For additional details please refer to the AM335x Datasheet and Technical Reference manual

Signal / Group	Type	# Pins	Description
SPI0_*	I/O	5	Serial Peripheral Interface 0 pins. These pins are directly connected to the corresponding SPI0_* pins on the AM335x processor. The SPI0_* function pins are multiplexed with other functions available in the AM335x as summarized in the Pin Function Table located in the Appendix. This interface is supported as a U-Boot boot device. For additional details please refer to the AM335x Datasheet and Technical Reference manual.
SPI1_*	I/O	3	Serial Peripheral Interface 1 pins. These pins are directly connected to the corresponding SPI1_* pins on the AM335x processor. Note that the SPI1_* interface is also connected to the NOR FLASH on the MityARM-335x module thereby locking down the function of these pins. For additional details please refer to the AM335x Datasheet and Technical Reference manual.
GPMC_*	I/O	39	General Purpose Memory Controller pins. These pins are directly connected to the corresponding GPMC_* pins on the AM335x processor. Note that a subset of the GPMC_* interface is also connected to the NAND FLASH on the MityARM-335x module thereby locking down the function of a subset of these pins. The remaining pins are multiplexed with other functions available in the AM335x as summarized in the Pin Function Table located in the Appendix. For additional details please refer to the AM335x Datasheet and Technical Reference manual.
GMII_*	I/O	13	Gigabit Media Independent Interface pins. These pins are directly connected to the corresponding GMII_* pins on the AM335x processor. The GMII_* function pins are multiplexed with other functions available in the AM335x as summarized in the Pin Function Table located in the Appendix. For additional details please refer to the AM335x Datasheet and Technical Reference manual.
MDIO MDC	I/O	2	Ethernet PHY Management Interface pins. The MDIO and MDC signals are directly connected to the corresponding signals on the AM335x processor. These pins are multiplexed with other functions available in the AM335x as summarized in the Pin Function Table located in the Appendix. For additional details please refer to the AM335x Datasheet and Technical Reference manual.

Signal / Group	Type	# Pins	Description
I2C0_*	I/O	2	Inter-Integrated Circuit Interface 0 pins. These pins are directly connected to the corresponding I2C0_* pins on the AM335x processor. The I2C0_* function pins are multiplexed with other functions available in the AM335x as summarized in the Pin Function Table located in the Appendix. For additional details please refer to the AM335x Datasheet and Technical Reference manual.
I2C1_*	I/O	2	Inter-Integrated Circuit Interface 1 pins. These pins are directly connected to the corresponding I2C1_* pins on the AM335x processor. Note that the I2C1_* interface is also connected to the Configuration EEPROM and Power Management IC on the MityARM-335x module thereby locking down the function of these pins. For additional details please refer to the AM335x Datasheet and Technical Reference manual.
MMC0_*	I/O	6	MultiMedia Card Interface pins. These pins are directly connected to the corresponding MMC0_* pins on the AM335x processor. The MMC0_* function pins are multiplexed with other functions available in the AM335x as summarized in the Pin Function Table located in the Appendix. For additional details please refer to the AM335x Datasheet and Technical Reference manual.
UART0_* UART1_*	I/O	6	Universal Asynchronous Receive Transmit Interface 0 / 1 pins. These pins are directly connected to the corresponding UART0_* and UART1_* pins on the AM335x processor. The UART0_* and UART1_* function pins are multiplexed with other functions available in the AM335x as summarized in the Pin Function Table located in the Appendix. For additional details please refer to the AM335x Datasheet and Technical Reference manual.
MCASP0_*	I/O	5	MultiChannel Audio Serial Port Interface pins. These pins are directly connected to the corresponding MCASP0_* pins on the AM335x processor. The MCASP0_* function pins are multiplexed with other functions available in the AM335x as summarized in the Pin Function Table located in the Appendix. For additional details please refer to the AM335x Datasheet and Technical Reference manual.

Signal / Group	Type	# Pins	Description
XDMA_EVENT_INTR0 XDMA_EVENT_INTR1	I/O	2	External DMA Event or Interrupt Interface 0 / 1 pins. These pins are directly connected to the corresponding XDMA_EVENT_INTR0/1 pins on the AM335x processor. The XDMA_EVENT_INTR0/1 function pins are multiplexed with other functions available in the AM335x as summarized in the Pin Function Table located in the Appendix. For additional details please refer to the AM335x Datasheet and Technical Reference manual.
AIN0-7	I	8	Analog Input Interface 0 - 7 pins. These pins are directly connected to the corresponding AIN* pins on the AM335x processor. For additional details please refer to the AM335x Datasheet and Technical Reference manual.
VREFP VREFN	PWR	2	Positive and Negative Analog Input Reference pins. These pins are directly connected to the corresponding VREFP and VREFN pins on the AM335x processor. For additional details please refer to the AM335x Datasheet and Technical Reference manual
AGND	PWR	2	System Analog Ground. Ground reference for the analog inputs and analog reference. Note that the MityARM-335x connects the Analog Ground (AGND) to the Digital Ground (GND) through a ferrite bead, part number Murata BLM15BB470SN1D.
TMS TDI TDO TCK TRSTN EMU0 EMU1	I/O	7	JTAG/Debugger Interface pins. These pins are directly connected to the corresponding JTAG/Debugger pins on the AM335x processor. All but two of the signals that comprise this interface are dedicated pins on the AM335x. The EMU0 and EMU1 pins can also be used as general purpose I/O pins. For additional details please refer to the AM335x Datasheet and Technical Reference manual
RFU	-	6	Reserved for future Use. No connections should be made to these pins.

3 Electrical Requirements

The following sections describe the various electrical requirements for the MityARM-335x module.

3.1 Power Supplies

The MityARM-335x module requires only one regulated power supply for the main power input rail. All other required power rails are generated on the-module by a combination of switching and linear, high-efficiency voltage regulators. The main power input rail can be sourced by either a linear or switching regulator as system requirements dictate. Table 3 describes the input voltage specifications and Table 4 provides current requirements.

Table 3: Module Voltage Specifications

Spec.	Minimum	Typical	Maximum	Units
V_{IN}	3.2	3.3	5.5	V

Table 4: Module Current Requirements

Spec.	Minimum	Typical	Maximum	Units
$I_{3.3V}$	240	500	TBD*	mA

*Note that module current requirements can vary considerably based upon many factors including, but not limited to, application loading, CPU clock speed, memory type, presence of NAND, etc.

3.1.1 Power Supply Sequencing

Based upon TI's AM335x processor datasheet it is recommended that the power supplies of any peripherals interfacing with a MityARM-335x SoM be brought up after the AM335x processor has been powered. We have included the power supply sequencing for our MityARM-335x Development Kit Baseboard in Figure 2 below.

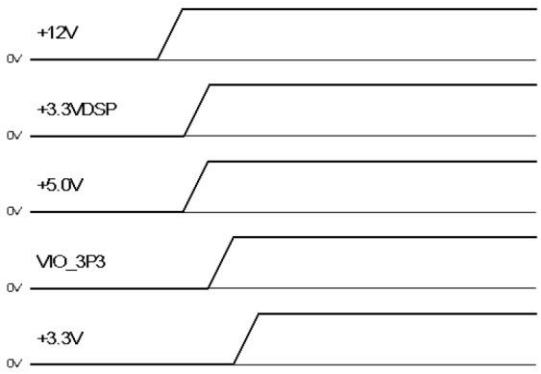

Figure 2: Example MityARM-335x Development Kit Baseboard Power Sequence

To accomplish the recommended power sequencing it is recommended that the MityARM-335x VIO_3P3 voltage output be used as an enable for the voltage supplies for any connected peripherals. Please refer to the Appendix for a list of the pins that output this voltage net.

In reference to the sequence of Figure 2 above Critical Link chose to split the 3.3V power supply on the baseboard into two separate domains through the use of a MOSFET enable circuit shown in Figure 3. The +3.3VDSP is the first to come on and powers only the MityARM-335x module through the VIN pins. When the module begins to output the VIO_3P3 voltage the "peripheral" +3.3V voltage domain on the baseboard is then enabled. Note that in some designs another common peripheral voltage that may require this sequencing control would be 1.8V powered peripherals.

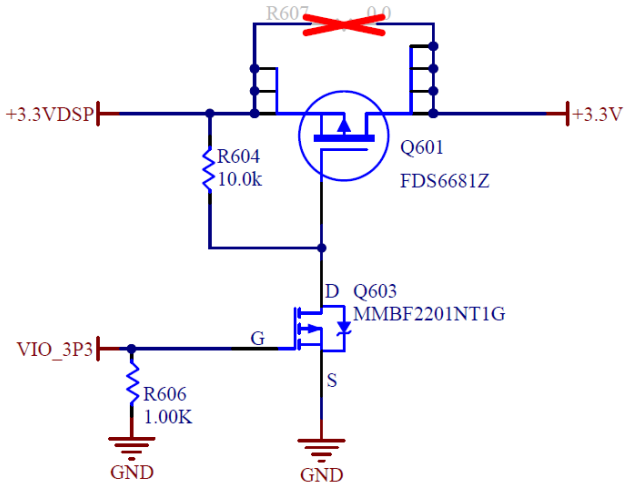

Figure 3: Voltage Sequencing Schematic Example

Critical Link has provided one example as shown on our MityARM-335x Development Kit Baseboard reference design; please contact your Critical Link representative to obtain the schematic and/or design files.

3.2 Recommended Capacitance

The MityARM-335x module includes some power supply rail bypass capacitors on-board, however additional capacitance is recommended on the carrier board to minimize the ripple effect caused by changing load currents. It is recommended to place one 10uF tantalum capacitor nearby each power supply pin pair. Please note that this is the minimum recommended amount of additional capacitance, and more is typically better.

3.3 I/O Interfaces

Most of the I/O pins directly connected to the AM335x processor are compliant to only 3.3V I/O standards. There are three groups of pins that are exceptions to this including:

- The USB interfaces – These interfaces utilize a low voltage differential signaling in accordance with the USB standard.
- All AM335x processor I/O pins powered from the HV2 power domain – These pins can be powered from either 1.8 volts or 3.3 volts as required by the application. The MityARM-335x provides 1.8 volt and 3.3 volt power on pins VIO_1P8/VIO_3P3 which can be connected to the VDDSHV2 pins on the connector. Please refer to the Appendix for a list of the pins contained within the HV2 power domain.
- All AM335x processor I/O pins powered from the HV4 power domain – These pins can be powered from either 1.8 volts or 3.3 volts as required by the application. The MityARM-335x provides 1.8 volts and 3.3 volts power on pins VIO_1P8/VIO_3P3 which can be connected to the VDDSHV4 pins on the connector. Please refer to the Appendix for a list of the pins contained within the HV4 power domain.

3.3.1 I/O Protection

Any I/O interfaces that are external to the MityARM-335x module must be protected to ensure that no out of range voltage conditions occur as the all I/O pins are direct to the AM335x processor. The host board should contain the necessary protection/isolation circuits as required to protect the processor. Please refer to the AM335x Datasheet for details about maximum voltage ranges for both 3.3V and 1.8V I/O domains as the maximum ranges are different.

3.4 Module Boot Configuration

The MityARM-335x is capable of booting from a number of peripherals as defined by the state of the 16 LCD_DATA pins at the time of a reset. The state of the 16 data lines is sampled on the rising edge of the power-on-reset signal to determine the search order of peripherals for a valid boot image. The host board needs to provide pull up/down resistors (10K) on the lower 12 bits of the LCD_Data pins to select the desired boot mode for the target application. When a boot mode pin is being pulled up the resistor should utilize the VIO_3P3 voltage output from the MityARM-335x module to ensure proper read timing. Please refer to the Appendix for a list of the pins that output this voltage net.

Note that bits 15 to 12 are already pulled high/low on the MityARM-335x module as binary pattern 0100b. Please refer to the AM335x Technical Reference Manual for guidance in selecting the desired boot mode.

3.5 Debugger Interface

The MityARM-335x JTAG/Debugger interface is available on the I/O connector and it is strongly recommended that this interface be wired up to a header so a debugger can be attached to the design. A basic debugger interface can be inexpensively implemented with a 14 pin header such as a Sullins Electronics PTC36DAAN as shown in Figure 4. Additional capability can be added to the debugger connector as required including trace. A good source of information on the JTAG/Debugger interface can be found at the following link:

http://processors.wiki.ti.com/index.php/JTAG_Connectors

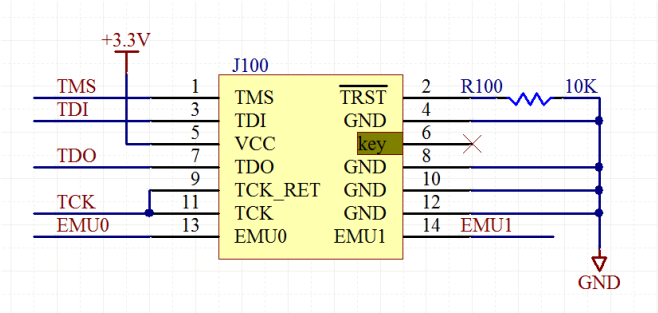

Figure 4: JTAG/Debugger Interface

3.6 RS232 Monitor Interface

It is strongly recommended that UART0 be used as a general purpose monitor port which can double as a boot peripheral. This port will require a physical Interface (PHY) chip, a connector, and a handful of discrete parts as shown in Figure 5. The PHY chip commonly used by Critical Link for this interface is the TI MAX3232.

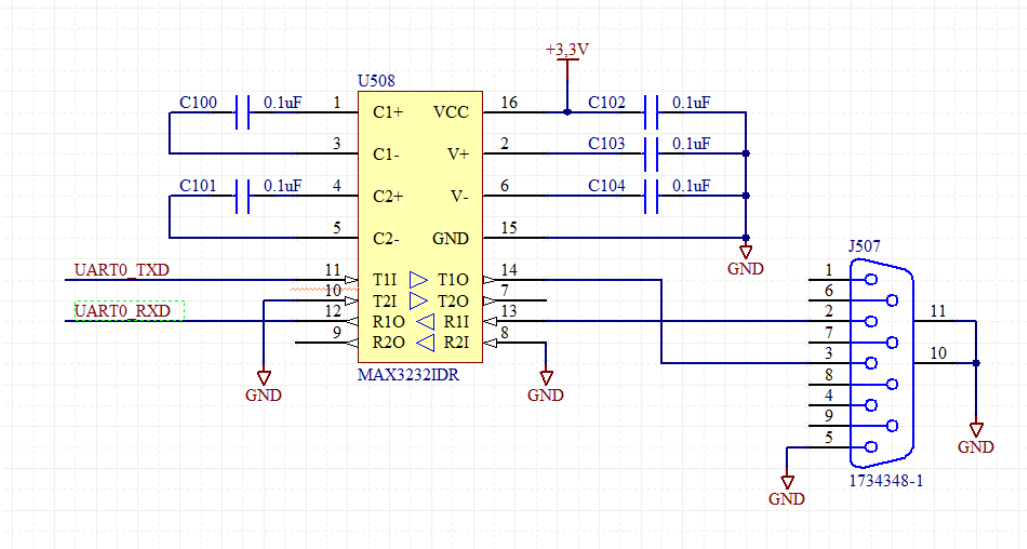

Figure 5: RS232 Monitor Port

3.7 LED Power Return

There are two LEDs on the MityARM-335x. One of the LEDs (D2) is hardwired to a voltage source to indicate that the module is powered while the other LED (D3) is connected to a GPIO pin and software controlled. Some applications may require very low power or blackout conditions so the cathodes of the two LEDs are connected to I/O connector pin LED_RTN. This allows the LEDs to be disabled in situations where power or visibility is a concern. Typically the LED_RTN pin would be connected to GND which would enable both LEDs.

3.8 Battery Backup

The host board can use a battery to maintain a real time clock and is connected to I/O connector pin VBACKUP. A recommended battery to use for this situation is a Panasonic BR1225-1VC. If a battery is not used, the VBACKUP pin should be connected to VIN.

Table 5: VBACKUP Current Draw

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{VBackup}$	VBACKUP Current draw[2]	3.3 VIN applied to SoM	-	<1	1	uA
$I_{VBackup-Active}$	VBACKUP Current draw	PMIC RTC active	-	10.2	-	uA

4 Interface Descriptions

4.1 Module Reset

On the MityARM-335x module, the main power input supply and all on-module generated power supplies are monitored and will trigger a module hard-reset if any of them fails or goes unstable. Also included on this module is a manual-reset (WARMRST_N) input pin that can be connected to a carrier board system reset and power supply monitoring circuitry.

4.2 Emulator/JTAG

The I/O connector on the MityARM-335x has a full set of JTAG/Debugger signals that can be used to connect to an emulator for code downloads and real time debugging.

4.3 McASP Port

The MityARM-335x module can provide up to two Multi-Channel Audio Serial Ports. The multichannel audio serial port (McASP) functions as a general-purpose audio serial port optimized for the needs of multichannel audio applications. The McASP is useful for time-division multiplexed (TDM) stream, Inter-Integrated Sound (I2S) protocols, and intercomponent digital audio interface transmission (DIT). The McASP consists of transmit and receive sections that may operate synchronized, or completely independently with separate master clocks, bit clocks, and frame syncs, and using different transmit modes with different bit-stream formats. The McASP module also includes serializers that can be individually enabled for either transmit or receive. For more information, please consult the AM335x device datasheets and Technical Reference Manual. Note that the McASP pins are shared with other peripherals.

4.4 Serial UARTs

The MityARM-335x module can support up to 6 Universal Asynchronous Receive/Transmit (UART) ports that all support IrDA, CIR, and RTS/CTS flow control. Additionally, the PRU Subsystem contains a single UART with flow control pins that can support data rates up to 12Mbps. UART0 should be configured as a UART as that is the factory default console port used to support the bootloading application as well as the console for most higher level operating systems. The other UARTs may be configured per application needs. For more information, please consult the AM335x device datasheets and Technical Reference Manual. Note that the UART pins are shared with other peripherals.

4.5 SPI Ports

The MityARM-335x module can support up to 2 Serial Peripheral Interface (SPI) ports with each port having up to 2 chip selects directly controlled by the peripheral. Additional chip selects can be implemented with general GPIO pins if necessary. Note that the SPI1 chip select 0, however, is reserved in order to support the on-board NOR flash. For more information, please consult the AM335x device datasheets and Technical Reference Manual. Note that the SPI pins are shared with other peripherals.

4.6 I2C Ports

The MityARM-335x module can support up to 3 Inter-Integrated Circuit (I2C) ports. I2C1 is connected to an on-board prom (address 1010XXXb) that is used to hold factory configuration data (serial number, MAC address, etc.) in addition to the Power Management IC (TPS65910) which uses address 00201101b. Users may use the I2C1 port to interface to other devices having different addresses than those mentioned on this bus. I2C2 is also connected to the Power Management IC to support the SmartReflex (address 00010010b) and is not available for use off board. I2C0 is available off board with no uses on the MityARM-335x module itself. For more information, please consult the AM335x device datasheets and Technical Reference Manual. Note that the I2C pins are shared with other peripherals.

4.7 USB

The MityARM-335x provides two Universal Serial Bus (USB) interfaces that are mapped directly to the edge connector of the module. Both USB ports are capable of operating using the On-The-Go (OTG) protocol and are USB 2.0 compliant. OTG protocols support dynamic switching from host mode (e.g., for controlling USB mass storage devices such as thumb drives) to client mode (e.g., for interfacing to a PC) based on application software. For more information, please consult the AM335x device datasheets and Technical Reference Manual.

4.8 LCD Controller

The MityARM-335x provides a Liquid Crystal Display (LCD) Controller port. This port consists of a 24-bit data bus, strobes, and clocks necessary to connect to industry standard LCD module interfaces up to WXGA resolution. The controller can operate in raster mode, or asynchronous memory-mapped mode (LIDD). For more information, please consult the AM335x device datasheets and Technical Reference Manual. Note that the LCD Controller pins are shared with other peripherals.

4.9 CAN Ports

The MityARM-335x module can support up to 2 Controller Area Network (CAN) ports with each port supporting CAN protocol version 2.0 part A,B. The CAN ports support bit rates up to 1 Mbps and have DMA and interrupt support. For more information, please consult the AM335x device datasheets and Technical Reference Manual. Note that the CAN pins are shared with other peripherals.

4.10 Analog Inputs

The MityARM-335x module contains a 12 bit Successive Approximation Register (SAR) Analog to Digital (ADC) converter. The ADC can be connected to 1 of 8 dedicated analog inputs which can be sampled at 100K samples per second. The Analog inputs can be configured to interface directly with a variety of touch screens including 4, 5 and 8 wire. The voltage reference for the ADC is connected to the VREFP and VREFN pins and is typically 1.8 volts. The analog inputs and voltage reference pins are all referenced to the AGND pins. For more information, please consult the AM335x device datasheets and Technical Reference Manual.

4.11 Timers

The MityARM-335x module contains up to 4 external Timers that can be individually configured as trigger inputs or PWM outputs. Each timer has a 32 bit register associated with it and supports 3 modes of operation: Timer mode, Capture mode, or Compare mode. For more information, please consult the AM335x device datasheets and Technical Reference Manual. Note that the Timer pins are shared with other peripherals.

4.12 MultiMedia Card

The MityARM-335x module contains up to 3 Multi-Media Card (MMC) interfaces that also support Secure Digital (SD) and Secure Digital Input/Output (SDIO) formats. The MMC interfaces can operate in 1bit, 4 bit, or 8 bit modes with a data transfer rate up to 48 MHz. The MMC ports are in compliance with MMC4.3 and SD/SDIO 2.0 specifications. For more information, please consult the AM335x device datasheets and Technical Reference Manual. Note that the MMC pins are shared with other peripherals.

4.13 Enhanced Capture

The MityARM-335x module contains up to three 32-bit Enhanced Capture (eCAP) modules that can be used to perform period and duty cycle measurements of external events. Each eCAP interface can also be configured as a PWM output. Note that the Programmable Real Time Subsystem (PRUSS) also contains a dedicated eCAP interface. For more information, please consult the AM335x device datasheets and Technical Reference Manual. Note that the eCAP pins are shared with other peripherals.

4.14 1 Enhanced High Resolution PWM

The MityARM-335x module contains up to three 32-bit Enhanced High-Resolution PWM (eHRPWM) modules that support extending time resolution capability and finer time granularity control or edge positioning. Each interface can be configured as six single ended, six dual-edge symmetric, or three dual-edge asymmetric outputs. For more information, please consult the AM335x device datasheets and Technical Reference Manual. Note that the eHRPWM pins are shared with other peripherals.

4.15 1 Enhanced Quadrature Encoder Pulse

The MityARM-335x module contains up to three Enhanced Quadrature Encoder Pulse (eQEP) modules that can interface directly to encoder disks like those used on shaft encoders For more information, please consult the AM335x device datasheets and Technical Reference Manual. Note that the eQEP pins are shared with other peripherals.

4.16 1 General Purpose Memory Controller

The MityARM-335x module contains a General Purpose Memory Controller (GPMC) that can be used for interfacing to external memory devices including SRAM-like memories, ASIC devices, and NAND Flash. The GPMC supports up to 100 MHz external memory clock performance. A subset of GPMC pins are used to interface to the onboard NAND Flash memory including AD[0:7], WAIT0, OEN_RE_N, BEN0_CLE, ADVN_ALE, WE_N, and WP_N. The remainder of the GPMC pins can be shared with other peripherals. For more information, please consult the AM335x device datasheets and Technical Reference Manual.

4.17 10/100/1000 Ethernet

The MityARM-335x module contains a 3-port switch (3PSW) Ethernet subsystem which supports dual gigabit media independent interface (GMII), reduced gigabit media independent interface (RGMII), reduced media independent interface (RMII), and Physical Layer (PHY) device management. For more information, please consult the AM335x device datasheets and Technical Reference Manual. Note that the Ethernet pins are shared with other peripherals.

4.18 GPIO

Most of the pins connected to the AM335x processor can be configured as General Purpose Input/Output (GPIO) pins. The Pin Function Table in the Appendix defines which pins can be configured as a GPIO pin and the GPIO register/bit they are associated with.

5 Mechanical Requirements

The following sections describe some of the mechanical requirements of incorporating a MityARM-335x module into a board design.

5.1 Module Connectors

The module has a single connector that contains all of the power and I/O for the module. The mating socket is a standard 204 position SODIMM connector that is commonly used for DDR3 memory modules. Example connectors are the JAE Electronics MM80-204B1-E1 (9.2mm height) and MM80-204B1-1 (5.2mm height) connectors that are available from DigiKey. There are many variants of this connector that allow the module to be positioned vertically, horizontally, or even stacked. Most of the connectors of this style are rated for approximately 25 insertions. Yamaichi Electronics makes a connector for this module that is rated for 10,000 insertions (p/n IC-657-9) that would be suitable for test fixtures, burn in sockets, or any other application that would require frequently changing the module.

5.2 Module Clearance – Horizontal Mount

The MityARM-335x module uses a SO-DIMM style main interface connector for electrical and mechanical attachment to the carrier board. This style of connector positions the MityARM-335x module in parallel with the carrier board, and as such there is limited clearance between the module and the carrier board. Therefore it is impossible to place high-profile carrier board components underneath the MityARM-335x module. However, it is possible to utilize most of this space for low-profile components. Please refer to the following diagrams and tables for module-specific clearances. Note that this configuration is based on the JAE Electronics MM80-204B1-E1 (9.2mm height) connector. Dimensions may have to be adjusted if other connectors are used. As shown a keep-out height of 3.00mm from the top of the module is recommended and a 2.00mm keep-out on the bottom.

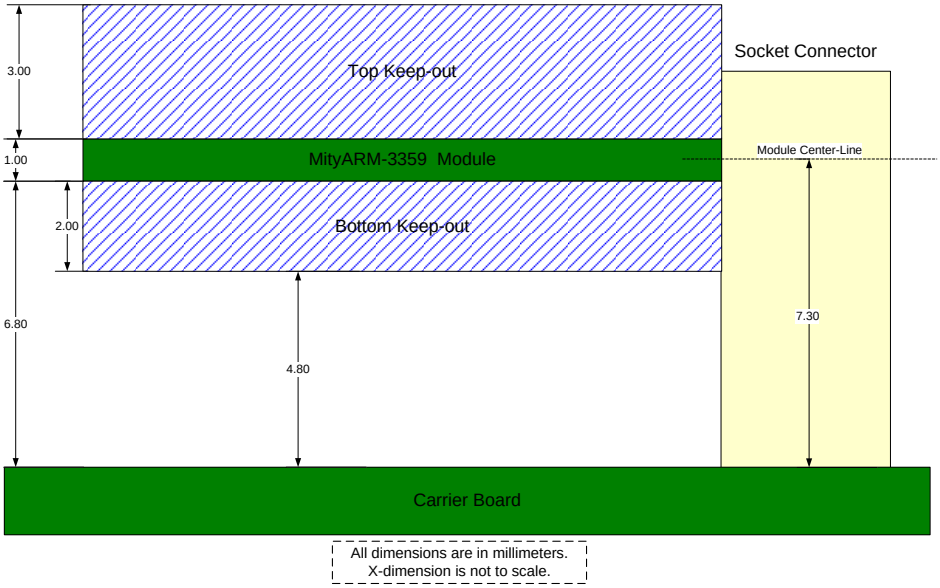

Figure 6: MityARM-335x Module Clearance - Side View

5.3 Mounting Methods

The modules feature an additional optional mechanical attachment method. A hard mechanical attachment by board-to-board standoffs and screw hardware may be used to mount the module. The corners of the free-floating edge of the SoMs feature mounting holes that are compatible with 4-40 size mounting hardware. For details and dimensions of corresponding mounting hole placement on your carrier board please reference Section 6.5 of this document. The mechanical drawing in Figure 7 illustrates the mechanical requirements of this optional attachment method. Note that this configuration is based on the JAE Electronics MM80-204B1-E1 (9.2mm height) connector. Dimensions may have to be adjusted if other connectors are used.

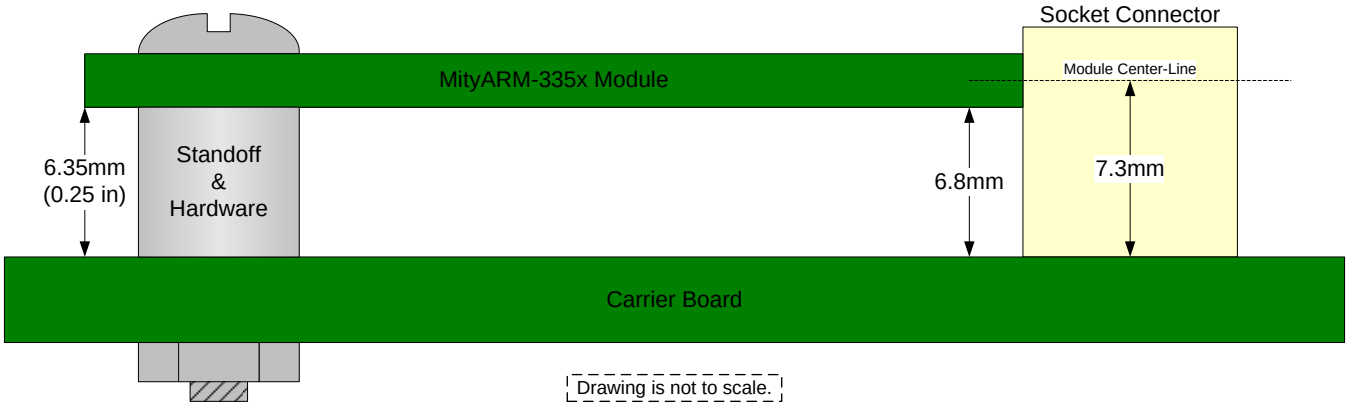

Figure 7: Hard Mounting the MityARM-335x

Table 6 shows the recommended hardware installation order and example part numbers from McMaster-Carr for each component listed. The standoff is slightly shorter than the socket, which puts a very slight downward tilt on the module, allowing the latching rails to engage correctly. This is normal and should not cause any stress to the board. Note that it is also possible to use a screw, spacer and a self-clinching nut (PEM) that is inserted into the carrier board mounting holes, please contact Critical Link for details about utilizing this option.

Table 6: Mounting hardware installation

Installation Order	Description	McMaster Carr PN
1	Screw, 4-40 x 1/4"	90272A106
2	Washer, Lock, No. 4	91102A720
3	Washer, Flat, No. 4	90126A505
4	MityARM-335x PCB	-
5	Standoff, 4-40, M-F	93505A101
6	Carrier Board PCB	-
7	Washer, Lock, No. 4	91102A720
8	Nut, 4-40 (Loctite recommended)	90480A005

Shock & Vibration

For customers who are interested in using MityARM-335x modules in rugged environments, the optional mechanical attachment methods discussed in section 5.3 enable MityARM-335x modules to tolerate much greater mechanical shock and vibration forces than without any additional mounting support.

5.4 Thermal Management

The MityARM-335x has no specific requirements regarding thermal management. The modules can be operated without heat sinks or air flow, and inside tight enclosures. However, if a module is intended to be used in hot industrial environments, it is advisable to do plenty of testing in the enclosure and environment that the module will be used in. In these cases, it may be necessary to either add thermal management to the enclosure, or lower the operating temperature specification of the end product.

6 Board Layout Recommendations

The following sections discuss topics for successful board layouts incorporating any module.

6.1 Placement

Placement of the module site is crucial to a successful carrier board layout. Because the module connector footprint is fine-pitch and dual-row, it is generally best to place the connector fairly centered in the overall board layout. This placement allows traces to be routed out from both sides of the connector, using mainly top-side copper tracks. The use of less signal layers, and therefore less vias, generally results in a more compact design with better signal integrity than a board using many layers and vias. Of course, ideally central placement is not always possible because of other mechanical constraints.

Mechanically, enough space must be allocated for the full extension of the module. Although it is possible for a module to hang over the edge of its carrier board, this may not be desirable if additional mechanical attachment methods are desired for ruggedness, as discussed in sections 5.3 and 0. Another thing to keep in mind with placement on the carrier board and in enclosures is the cam-in action of the MityARM modules into their respective sockets. The modules are generally installed at an angle of about 25° to 30° before swinging down to locked position. Enclosure designs should accommodate this motion.

6.2 Pin-out and Routing

Care must be taken when routing the MityARM-335x high speed interfaces – specifically the USB 2.0 OTG ports and the gigabit Ethernet ports. Please refer to the specific device specification for guidance related to these pins.

6.3 Access issues

Given that it is possible and often desirable to make best use of available space by placing components underneath the MityARM module (refer to section 5.2), hardware and software engineers who will be debugging code on the platform could find themselves in a tough situation if the component they need to access is blocked by the installed MityARM-335x module. Because of these situations it is advisable to either not use the space under the MityARM module for active components that might need live probing with the MityARM in-circuit, or only place circuits there that are already tried and tested by engineers on other platforms. In the event that an obscured circuit does need to be probed, it may be necessary to solder temporary wires onto probe points. An even better solution would be to design the board with bottom-side test points, at least in the MityARM region, if this is possible on a given design.

6.4 PCB/PCA Technology

The MityARM module does not have any specific requirements about the PCB technology used for its carrier board. The required socket connectors are available as RoHS compliant, and may be used in both leaded and lead-free assembly processes. The only recommendation is to fabricate the carrier board thick enough to rigidly support the MityARM socket connector. In practice, FR-4 with a common finished thickness of 0.062 inches is enough for all types of MityARM modules.

6.5 PCB Footprints

A drawing, Figure 8, of the recommended PCB footprint for the JAE MM80-204B1-E1 connector is shown below. This drawing should include all measurements to ensure that a proper footprint for the SO-DIMM module connector is created. We recommend that the two mounting holes be added to this footprint so they are placed properly on your carrier board. Figure 9 shows the necessary dimensions to properly place the mounting holes for the module.

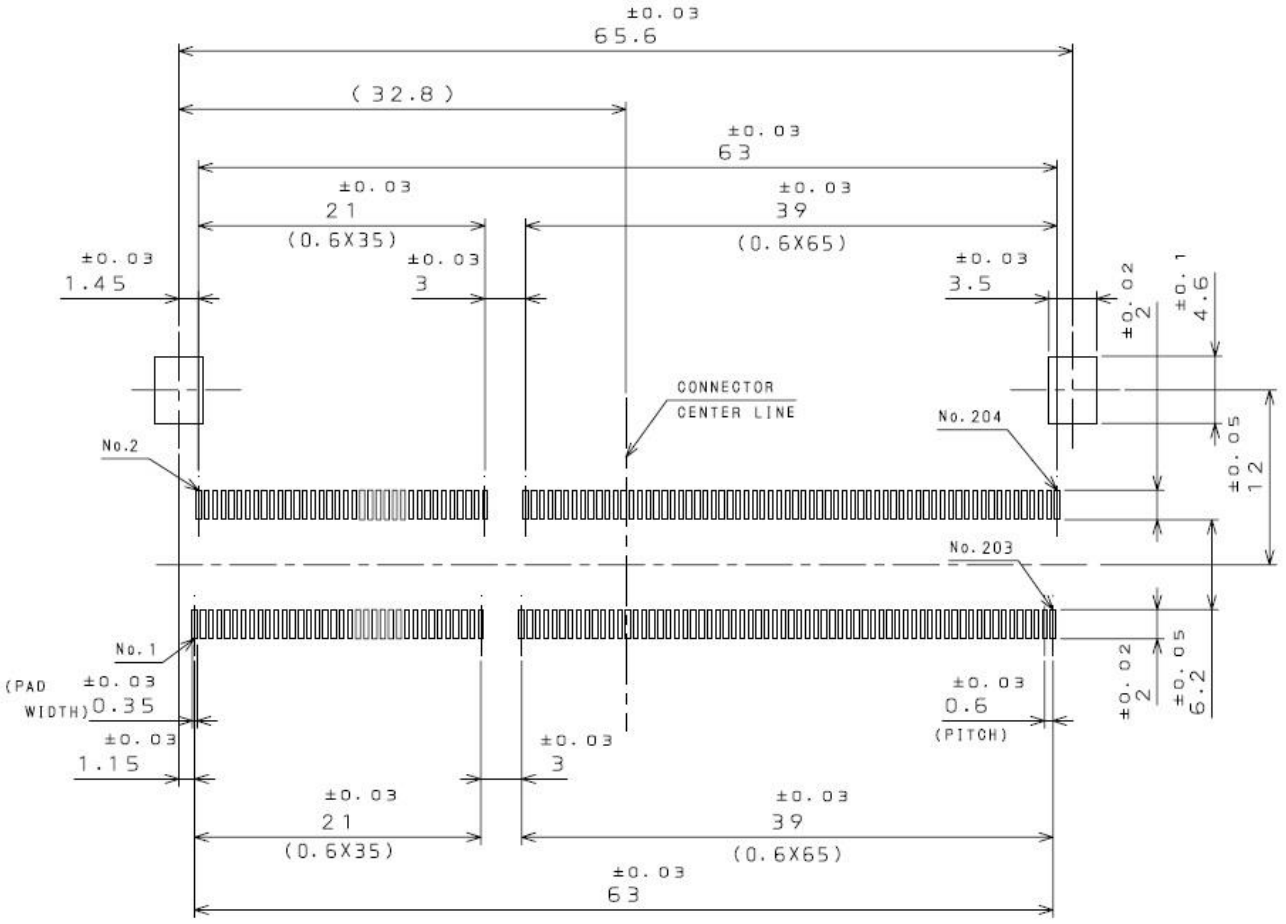

Figure 8: MM80-204B1-E1 Recommended PCB Footprint

Note: Pin 1 is 31.65mm from the connector center line and Pin 2 is 31.35mm from the connector center line.

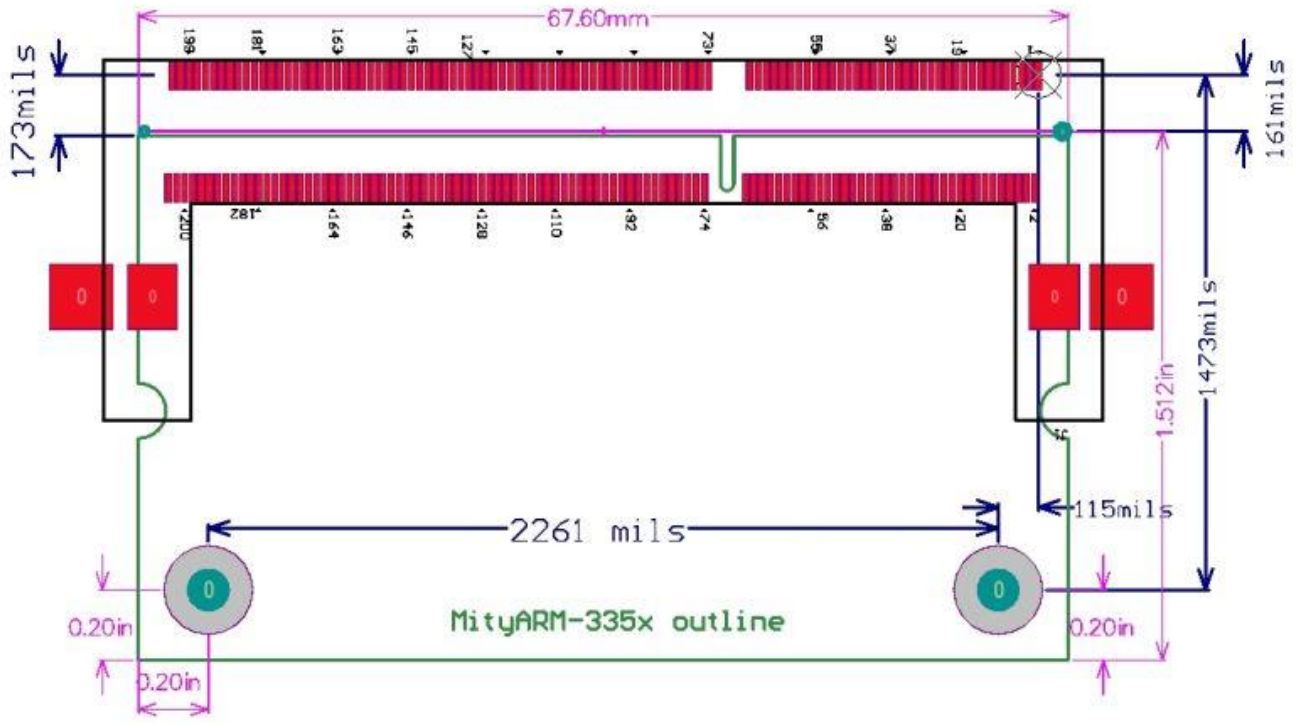

Figure 9: MityARM-335x Mounting Hole Locations

Note: These dimensions are in reference to the center of Pin 1.

7 Revision History

Revision	Date	Description of Changes
1.0	12-December-2011	Initial Revision
1.1	8-January-2012	Review updates
1.2	1-October-2012	Update Figure 6 with image showing centerline to edge dimension.
1.3	27-March-2013	Mounting options and available connectors updated as well as module current usage information.
1.4	23-April-2013	Update module keep-out clearances and remove note about SPI1 NOR flash boot capabilities.
1.5	30-September-2013	Update boot configuration pull up voltage net and add power-on sequencing and I/O protection sections.

8 Appendix

Table 7 contains a Pin Function Table that lists all the pins present on the SODIMM I/O connector and some characteristics of the pin including:

- Functional pin mapping options
- Voltage domain information (where applicable)
- Mapping of pins to the AM335x SOC and TPS65910 PMIC
- Class of Pin defined as:
    - Power (PWR)
    - Dedicated signals mapped to the on-board Power Management device (PM)
    - Dedicated signals mapped to the AM3359ZCZ device (335D)
    - Multi-function signals mapped to the AM3359ZCZ device (335M)
- Not all signals/mux options are available with all AM335x processor options (i.e. PRU's)
- The I2C1 and I2C2 interface signals/mux options cannot be changed as they are used for dedicated functions on the MityARM-335x module

Table 7 MityARM-335x Pin Function Table

PIN	Class	Signal	PMIC Pin	AM335x Pin	Power	Pin	Pin	Pin	Pin	Pin	Pin	Pin	Pin
1	PWR	VIN	-	-	-								
2	PWR	GND	-	-	-								
3	PWR	VIN	-	-	-								
4	PWR	GND	-	-	-								
5	PWR	VIN	-	-	-								
6	PWR	GND	-	-	-								
7	PWR	VIN	-	-	-								

PIN	Class	Signal	PMIC Pin	AM335x Pin	Power	Pin	Pin	Pin	Pin	Pin	Pin	Pin	Pin
8	PWR	GND	-	-	-								
9	PWR	VIN	-	-	-								
10	PWR	GND	-	-	-								
11	PWR	VIN	-	-	-								
12	PWR	GND	-	-	-								
13	PWR	VIN	-	-	-								
14	PWR	GND	-	-	-								
15	PWR	VIN	-	-	-								
16	PWR	GND	-	-	-								
17	PWR	GND	-	-	-								
18	PWR	GND	-	-	-								
19	PWR	GND	-	-	-								
20	PWR	GND	-	-	-								
21	PWR	VIO_3P3	-	-	-								
22	PWR	VIO_1P8	-	-	-								
23	PWR	VIO_3P3	-	-	-								
24	PWR	VIO_1P8	-	-	-								
25	PWR	VIO_3P3	-	-	-								
26	PWR	VIO_1P8	-	-	-								
27	PWR	VIO_3P3	-	-	-								
28	PWR	VIO_1P8	-	-	-								
29	335M	LCD_DATA0	-	R1	3.3V	lcd_data0	gpmc_a0	pr1_mii_mt0_clk	ehrpwm2A	pr1_pru1_pru_r30_0	pr1_pru1_pru_r31_0	gpio2_6	
30	PWR	LED_RTN	-	-									
31	335M	LCD_DATA1	-	R2	3.3V	lcd_data1	gpmc_a1	pr1_mii0_txen	ehrpwm2B	pr1_pru1_pru_r30_1	pr1_pru1_pru_r31_1	gpio2_7	
32	PM	PWR_ON	33	-	3.3V								
33	335M	LCD_DATA2	-	R3	3.3V	lcd_data2	gpmc_a2	pr1_mii0_txd3	ehrpwm2_tripzone input	pr1_pru1_pru_r30_2	pr1_pru1_pru_r31_2	gpio2_8	
34	PWR	VBACKUP	27	-									
35	335M	LCD_DATA3	-	R4	3.3V	lcd_data3	gpmc_a3	pr1_mii0_txd2	ehrpwm0_synco	pr1_pru1_pru_r30_3	pr1_pru1_pru_r31_3	gpio2_9	
36	PM	PMIC_SLEEP	37	-	3.3V								
37	PWR	GND	-	-	-								

PIN	Class	Signal	PMIC Pin	AM335x Pin	Power	Pin	Pin	Pin	Pin	Pin	Pin	Pin	Pin
38	PWR	GND	-	-	-								
39	335M	LCD_DATA4	-	T1	3.3V	lcd_data4	gpmc_a4	pr1_mii0_txd1	eQEP2A_in	pr1_pru1_pru_r30_4	pr1_pru1_pru_r31_4	gpio2_10	
40	PWR	GND	-	-	-								
41	335M	LCD_DATA5	-	T2	3.3V	lcd_data5	gpmc_a5	pr1_mii0_txd0	eQEP2B_in	pr1_pru1_pru_r30_5	pr1_pru1_pru_r31_5	gpio2_11	
42	PWR	GND	-	-	-								
43	335M	LCD_DATA6	-	T3	3.3V	lcd_data6	gpmc_a6	pr1_edio_data_in6	eQEP2_index	pr1_edio_data_out6	pr1_pru1_pru_r30_6	pr1_pru1_pru_r31_6	gpio2_12
44	PWR	VDDS_HV2	-	P10	VDDSHV2	VDDSHV2							
45	335M	LCD_DATA7	-	T4	3.3V	lcd_data7	gpmc_a7	pr1_edio_data_in7	eQEP2_strobe	pr1_edio_data_out7	pr1_pru1_pru_r30_7	pr1_pru1_pru_r31_7	gpio2_13
46	PWR	VDDS_HV2	-	P11	VDDSHV2	VDDSHV2							
47	335M	LCD_DATA8	-	U1	3.3V	lcd_data8	gpmc_a12	ehrpwm1_tripzone_input	mcasp0_aclkx	uart5_txd	pr1_mii0_rxd3	uart2_ctsn	gpio2_14
48	PWR	VDDS_HV4	-	H14	VDDSHV4	VDDSHV4							
49	335M	LCD_DATA9	-	U2	3.3V	lcd_data9	gpmc_a13	ehrpwm0_synco	mcasp0_fsx	uart5_rxd	pr1_mii0_rxd2	uart2_rtsn	gpio2_15
50	PWR	VDDS_HV4	-	J14	VDDSHV4	VDDSHV4							
51	335M	LCD_DATA10	-	U3	3.3V	lcd_data10	gpmc_a14	ehrpwm1A	mcasp0_axr0	pr1_mii0_rxd1	uart3_ctsn	gpio2_16	
52	PM	PMIC_INT_N	45	-	3.3V								
53	335M	LCD_DATA11	-	U4	3.3V	lcd_data11	gpmc_a15	ehrpwm1B	mcasp0_ahclkr	mcasp0_axr2	pr1_mii0_rxd0	uart3_rtsn	gpio2_17
54	PWR	GND	-	-	-								
55	PWR	GND	-	-	-								
56	PWR	GND	-	-	-								
57	335M	LCD_DATA12	-	V2	3.3V	lcd_data12	gpmc_a16	eQEP1A_in	mcasp0_aclkr	mcasp0_axr2	pr1_mii0_rxlink	uart4_ctsn	gpio0_8
58	335M	GPMC_A0	-	R13	3.3V	gpmc_a0	gmii2_txen	rgmii2_tctl	rmii2_txen	gpmc_a16	pr1_mii_mt1_clk	ehrpwm1_tripzone_input	gpio1_16
59	335M	LCD_DATA13	-	V3	3.3V	lcd_data13	gpmc_a17	eQEP1B_in	mcasp0_fsr	mcasp0_axr3	pr1_mii0_rxer	uart4_rtsn	gpio0_9
60	335M	GPMC_A1	-	V14	3.3V	gpmc_a1	gmii2_rxdv	rgmii2_rctl	mmc2_dat0	gpmc_a17	pr1_mii1_txd3	ehrpwm0_synco	gpio1_17
61	335M	LCD_DATA14	-	V4	3.3V	lcd_data14	gpmc_a18	eQEP1_index	mcasp0_axr1	uart5_rxd	pr1_mii_mr0_clk	uart5_ctsn	gpio0_10
62	335M	GPMC_A2	-	U14	3.3V	gpmc_a2	gmii2_txd3	rgmii2_td3	mmc2_dat1	gpmc_a18	pr1_mii1_txd2	ehrpwm1A	gpio1_18
63	335M	LCD_DATA15	-	T5	3.3V	lcd_data15	gpmc_a19	eQEP1_strobe	mcasp0_ahclkx	mcasp0_axr3	pr1_mii0_rxdv	uart5_rtsn	gpio0_11
64	335M	GPMC_A3	-	T14	3.3V	gpmc_a3	gmii2_txd2	rgmii2_td2	mmc2_dat2	gpmc_a19	pr1_mii1_txd1	ehrpwm1B	gpio1_19
65	335M	LCD_PCLK	-	V5	3.3V	lcd_pclk	gpmc_a10	pr1_mii0_crs	pr1_edio_data_in4	pr1_edio_data_out4	pr1_pru1_pru_r30_10	pr1_pru1_pru_r31_10	gpio2_24
66	335M	GPMC_A4	-	R14	3.3V	gpmc_a4	gmii2_txd1	rgmii2_td1	rmii2_txd1	gpmc_a20	pr1_mii1_txd0	eQEP1A_in	gpio1_20
67	335M	LCD_VSYNC	-	U5	3.3V	lcd_vsync	gpmc_a8	pr1_edio_data_in2	pr1_edio_data_out2	pr1_pru1_pru_r30_8	pr1_pru1_pru_r31_8	gpio2_22	

PIN	Class	Signal	PMIC Pin	AM335x Pin	Power	Pin	Pin	Pin	Pin	Pin	Pin	Pin	Pin
68	335M	GPMC_A5	-	V15	3.3V	gpmc_a5	gmii2_txd0	rgmii2_td0	rmii2_txd0	gpmc_a21	pr1_mii1_rxd3	eQEP1B_in	gpio1_21
69	335M	LCD_HSYNC	-	R5	3.3V	lcd_hsync	gpmc_a9	pr1_edio_data_in3	pr1_edio_data_out3	pr1_pru1_pru_r309	pr1_pru1_pru_r31_9	gpio2_23	
70	335M	GPMC_A6	-	U15	3.3V	gpmc_a6	gmii2_txclk	rgmii2_tclk	mmc2_dat4	gpmc_a22	pr1_mii1_rxd2	eQEP1_index	gpio1_22
71	335M	LCD_AC_BIAS_EN	-	R6	3.3V	lcd_ac_bias_en	gpmc_a11	pr1_mii1_crs	pr1_edio_data_in5	pr1_edio_data_out5	pr1_pru1_pru_r30_11	pr1_pru1_pru_r3111	gpio2_25
72	335M	GPMC_A7	-	T15	3.3V	gpmc_a7	gmii2_rxclk	rgmii2_rclk	mmc2_dat5	gpmc_a23	pr1_mii1_rxd1	eQEP1_strobe	gpio1_23
73	PWR	GND	-	-	-								
74	PWR	GND	-	-	-								
75	335D	GPMC_AD0	-	U7	3.3V	gpmc_ad0							
76	335M	GPMC_A8	-	V16	3.3V	gpmc_a8	gmii2_rxd3	rgmii2_rd3	mmc2_dat6	gpmc_a24	pr1_mii1_rxd0	mcasp0_aclkx	gpio1_24
77	335D	GPMC_AD1	-	V7	3.3V	gpmc_ad1							
78	335M	GPMC_A9	-	U16	3.3V	gpmc_a9	gmii2_rxd2	rgmii2_rd2	mmc2_dat7	gpmc_a25	pr1_mii_mr1_clk	mcasp0_fsx	gpio1_25
79	335D	GPMC_AD2	-	R8	3.3V	gpmc_ad2							
80	335M	GPMC_A10	-	T16	3.3V	gpmc_a10	gmii2_rxd1	rgmii2_rd1	rmii2_rxd1	gpmc_a26	pr1_mii1_rxdv	mcasp0_axr0	gpio1_26
81	335D	GPMC_AD3	-	T8	3.3V	gpmc_ad3							
82	335M	GPMC_A11	-	V17	3.3V	gpmc_a11	gmii2_rxd0	rgmii2_rd0	rmii2_rxd0	gpmc_a27	pr1_mii1_rxer	mcasp0_axr1	gpio1_27
83	335D	GPMC_AD4	-	U8	3.3V	gpmc_ad4							
84	335M	GPMC_CLK	-	V12	VDDSHV2	gpmc_clk	lcd_memory_clk	gpmc_wait1	mmc2_clk	pr1_mii1_crs	pr1_mdio_mdclk	mcasp0_fsr	gpio2_1
85	335D	GPMC_AD5	-	V8	3.3V	gpmc_ad5							
86	335D	GPMC_BEN0_CLE	-	T6	3.3V	gpmc_be0n_cle							
87	335D	GPMC_AD6	-	R9	3.3V	gpmc_ad6							
88	335D	GPMC_ADVN_ALE	-	R7	3.3V	gpmc_advn_ale							
89	335D	GPMC_AD7	-	T9	3.3V	gpmc_ad7							
90	335D	GPMC_OEN_RE_N	-	T7	3.3V	gpmc_oen_ren							
91	PWR	GND	-	-	-								
92	PWR	GND	-	-	-								
93	335M	GPMC_AD8	-	U10	VDDSHV2	gpmc_ad8	lcd_data23	mmc1_dat0	mmc2_dat4	ehrpwm2A	pr1_mii_mt0_clk	gpio0_22	
94	335M	GPMC_CSN3	-	T13	VDDSHV2	gpmc_csn3	mmc2_cmd	pr1_mii0_crs	pr1_mdio_data	EMU4	gpio2_0		
95	335M	GPMC_AD9	-	T10	VDDSHV2	gpmc_ad9	lcd_data22	mmc1_dat1	mmc2_dat5	ehrpwm2B	pr1_mii0_col	gpio0_23	
96		No Connect											
97	335M	GPMC_AD10	-	T11	VDDSHV2	gpmc_ad10	lcd_data21	mmc1_dat2	mmc2_dat6	ehrpwm2_tripzone input	pr1_mii0_txen	gpio0_26	

PIN	Class	Signal	PMIC Pin	AM335x Pin	Power	Pin	Pin	Pin	Pin	Pin	Pin	Pin	Pin
98	335D	GPMC_WE_N	-	U6	3.3V	gpmc_wen							
99	335M	GPMC_AD11	-	U12	VDDSHV2	gpmc_ad11	lcd_data20	mmc1_dat3	mmc2_dat7	ehrpwm0_synco	pr1_mii0_txd3	gpio0_27	
100	335D	GPMC_WAIT0	-	T17	3.3V	gpmc_wait0							
101	335M	GPMC_AD12	-	T12	VDDSHV2	gpmc_ad12	lcd_data19	mmc1_dat4	mmc2_dat0	eQEP2A_in	pr1_mii0_txd2	pr1_pru0_pru_r3014	gpio1_12
102	335M	GPMC_BEN1	-	U18	3.3V	gpmc_be1n	gmii2_col	gpmc_csn6	mmc2_dat3	gpmc_dir	pr1_mii1_rxlink	mcasp0_aclkr	gpio1_28
103	335M	GPMC_AD13	-	R12	VDDSHV2	gpmc_ad13	lcd_data18	mmc1_dat5	mmc2_dat1	eQEP2B_in	pr1_mii0_txd1	pr1_pru0_pru_r3015	gpio1_13
104	335D	GPMC_WP_N	-	U17	3.3V	gpmc_wpn							
105	335M	GPMC_AD14	-	V13	VDDSHV2	gpmc_ad14	lcd_data17	mmc1_dat6	mmc2_dat2	eQEP2_index	pr1_mii0_txd0	pr1_pru0_pru_r3114	gpio1_14
106		No Connect											
107	335M	GPMC_AD15	-	U13	VDDSHV2	gpmc_ad15	lcd_data16	mmc1_dat7	mmc2_dat3	eQEP2_strobe	pr1_ecap0_ecap_capinapwm_o	pr1_pru0_pru_r3115	gpio1_15
108		No Connect											
109	PWR	GND	-	-	-								
110	PWR	GND	-	-	-								
111	335M	GPMC_CSN2	-	V9	3.3V	gpmc_csn2	gpmc_be1n	mmc1_cmd	pr1_edio_data_in7	pr1_edio_data_out7	pr1_pru1_pru_r30_13	pr1_pru1_pru_r3113	gpio1_31
112	335M	GMII1_RXD0	-	M16	3.3V	gmii1_rxd0	rmii1_rxd0	rgmii1_rd0	mcasp1_ahclkx	mcasp1_ahclkr	mcasp1_aclkr	mcasp0_axr3	gpio2_21
113	335M	GPMC_CSN1	-	U9	3.3V	gpmc_csn1	gpmc_clk	mmc1_clk	pr1_edio_data_in6	pr1_edio_data_out6	pr1_pru1_pru_r30_12	pr1_pru1_pru_r3112	gpio1_30
114	335M	GMII1_RXD1	-	L15	3.3V	gmii1_rxd1	rmii1_rxd1	rgmii1_rd1	mcasp1_axr3	mcasp1_fsr	eQEP0_strobe	mmc2_clk	gpio2_20
115	335D	USB0_VBUS	-	P15		USB0_VBUS							
116	335M	GMII1_RXD2	-	L16	3.3V	gmii1_rxd2	uart3_txd	rgmii1_rd2	mmc0_dat4	mmc1_dat3	uart1_rin	mcasp0_axr1	gpio2_19
117	335D	USB0_ID	-	P16		USB0_ID							
118	335M	GMII1_RXD3	-	L17	3.3V	gmii1_rxd3	uart3_rxd	rgmii1_rd3	mmc0_dat5	mmc1_dat2	uart1_dtrn	mcasp0_axr0	gpio2_18
119	335D	USB1_VBUS	-	T18		USB1_VBUS							
120	335M	GMII1_RXCLK	-	L18	3.3V	gmii1_rxclk	uart2_txd	rgmii1_rclk	mmc0_dat6	mmc1_dat1	uart1_dsrn	mcasp0_fsx	gpio3_10
121	335D	USB1_DP	-	R17		USB1_DP							
122	335M	GMII1_RXDV	-	J17	3.3V	gmii1_rxdv	lcd_memory_clk	rgmii1_rctl	uart5_txd	mcasp1_aclkx	mmc2_dat0	mcasp0_aclkr	gpio3_4
123	335D	USB1_DM	-	R18		USB1_DM							
124		No Connect											
125	335D	USB1_CE	-	P18		USB1_CE							
126	335M	GMII1_TXCLK	-	K18	3.3V	gmii1_txclk	uart2_rxd	rgmii1_tclk	mmc0_dat7	mmc1_dat0	uart1_dcdn	mcasp0_aclkx	gpio3_9
127	PWR	GND	-	-	-								

PIN	Class	Signal	PMIC Pin	AM335x Pin	Power	Pin	Pin	Pin	Pin	Pin	Pin	Pin	Pin
128	335M	GMII1_TXD0	-	K17	3.3V	gmii1_txd0	rmii1_txd0	rgmii1_td0	mcasp1_axr2	mcasp1_aclkr	eQEP0B_in	mmc1_clk	gpio0_28
129	335D	USB1_ID	-	P17		USB1_ID							
130	335M	GMII1_TXD1	-	K16	3.3V	gmii1_txd1	rmii1_txd1	rgmii1_td1	mcasp1_fsr	mcasp1_axr1	eQEP0A_in	mmc1_cmd	gpio0_21
131	335D	USB0_DM	-	N18		USB0_DM							
132	335M	GMII1_TXD2	-	K15	3.3V	gmii1_txd2	dcan0_rx	rgmii1_td2	uart4_txd	mcasp1_axr0	mmc2_dat2	mcasp0_ahclkx	gpio0_17
133	335D	USB0_DP	-	N17		USB0_DP							
134	335M	GMII1_TXD3	-	J18	3.3V	gmii1_txd3	dcan0_tx	rgmii1_td3	uart4_rxd	mcasp1_fsx	mmc2_dat1	mcasp0_fsr	gpio0_16
135	335D	USB0_CE	-	M15		USB0_CE							
136	335M	GMII1_TXEN	-	J16	3.3V	gmii1_txen	rmii1_txen	rgmii1_tctl	timer4	mcasp1_axr0	eQEP0_index	mmc2_cmd	gpio3_3
137	335M	USB1_DRVVBUS	-	F15	3.3V	USB1_DRVVBUS	gpio3_13						
138	335M	GMII1_COL	-	H16	3.3V	gmii1_col	rmii2_refclk	spi1_sclk	uart5_rxd	mcasp1_axr2	mmc2_dat3	mcasp0_axr2	gpio3_0
139	335M	USB0_DRVVBUS	-	F16	3.3V	USB0_DRVVBUS	gpio0_18						
140		No Connect											
141	335M	MDC	-	M18	3.3V	mdio_clk	timer5	uart5_txd	uart3_rtsn	mmc0_sdwp	mmc1_clk	mmc2_clk	gpio0_1
142		No Connect											
143	335M	MDIO	-	M17	3.3V	mdio_data	timer6	uart5_rxd	uart3_ctsn	mmc0_sdcd	mmc1_cmd	mmc2_cmd	gpio0_0
144	335M	MCASP0_AXR1	-	D13	3.3V	mcasp0_axr1	eQEP0_index	mcasp1_axr0	EMU3	pr1_pru0_pru_r30_6	pr1_pru0_pru_r31_6	gpio3_20	
145	335M	RMII1_REFCLK	-	H18	3.3V	rmii1_refclk	xdma_event_intr2	spi1_cs0	uart5_txd	mcasp1_axr3	mmc0_pow	mcasp1_ahclkx	gpio0_29
146	PWR	GND	-	-	-								
147	335D	I2C1_SDA	-	H17	3.3V	I2C1_SDA							
148	335M	MCASP0_FSR	-	C13	3.3V	mcasp0_fsr	eQEP0B_in	mcasp0_axr3	mcasp1_fsx	EMU2	pr1_pru0_pru_r30_5	pr1_pru0_pru_r31_5	gpio3_19
149	335D	I2C1_SCL	-	J15	3.3V	I2C1_SCL							
150	335M	MCASP0_ACLKR	-	B12	3.3V	mcasp0_aclkr	eQEP0A_in	mcasp0_axr2	mcasp1_aclkx	mmc0_sdwp	pr1_pru0_pru_r30_4	pr1_pru0_pru_r31_4	gpio3_18
151	335M	MMC0_CMD	-	G18	VDDSHV4	mmc0_cmd	gpmc_a25	uart3_rtsn	uart2_txd	dcan1_rx	pr1_pru0_pru_r30_13	pr1_pru0_pru_r31_13	gpio2_31
152	335M	MCASP0_ACLKX	-	A13	3.3V	mcasp0_aclkx	ehrpwm0A	spi1_sclk	mmc0_sdcd	pr1_pru0_pru_r30_0	pr1_pru0_pru_r31_0	gpio3_14	
153	335M	MMC0_CLK	-	G17	VDDSHV4	mmc0_clk	gpmc_a24	uart3_ctsn	uart2_rxd	dcan1_tx	pr1_pru0_pru_r30_12	pr1_pru0_pru_r31_12	gpio2_30
154	335M	MCASP0_AHCLKX	-	A14	3.3V	mcasp0_ahclkx	eQEP0_strobe	mcasp0_axr3	mcasp1_axr1	EMU4	pr1_pru0_pru_r30_7	pr1_pru0_pru_r31_7	gpio3_21
155	335M	MMC0_DAT0	-	G16	VDDSHV4	mmc0_dat0	gpmc_a23	uart5_rtsn	uart3_txd	uart1_rin	pr1_pru0_pru_r30_11	pr1_pru0_pru_r31_11	gpio2_29
156	335D	EXTINT_N	-	B18	3.3V	nNMI							
157	335M	MMC0_DAT1	-	G15	VDDSHV4	mmc0_dat1	gpmc_a22	uart5_ctsn	uart3_rxd	uart1_dtrn	pr1_pru0_pru_r30_10	pr1_pru0_pru_r31_10	gpio2_28

PIN	Class	Signal	PMIC Pin	AM335x Pin	Power	Pin	Pin	Pin	Pin	Pin	Pin	Pin	Pin
158	335D	WARMRST_N	-	A10	3.3V	nRESETIN_OUT							
159	335M	MMC0_DAT2	-	F18	VDDSHV4	mmc0_dat2	gpmc_a21	uart4_rtsn	timer6	uart1_dsrn	pr1_pru0_pru_r30_9	pr1_pru0_pru_r31_9	gpio2_27
160	335M	EMU0	-	C14	3.3V	EMU0	gpio3_7						
161	335M	MMC0_DAT3	-	F17	VDDSHV4	mmc0_dat3	gpmc_a20	uart4_ctsn	timer5	uart1_dcdn	pr1_pru0_pru_r30_8	pr1_pru0_pru_r31_8	gpio2_26
162	335M	EMU1	-	B14	3.3V	EMU1	gpio3_8						
163	PWR	GND	-	-	-								
164	PWR	GND	-	-	-								
165	335M	UART0_CTSN	-	E18	3.3V	uart0_ctsn	uart4_rxd	dcan1_tx	I2C1_SDA	spi1_d0	timer7	pr1_edc_sync0_out	gpio1_8
166	335D	TCK	-	A12	3.3V	TCK							
167	335M	UART0_RTSN	-	E17	3.3V	uart0_rtsn	uart4_txd	dcan1_rx	I2C1_SCL	spi1_d1	spi1_cs0	pr1_edc_sync1_out	gpio1_9
168	335D	TDI	-	B11	3.3V	TDI							
169	335M	UART0_TXD	-	E16	3.3V	uart0_txd	spi1_cs1	dcan0_rx	I2C2_SCL	eCAP1_in_PWM1_out	pr1_pru1_pru_r30_15	pr1_pru1_pru_r31_15	gpio1_11
170	335D	TDO	-	A11	3.3V	TDO							
171	335M	UART0_RXD	-	E15	3.3V	uart0_rxd	spi1_cs0	dcan0_tx	I2C2_SDA	eCAP2_in_PWM2_out	pr1_pru1_pru_r30_14	pr1_pru1_pru_r31_14	gpio1_10
172	335D	TMS	-	C11	3.3V	TMS							
173	335M	UART1_RXD	-	D16	3.3V	uart1_rxd	mmc1_sdwp	dcan1_tx	I2C1_SDA	pr1_uart0_rxd	pr1_pru1_pru_r31_16	gpio0_14	
174	335D	TRSTN	-	B10	3.3V	nTRST							
175	335M	UART1_TXD	-	D15	3.3V	uart1_txd	mmc2_sdwp	dcan1_rx	I2C1_SCL	pr1_uart0_txd	pr1_pru0_pru_r31_16	gpio0_15	
176	PWR	VREFN	-	A9	1.8V	VREFN							
177	335M	I2C0_SDA	-	C17	3.3V	I2C0_SDA	timer4	uart2_ctsn	eCAP2_in_PWM2_out	gpio3_5			
178	PWR	VREFP	-	B9	1.8V	VREFP							
179	335M	I2C0_SCL	-	C16	3.3V	I2C0_SCL	timer7	uart2_rtsn	eCAP1_in_PWM1_out	gpio3_6			
180	335D	EXT_WAKEUP	-	C5	1.8V	EXT_WAKEUP							
181	PWR	GND	-	-	-								
182	PWR	GND	-	-	-								
183	335M	SPI0_D0	-	B17	3.3V	spi0_d0	uart2_txd	I2C2_SCL	ehrpwm0B	pr1_uart0_rts_n	pr1_edio_latch_in	EMU3	gpio0_3
184	335D	AIN0	-	B6	1.8V	AIN0							
185	335M	SPI0_D1	-	B16	3.3V	spi0_d1	mmc1_sdwp	I2C1_SDA	ehrpwm0_tripzone input	pr1_uart0_rxd	pr1_edio_data_in0	pr1_edio_data_out0	gpio0_4
186	335D	AIN1	-	C7	1.8V	AIN1							
187	335M	SPI0_SCLK	-	A17	3.3V	spi0_sclk	uart2_rxd	I2C2_SDA	ehrpwm0A	pr1_uart0_cts_n	pr1_edio_sof	EMU2	gpio0_2

PIN	Class	Signal	PMIC Pin	AM335x Pin	Power	Pin	Pin	Pin	Pin	Pin	Pin	Pin	Pin
188	335D	AIN2	-	B7	1.8V	AIN2							
189	335M	SPI0_CS1	-	C15	3.3V	spi0_cs1	uart3_rxd	eCAP1_in_PWM1_out	mmc0_pow	xdma_event_intr2	mmc0_sdcd	EMU4	gpio0_6
190	335D	AIN3	-	A7	1.8V	AIN3							
191	335M	SPI0_CS0	-	A16	3.3V	spi0_cs0	mmc2_sdwp	I2C1_SCL	ehrpwm0_synci	pr1_uart0_txd	pr1_edio_data_in1	pr1_edio_data_out1	gpio0_5
192	335D	AIN4	-	C8	1.8V	AIN4							
193	335D	SPI1_SCLK	-	C18	3.3V	spi1_sclk							
194	335D	AIN5	-	B8	1.8V	AIN5							
195	335D	SPI1_D0_MOSI	-	B13	3.3V	spi1_d0							
196	335D	AIN6	-	A8	1.8V	AIN6							
197	335D	SPI1_D1_MISO	-	D12	3.3V	spi1_d1							
198	335D	AIN7	-	C9	1.8V	AIN7							
199	PWR	GND	-	-	-								
200	PWR	GND	-	-	-								
201	335M	XDMA_EVENT_INTR1	-	D14	3.3V	xdma_event_intr1	tclkin	clkout2	timer7	pr1_pru0_pru_r31_16	EMU3	gpio0_20	
202	PWR	AGND	-	-	-								
203	335M	XDMA_EVENT_INTR0	-	A15	3.3V	xdma_event_intr0	timer4	clkout1	spi1_cs1	pr1_pru1_pru_r31_16	EMU2	gpio0_19	
204	PWR	AGND	-	-	-								