FEATURES

- Direct Interface to Critical Link's Industrial IO Development Kit
- Vision Sensor Boards Supported
  - 0.3MP Monochrome
  - 0.3MP Color
  - 1.0MP Monochrome
  - 5.0MP Monochrome
  - 5.0MP Color
  - Others available

APPLICATIONS

- Machine Vision
- Quality Control
- Semiconductor Inspection
- Image Processing (DSP and FPGA)

Expansion

- Dual +5V GPIO Enabled Outputs
- Dual +5V Servo Control Outputs
- 2 Red and 2 Green GPIO Status LED's
- GPIO Expansion Header with +3.3V

Overview

The Industrial Camera Expansion (80-000322) Board by Critical Link is an expansion that directly connects to the Critical Link Industrial IO Development Kit Baseboard that is powered by a MityDSP-L138F (A System on Module with FPGA is required). This expansion allows the connection for one of five sensor boards that Critical Link has designed and other custom sensors may be compatible, contact Critical Link for further details. This document will outline the HW specifications including features, electrical requirements and pin outs. All power supplies needed for this board are supplied through the Industrial IO Boards three 50-pin headers.

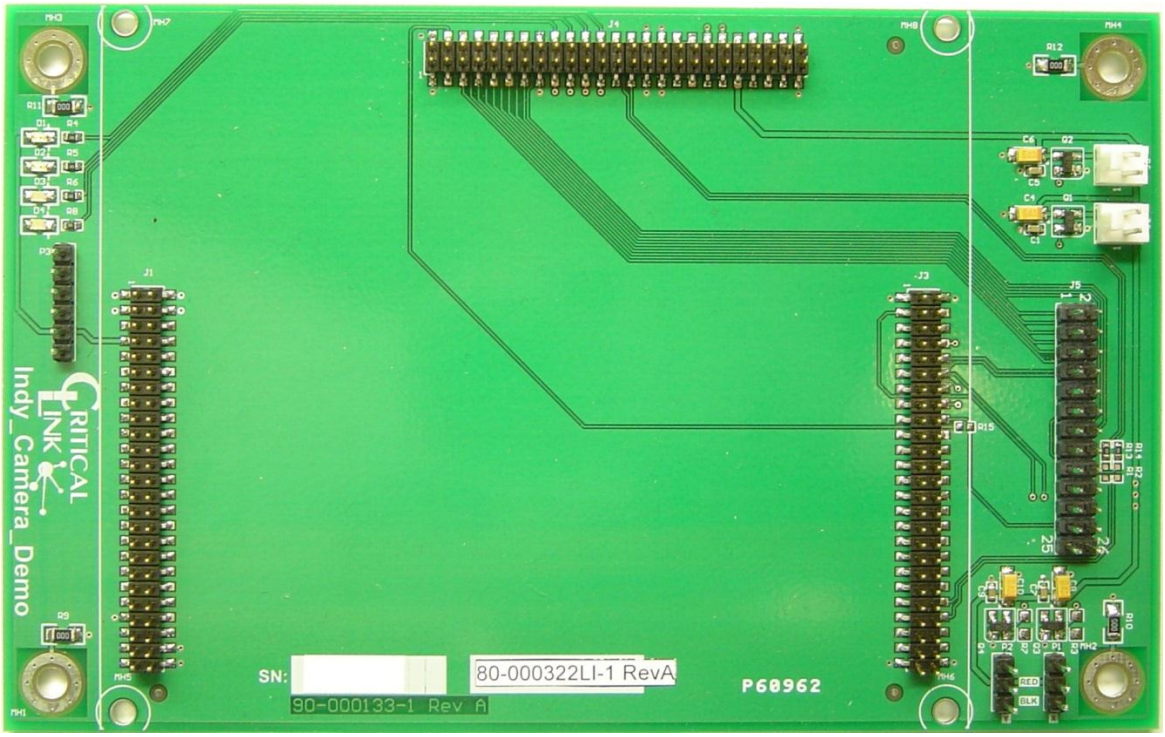

Figure 1 – Industrial Camera Expansion Board

Critical Link, LLC
6712 Brooklawn Parkway
Syracuse, NY 13211
PHONE 315.425.4045
FAX 315.425.4048
www.CriticalLink.com

FEATURE DESCRIPTIONS

Power Supplies

No external power supplies are needed for this expansion board. Both the +3.3V and +5V supplies are provided from the attached Industrial IO Development Kit through the three 50-pin headers.

Camera Interface

The 26-Pin header allows for the connection of a number of different sensor boards for evaluation and development. The sensor data signals are routed through this interface to the Industrial IO Development Kit and then to the FPGA of a MityDSP-L138F System on Module.

By utilizing a MityDSP-L138F SoM developers are able to generate vision algorithms at both the Xilinx Spartan 6 FPGA and TI C674x DSP levels and then display those results in an application/GUI through the TI ARM9 applications processor.

GPIO Header

A header consisting of 4 individual General Purpose Input Output signals is also available on the expansion board. These signals are connected to the ARM9 GPIO signals of the SoM module. The header also contains a +3.3V pin and a GND pin to power a device or other expansion board if necessary.

4 General Purpose LEDS

A set of four LEDS, two red and two green, are provided for general usage. Each LED is controlled by a GPIO pin from the ARM9 GPIO signals of the SoM module.

Servo Motor Controls

There are two 3-pin servo motor controller headers on the expansion board that are controlled by the SoM FPGA. +5V and GND are provided through two of the pins and the other pin controls the servos movement through the FPGA GPIO.

+5V GPIO Controlled Pins

Two sets of 2-pin headers are provided that provide a FPGA controlled set of +5V and GND pins. Through the use of a GPIO an enable signal is created that when enabled connects the GND pin of the header to GND and when disabled floats the GND pin.

Expansion Headers to Industrial IO Board

These headers provide the interface to the Industrial IO Board that contains a MityDSP-L138 System on Module. Through the use of the MityDSP-L138 it is possible to utilize all of the above features in a Vision Development design.

Critical Link, LLC PHONE 315.425.4045
6712 Brooklawn Parkway FAX 315.425.4048
Syracuse, NY 13211 www.CriticalLink.com

ELECTRICAL INTERFACE DESCRIPTIONS

Power Supplies

No external power supply is necessary for the expansion board. It is powered by the Industrial IO board that it is connected to. Please see the following tables for information on which pins of the three 50-pin headers provide power for the expansion board: Table 9, Table 10 and Table 11.

Camera Interface – J5

The Camera Interface connector, J5, allows for one of five camera sensors from Critical Link to be connected. All of these sensors options are compatible with this connector.

- 0.3MP Monochrome
- 0.3MP Color
- 1.0MP Monochrome
- 5.0MP Monochrome
- 5.0MP Color

Other custom sensor options may be available, please contact Critical Link for details.

Table 1: J5 Camera Sensor Interface Pin Description

Pin	Schematic Signal	Expansion Header	Type	Standard	Notes
1	D2	J4 Pin 10	I/O	3.3V LVCMOS	
2	D3	J4 Pin 9	I/O	3.3V LVCMOS	
3	D4	J4 Pin 8	I/O	3.3V LVCMOS	
4	D5	J4 Pin 7	I/O	3.3V LVCMOS	
5	D6	J4 Pin 6	I/O	3.3V LVCMOS	
6	D7	J4 Pin 5	I/O	3.3V LVCMOS	
7	D8	J3 Pin 10	I/O	3.3V LVCMOS	
8	D9	J3 Pin 9	I/O	3.3V LVCMOS	
9	D0	J4 Pin 12	I/O	3.3V LVCMOS	
10	D1	J4 Pin 11	I/O	3.3V LVCMOS	
11	GND	-	Power	3.3V LVCMOS	
12	GND	-	Power	3.3V LVCMOS	
13	LV	J4 Pin 14	I/O	3.3V LVCMOS	
14	EXPOSURE	J3 Pin 11	I/O	3.3V LVCMOS	
15	Reserved	-	-	-	
16	Reserved	-	-	-	
17	FV	J4 Pin 13	I/O	3.3V LVCMOS	
18	I2C0_SDA	J4 Pin 28	I/O	3.3V LVCMOS	
19	I2C0_SCL	J4 Pin 27	I/O	3.3V LVCMOS	
20	Reserved	-	-	-	
21	+5V	-	Power	200mA max	Total external draw on 5V supply should not exceed 1000mA
22	+5V	-	Power	200mA max	Total external draw on 5V supply should not exceed 1000mA
23	PIXCLK	J3 Pin 18	I/O	3.3V LVCMOS	
24	GND	-	Power	-	
25	GND	-	Power	-	
26	Reserved	-	-	-	

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6712 Brooklawn Parkway
Syracuse, NY 13211
PHONE 315.425.4045
FAX 315.425.4048
www.CriticalLink.com

GPIO Header – P3

The GPIO header allows for 4 general purpose Inputs or Outputs, depending on implementation of the ARM9 SW design. Included are both +3.3V and GND signals on the header to power an external board/device.

Note that the GPIO signals are directly connected to the expansion header pins and do not have net names.

Table 2: P3 GPIO Header Pin Description

Pin	Schematic Signal	Expansion Header	Type	Standard	Notes
1	-	J4 Pin 17	I/O	3.3V LVCMOS	
2	-	J4 Pin 19	I/O	3.3V LVCMOS	
3	-	J4 Pin 21	I/O	3.3V LVCMOS	
4	-	J4 Pin 23	I/O	3.3V LVCMOS	
5	+3.3V	-	Power	-	
6	GND	-	Power	-	

LEDS – D1 through D4

A set of four LEDS are provided for general usage that are routed to ARM9 GPIO pins for control. The LED's are supplied with +3.3V and have 1.00K resistors in series with them making the GPIO signals active low.

Table 3: LED Pin Descriptions

LED	Schematic Signal	Expansion Header	Type	Standard	Notes
D1	LED 1	J4 Pin 24	O	3.3V LVCMOS	Red
D2	LED 2	J4 Pin 22	O	3.3V LVCMOS	Red
D3	LED 3	J4 Pin 20	O	3.3V LVCMOS	Green
D4	LED 4	J4 Pin 10	O	3.3V LVCMOS	Green

Critical Link, LLC
6712 Brooklawn Parkway
Syracuse, NY 13211
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FAX 315.425.4048
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Servo Motor Controls – P1 and P2

There are two servo motor controller headers which use a GPIO from the FPGA to control each, active high. +5V and GND connections are also provided. The servos are controlled by a MOSFET driver for the X or Y signal.

Table 4: P1 - X Servo Control Pin Description

Pin	Schematic Signal	Type	Standard	Notes
1	X	O	LVTTL	Controlled by Servo_X on J3 Pin 3
2	+5V	Power	-	Total external draw on 5V supply should not exceed 1000mA
3	GND	Power	-	

Table 5: P2 - Y Servo Control Pin Description

Pin	Schematic Signal	Type	Standard	Notes
1	Y	O	LVTTL	Controlled by Servo_Y on J3 Pin 12
2	+5V	Power	-	Total external draw on 5V supply should not exceed 1000mA
3	GND	Power	-	

+5V GPIO Controlled Pins – J2 and J6

Through the use of a MOSFET driver a FPGA GPIO can control the connection to ground (GND) on Pin 2 of these headers. Pin 1 is connected to the +5V supply.

Table 6: J2 Pin Descriptions

Pin	Schematic Signal	Type	Standard	Notes
1	+5V	Power	-	Total external draw on 5V supply should not exceed 1000mA
2	GND	Power	-	Controlled by D1_ON_OFF on J3 Pin 8. Enabled pin 2 is tied to GND.

Table 7: J6 Pin Descriptions

Pin	Schematic Signal	Type	Standard	Notes
1	+5V	Power	-	Total external draw on 5V supply should not exceed 1000mA
2	GND	Power	-	Controlled by D2_ON_OFF on J3 Pin 16. Enabled pin 2 is tied to GND.

Table 8: J2 and J6 Pin 2 Logic States

D1/D2_ON_OFF	Pin 2
High	GND
Low	Floating

Critical Link, LLC
6712 Brooklawn Parkway
Syracuse, NY 13211
PHONE 315.425.4045
FAX 315.425.4048
www.CriticalLink.com

Expansion Headers to Industrial IO Board – J1, J3 and J4

Indy Camera Expansion Board Connector	Industrial IO Board Connector
J1	J700
J3	J702
J4	J701

Table 9: J1 Connector Pin Assignments – Connected to J700 of Industrial IO Board

Pin	Signal	Type	Standard	Notes
1	GND	Power		
2	GND	Power		
3	GND	Power		
4	GND	Power		
5	+3.3V	Power		250mA Max (Per pin) 1A Total External Draw
6	+3.3V	Power		250mA Max (Per pin) 1A Total External Draw
7	+3.3V	Power		250mA Max (Per pin) 1A Total External Draw
8	+3.3V	Power		250mA Max (Per pin) 1A Total External Draw
9	RESERVED			
10	RESERVED			
11	RESERVED			
12	RESERVED			
13	RESERVED			
14	RESERVED			
15	RESERVED			
16	RESERVED			
17	RESERVED			
18	RESERVED			
19	RESERVED			
20	RESERVED			
21	RESERVED			
22	RESERVED			
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36	RESERVED			
37	RESERVED			
38	RESERVED			
39	RESERVED			
40	RESERVED			
41	RESERVED			
42	RESERVED			
43	GND	Power		
44	RESERVED			
45	GND	Power		
46	RESERVED			
47	GND	Power		
48	GND	Power		
49	GND	Power		
50	GND	Power		

Critical Link, LLC
6712 Brooklawn Parkway
Syracuse, NY 13211
PHONE 315.425.4045
FAX 315.425.4048
www.CriticalLink.com

Table 10: J3 Connector Pin Assignments – Connected to J702 of Industrial IO Board

Pin	Signal	Type	Standard	Notes
1	GND	Power		
2	GND	Power		
3	Servo_X	O	LVTTL	Hardware Configurable FPGA IO
4	RESERVED			
5	RESERVED			
6	RESERVED			
7	RESERVED			
8	D1_ON_OFF	O	LVTTL	Hardware Configurable FPGA IO
9	D9	I/O	3.3V LVCMOS	Hardware Configurable FPGA IO
10	D8	I/O	3.3V LVCMOS	Hardware Configurable FPGA IO
11	EXPOSURE	I/O	3.3V LVCMOS	Hardware Configurable FPGA IO
12	Servo_Y	O	LVTTL	Hardware Configurable FPGA IO
13	RESERVED			
14	RESERVED			
15	RESERVED			
16	D2_ON_OFF	O	LVTTL	Hardware Configurable FPGA IO
17	RESERVED			
18	PIXCLK	I/O	3.3V LVCMOS	Hardware Configurable FPGA IO
19	RESERVED			
20	RESERVED			
21	RESERVED			
22	RESERVED			
23	RESERVED			
24	RESERVED			
25	RESERVED			
26	RESERVED			
27	RESERVED			
28	RESERVED			
29	RESERVED			
30	RESERVED			
31	RESERVED			
32	RESERVED			
33	RESERVED			
34	RESERVED			
35	RESERVED			
36	RESERVED			
37	RESERVED			
38	RESERVED			
39	RESERVED			
40	RESERVED			
41	RESERVED			
42	SDAT	I/O	3.3V LVCMOS	Hardware Configurable FPGA IO
43	RESERVED			
44	SCLK	I/O	3.3V LVCMOS	Hardware Configurable FPGA IO
45	RESERVED			
46	RESERVED			
47	RESERVED			
48	RESERVED			
49	GND	Power		
50	GND	Power		

Critical Link, LLC
6712 Brooklawn Parkway
Syracuse, NY 13211
PHONE 315.425.4045
FAX 315.425.4048
www.CriticalLink.com

Table 11: J4 Connector Pin Assignments – Connected to J701 of Industrial IO Board

Pin	Signal	Type	Standard	Notes
1	GND	Power		
2	GND	Power		
3	RESERVED			
4	PIXCLK 1	I/O	3.3V LVCMOS	Hardware Configurable FPGA IO
5	D7	I/O	3.3V LVCMOS	Hardware Configurable FPGA IO
6	D6	I/O	3.3V LVCMOS	Hardware Configurable FPGA IO
7	D5	I/O	3.3V LVCMOS	Hardware Configurable FPGA IO
8	D4	I/O	3.3V LVCMOS	Hardware Configurable FPGA IO
9	D3	I/O	3.3V LVCMOS	Hardware Configurable FPGA IO
10	D2	I/O	3.3V LVCMOS	Hardware Configurable FPGA IO
11	D1	I/O	3.3V LVCMOS	Hardware Configurable FPGA IO
12	D0	I/O	3.3V LVCMOS	Hardware Configurable FPGA IO
13	FV	I/O	3.3V LVCMOS	Hardware Configurable FPGA IO
14	LV	I/O	3.3V LVCMOS	Hardware Configurable FPGA IO
15	GND	Power		
16	GND	Power		
17	P3 Pin 1	I/O	3.3V LVCMOS	ARM Software configurable GPIO
18	LED_4	O	3.3V LVCMOS	ARM Software configurable GPIO
19	P3 Pin 2	I/O	3.3V LVCMOS	ARM Software configurable GPIO
20	LED_3	O	3.3V LVCMOS	ARM Software configurable GPIO
21	P3 Pin 3	I/O	3.3V LVCMOS	ARM Software configurable GPIO
22	LED_2	O	3.3V LVCMOS	ARM Software configurable GPIO
23	P3 Pin 4	I/O	3.3V LVCMOS	ARM Software configurable GPIO
24	LED_1	O	3.3V LVCMOS	ARM Software configurable GPIO
25	RESERVED			
26	RESERVED			
27	I2C0_SCL	I/O	3.3V LVCMOS	ARM Software configurable
28	I2C0_SDA	I/O	3.3V LVCMOS	ARM Software configurable
29	GND	Power		
30	GND	Power		
31	GND	Power		
32	GND	Power		
33	-12V	Power		250mA Max (Per pin) 1A Total -12V
34	-12V	Power		250mA Max (Per pin) 1A Total -12V
35	-12V	Power		250mA Max (Per pin) 1A Total -12V
36	-12V	Power		250mA Max (Per pin) 1A Total -12V
37	+3.3V	Power		250mA Max (Per pin) 1A Total 3.3V
38	+3.3V	Power		250mA Max (Per pin) 1A Total 3.3V
39	+3.3V	Power		250mA Max (Per pin) 1A Total 3.3V
40	+3.3V	Power		250mA Max (Per pin) 1A Total 3.3V
41	+5V	Power		250mA Max (Per pin) 1A Total 5V
42	+5V	Power		250mA Max (Per pin) 1A Total 5V
43	+5V	Power		250mA Max (Per pin) 1A Total 5V
44	+5V	Power		250mA Max (Per pin) 1A Total 5V
45	+12V	Power		250mA Max (Per pin) 1A Total +12V
46	+12V	Power		250mA Max (Per pin) 1A Total +12V
47	+12V	Power		250mA Max (Per pin) 1A Total +12V
48	+12V	Power		250mA Max (Per pin) 1A Total +12V
49	GND	Power		
50	GND	Power		

Critical Link, LLC PHONE 315.425.4045
6712 Brooklawn Parkway FAX 315.425.4048
Syracuse, NY 13211 www.CriticalLink.com

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Storage Temperature Range	-65 to 80C

OPERATING CONDITIONS

Commercial Temperature Range	0 to 70C
Humidity	0 to 95% Non-condensing

Critical Link, LLC
6712 Brooklawn Parkway
Syracuse, NY 13211
PHONE 315.425.4045
FAX 315.425.4048
www.CriticalLink.com

ORDERING INFORMATION

The following table lists the orderable configurations. For shipping status, availability, and lead time of these or other configurations please contact your Critical Link representative.

Table 12: Orderable Model Numbers

Model
80-000322

MECHANICAL INTERFACE

A mechanical outline of the Indy Camera Expansion Board is illustrated below.

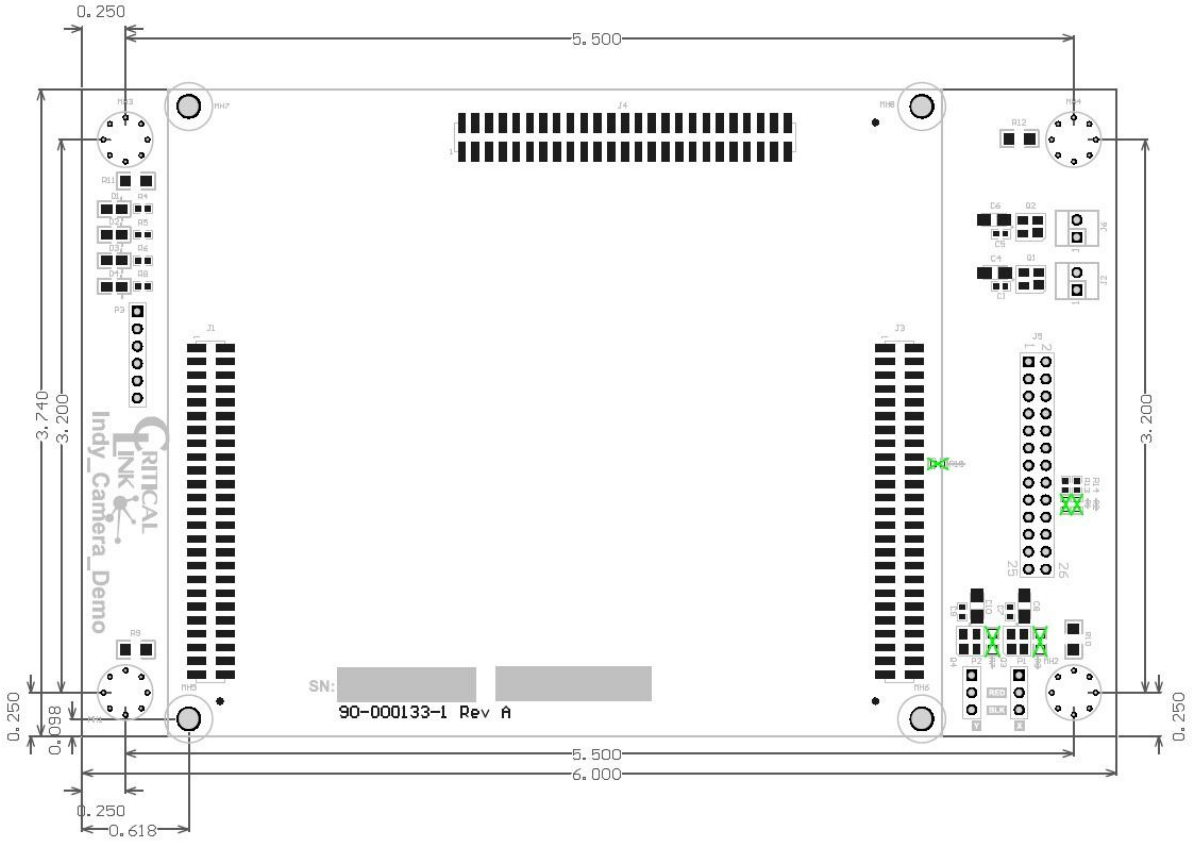

Figure 2: Dimensions 6.0" x 3.75"

REVISION HISTORY

Date	Change Description
13-JUN-2012	Initial revision.

Critical Link, LLC
6712 Brooklawn Parkway
Syracuse, NY 13211
PHONE 315.425.4045
FAX 315.425.4048
www.CriticalLink.com